CMOS-compatible highly efficient polarization splitter and rotator based on a double-etched directional coupler

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Abstract: We present a highly efficient polarization splitter and rotator (PSR), fabricated using 248 nm deep ultraviolet lithography on a silicon-on-insulator substrate. The PSR is based on a double-etched directional coupler with a length of 27 µm. The fabricated PSR yields a TM-to-TE conversion loss better than 0.5 dB and TE insertion loss better than 0.3 dB, with an ultra-low crosstalk (−20 dB) in the wavelength regime 1540–1570 nm.

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References and links
1. Introduction

Silicon photonics built on a silicon-on-insulator (SOI) platform has received much attention in recent years due to its compatibility with complementary metal-oxide-semiconductor (CMOS) technology, which makes the mass production of photonics devices cost-effective [1,2]. The intrinsic high-index contrast property of SOI allows for photonics with very small footprint [3,4], which is highly desirable for system integration. However, this property results in high polarization dependence for silicon photonic devices. To solve this problem, polarization diversity circuits have been proposed [5–7], which could be divided into two types [8]. One is based on a polarization splitting grating coupler (PSGC) [9], which is limited by the insertion loss and bandwidth of the PSGC. Another approach is based on a polarization splitter and rotator (PSR), connected to an edge coupler that can couple both TE and TM input modes [10,11].

PSRs based on symmetrical directional couplers have been successfully demonstrated [8,12,13]. However, these demonstrations are either simulation work or experimental demonstrations based on electron beam lithography (EBL) with air as top cladding. This lack of cladding breaks the mirror symmetric of an un-etched waveguide, making a polarization rotator easier to construct. Meanwhile, this same lack of solid cladding layer makes these devices incompatible with most metal back-end-of-line (BEOL) processes, and thus greatly complicates integration with other SOI photonic devices. Polarization rotators (PRs) using silicon dioxide layer as cladding were recently demonstrated in [14,15] on a 220 nm SOI platform using a 193 nm deep UV photolithography. However, the worst-case insertion loss of this device is 2.5 dB.

In this letter, we experimentally demonstrate a compact, very low loss PSR on a 220 nm SOI platform using 248 nm lithography. The length of the device is 27 µm. It uses a double etch with 220 nm deep etch and 90 nm shallow etch as well as a silicon dioxide cladding. A 0.3 dB TE-to-TE insertion loss and a 0.5 dB TM-to-TE conversion loss over a bandwidth of 30 nm are measured.

2. Principle and simulation

2.1 Device principle

The proposed PSR is schematically depicted in Fig. 1. Both TE₀ and TM₀ modes are sent into the ridge waveguide on the bottom left. In case of the TE₀ mode, the beam will keep propagating along this ridge waveguide and exit from the through port. To make this happen, a significant difference between the effective refractive indices of the TE₀ mode in the ridge waveguide and modes in the double-etched waveguide should be maintained. On the other hand, TM₀ mode should be coupled to the right-hand side and converted to TE₀ mode at the cross port. In order to achieve an efficient cross-polarization coupling, both horizontal and vertical symmetry need to be broken [8]. Since silicon dioxide is used as the top-cladding to enable compatibility with our metal BEOL processes, vertical symmetry could not be broken by using air as top-cladding. Inspired by the work of [14–17], we use a double-etched waveguide to break the two dimensional symmetry. In addition, we need to make sure that the effective refractive index of the TM₀ mode in the ridge waveguide and that of the TE₀ mode in the double-etched waveguide are close enough to achieve strong cross-polarization coupling.
The device is designed on a SOI wafer with top silicon thickness \( H_1 = 220 \text{ nm} \) and partial-etched silicon thickness \( H_2 = 90 \text{ nm} \). On the left hand side, we choose ridge waveguide with width \( W_1 = 480 \text{ nm} \) and length \( L_5 = 21 \mu\text{m} \). After the waveguide, a bend is used to prevent further coupling between the two parallel waveguides. Separated by gap with width \( W_g = 0.2 \mu\text{m} \), a double-etched waveguide is used on the right-hand side, which is made from three sections. The first section is a bend with bending radius \( L_1 = 5 \mu\text{m} \), which is used to make an adiabatic transition of the refractive index and therefore reduce the backscattering when launching light at the input port. The second section is a coupling section with a length \( L_2 = 19 \mu\text{m} \). The fully-etched layer has a width \( W_2 = 0.19 \mu\text{m} \), and the partial-etched layer has a width \( W_3 = 0.2 \mu\text{m} \).

Figure 2 shows the effective indices for the two waveguides as the wavelength increases from 1.54 \( \mu\text{m} \) to 1.57 \( \mu\text{m} \). As can be seen, the effective refractive index of the TE\(_0\) mode in the ridge waveguide is far from that of the TE\(_0\) or TM\(_0\) mode in the double-etched waveguide. This will prevent mode coupling between the two waveguides when injecting TE\(_0\) mode. In addition, the effective refractive index of the TM\(_0\) mode in the ridge waveguide is very close to that of the TE\(_0\) mode in the double-etched waveguide. Although this does not satisfy the exact phase
matching condition, it is already close enough to result in a strong cross-polarization coupling between the two waveguides. The third section is a taper, which is used to transform the double-etched waveguide into a ridge waveguide, with taper length of $L_3 = 3 \, \mu m$.

![Fig. 3. Simulation results for the intensity of light when launching (a) TE mode and (b) TM mode as the input.](image)

To verify the behavior of this device, three-dimensional finite-difference-time-domain (3-D FDTD) simulation was performed. Figure 3 shows the intensity of light when launching TE$_0$ mode and TM$_0$ mode as the input. As expected, when launching TE$_0$ mode at the bottom left, the beam travels through the ridge waveguide and exits from the through port without coupling to the double-etched waveguide. On the contrary, when launching TM$_0$ mode at the bottom left, the beam is efficiently coupled to the double-etched waveguide and exits from the cross port.

![Fig. 4. Total electrical field amplitude ($|E|$) profile as the input TM$_0$ field travels through the PSR](image)

The TM$_0$ mode coupling process is further explained in Fig. 4, which shows the total electrical field amplitude at different cross sections. At cross section (I), most of the power is carried by the TM$_0$ in the ridge waveguide. Only a small portion of the power has been coupled to the double-etched waveguide. At cross section (II), most of the power has been transferred to the TE$_0$ mode in the double-etched waveguide. At cross section (III), the two waveguides are separated so far away that light could not couple back from the double-etched waveguide to the ridge waveguide any more, so the TE$_0$ mode in the ridge waveguide would maintain most of
the power. At cross section (IV), there is only the right-hand waveguide, which has tapered to a ridge waveguide.

2.2 Fabrication sensitivity discussions and critical dimension (CD) SEM data

To investigate the fabrication tolerance, five key geometry parameters ($W_1$, $W_2$, $W_3$, $H_2$, and $W_g$) have been varied within $\pm 10$ nm. As shown in Fig. 5, the polarization conversion loss does not experience any obvious degradation as $W_1$, $W_3$, and $W_g$ change. Thus, it is safe to conclude that the device has a high fabrication tolerance towards $W_1$, $W_3$, and $W_g$. However, it is also evident that this device is relatively sensitive to $W_2$ and $H_2$, though excess losses remain relatively modest even for 10 nm deviations in the case of $W_2$. Controlling these fabrication dimensions will be a challenge in achieving the ultra-low loss of 0.5 dB.

CDSEM data and layer thickness measurements were available for standard process characterization structures from the wafer that we tested. Based on several measurements across the wafer, we report that a 200 nm wide fully etched waveguide yields with $192 \pm 4$ nm width, the unetched silicon thickness is $211.8 \pm 2.4$ nm, and the partially etched layer thickness is $96.8 \pm 7.5$ nm. The CDSEM data we present is not taken from the actual device tested, but it does suggest that the fabricated dimensions are likely in fairly close agreement with the design.
values, in all cases with the average under 10 nm from the design goal. This data supports our belief that the device we report on likely has dimensions quite close to the design goal.

3. Fabrication and experimental results

3.1 Device fabrication

The device was fabricated on an 8-inch SOI wafer, consisting a 220 nm thick silicon film on top of a 2 µm thick buried oxide layer (BOX). Three masks were used to pattern the wafer using 248 nm deep ultraviolet lithography. The first mask defined the 220 nm silicon height used for gratings and waveguides. The second mask was used to define a 160 nm silicon layer, which is used for the grating teeth. The final mask defined the 90 nm layer for the double-etched PSR. Finally, un-patterned areas were fully etched to the BOX and an oxide layer was deposited as the top cladding. Figure 6(a) shows the fabricated PSR with two calibration structures and Fig. 6(b) shows only the PSR.

![Fig. 6. Optical micrograph of the fabricated devices (a) PSR with two calibration structures (b) PSR.](image)

3.2 Testing configuration

The device performance was characterized on a wafer scale optical test setup, by means of grating couplers [14,15]. First, light was generated from a tunable laser at 1550 nm, with its polarization state controlled by a polarization controller. Then, the light was coupled into the device under test by aligning a pair of polarization-maintaining fibers to a set of input and output periodic single-polarization grating couplers (SPGCs). These SPGCs are highly polarization dependent [18], which preserve low loss for designed polarization state, but show high extinction ratio to perpendicular polarization state. The periodicity of the TE SPGC is 0.63 µm, with a duty cycle of 65%. And the periodicity of the TM SPGC is 0.93 µm, with a duty cycle of 76%. The phase match condition for both TE SPGC and TM SPGC are satisfied simultaneously at a 17° incidental angle. 3-D FDTD simulations showed that both the TE SPGCs and TM SPGCs exhibit above 25 dB polarization extinction ratios. Measurements were made on control structures containing TE SPGCs to determine their polarization crosstalk value for TM modes, and the results were in agreement with these simulated values. Given the broadband performance seen with minimal ripples in the output spectra, and the fact that the input polarization states were carefully controlled, we do not anticipate polarization crosstalk to have been a significant factor in adding noise or uncertainty to our measurements.
To extract the actual response of the PSR, we need to characterize the TE and TM SPGCs used in the PSR characterization structure first. We designed a characterization structure for the SPGCs, which consist of two identical SPGCs connected by a silicon waveguide. Calibration farms containing four TE SPGC loops and four TM SPGC loops were measured and the spectral responses of these devices are shown in Fig. 7. The peak coupling efficiency of the SPGC are located at 1547 nm, which is very close to the desired peak point at 1550 nm. More importantly, the spectral response of the TM SPGCs and TE SPGCs are quite consistent, with a maximum deviation of 0.3 dB. So it would be reasonable to use the average of these responses as the spectral response in PSR calibration structure. In addition, two different structures are used to calibrate the loss and crosstalk of the PSR, as shown in Fig. 6(a). Both structures have 3 ports and use the center port as the input. The first structure measures the response of the PSR to TM input. Similarly, the other structure measures the response of the PSR to TE input. It should be noted that while the grating couplers changed between the two structures, the structure of the PSR itself was designed to be identical.

3.3 Device performance

By subtracting the loss caused by the grating couplers, we can get the losses due to the PSR. As shown in Fig. 8(a), the PSR shows a TM-to-TE conversion loss better than 0.5 dB and a TE insertion loss better than 0.3 dB over a wavelength range of 30 nm. As shown in Fig. 8(b), the crosstalk of this device is below −20 dB. As far as the authors know, this is the lowest crosstalk that has ever been demonstrated on a SOI platform. In addition, it is worth noting that there is an excellent match between the simulation results and the measurement results. There is a slight possibility that TM0 on-chip radiation coupling through a TE SPGC or TE0 on-chip radiation coupling through a TM SPGC could influence the data shown in Fig. 8(b). However, in light of the expected 25 dB polarization selectivity of the SPGCs, and the fairly close agreement between the simulated crosstalk values and the measured results, we believe that the data shown in Fig. 8(b) comfortably supports our assertion of crosstalk lower than −20 dB.
Finally, we note that unlike the TE and TM grating coupler calibration loops, for the PSR device, one must align to a TE and TM grating coupler loop simultaneously. Since a fiber array was used, this meant that the incident angle was fixed for the fibers over both couplers, and a strict relative position between the two fibers was also enforced. We performed our layout so that ideally, both grating couplers would be coupled to simultaneously with the same high efficiency that was achieved for the isolated TE and TM grating coupler loop calibration structures. However, it is possible that fully optimal coupling is not obtained simultaneously for either or both grating couplers. We note that in such a situation, the normalization procedure we have used to identify the PSR losses would result in an over-estimation of the PSR losses. This is because the additional losses from the TE and TM grating coupler misalignment would be incorrectly attributed to the PSR device.

4. Conclusion

We experimentally demonstrated a fully CMOS compatible compact and low loss polarization rotator and splitter. The 27 µm long device features a TM-to-TE conversion loss above 0.5 dB and a TE insertion loss above 0.3 dB over a wavelength range of 30 nm, with an ultra-low polarization crosstalk (~20 dB). The solid cladding buffer layer makes this device compatible with metal back-end-of-line (BEOL) processes. The result is lowest conversion loss demonstrated to date for polarization splitter and rotator using deep UV photolithography on a SOI platform.

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