ABSTRACT

In our digital world, microelectromechanical system (MEMS) are here to stay and will open the doors for the next exciting wave in the advancement of technology such as the Internet of Things (IoT). The MEMS devices in wafer forms are fabricated in minute details and eventually singulated into individual units to act as sensing or actuation elements in various applications such as accelerometer and gyroscopes for navigation, in wireless mobile and smart car applications. Handling of such MEMS device require to overcome may challenges in both fabrication and assembly. Singulation of MEMS device with fragile and sensitive structures is one of the many assembly challenges. In fact, most devices are capped to protect its active moving components that may be damaged when using conventional singulation method that is by mechanical dicing wherein water splashes or pressure is unavoidable. With the introduction of stealth laser dicing, where micro damage is created internally and through several layers of this damages creates a propagation to eventually separate the wafer upon forced expansion through tape, it became possible for a dry process singulation without damaging the fragile components. However, stealth dicing leverages on infrared waves being transparent only and able to penetrate through smooth surface silicon wafers and at certain resistivity or level of doping to create internal damage on the workpiece. As such, stealth dicing process may have difficulty to handle saw street with metallization, heavily doped or high resistivity wafer as in the case of SOI wafer and deep trenches that may surface in some MEMS devices. This created limitations for MEMS designs, processes and materials selection that may not be limited to the active region alone but as well as on the dicing saw street.

In this paper we will conduct stealth dicing study on various type of wafer configuration and thus making a clearer assembly process for next generation of mobile applications and the fast growing market of IoT.

Key words: MEMS, Stealth Dicing, Front/Backside Irradiation, Singulation, Laser Dicing

INTRODUCTION

With the popularity of smart mobiles, wearable devices applications and MEMS sensors and actuators, the innovation and complexity of MEMS are in rapid development. And with the availability of low-cost SOI wafers, new thin films, electrode material and structural membranes are emerging and showing greater overall electrical performance and manufacturability advantage. Other than SiO2, AlN and Mo are structured as thin film diaphragm or suspended type cantilever as it has good piezoelectric characteristics, high temperature stability and good resistance to permanent deformation leading to a stable performance as an energy harvester, resonators, transducers and chemical or physical sensing devices. All these are too fragile to handle in singulation process. The use of encapsulation or capping process help to mitigate the dicing process issue. Usually, this additional process steps introduces other defects which is not limited to CTE mismatch of metal bond or shrinkage of capping adhesive materials but also may cause performance to deteriorate. But without protection, dicing method with a blade spindle spinning at rotation speed of as much as 40,000 rpm is a killer which brings tiny water spray and saw dust slurry to a high energy trajectory that will destroy fragile MEMS structures. To the rescue is the new technology of stealth dicing which has far more advantages than the wet process of conventional water cooled blade dicing or the equally popular ablation-protection-coated laser dicing as shown in Fig. 1 where water is use to wash and clean the ablation debris and remove the coating materials.

![Fig. 1 – Laser Ablation with Coating/Wash](image)

For several years now Stealth Dicing has gained popularity and was showcased in a wide variety of application. Very much recent works such as of A. Podpod et al demonstrated stealth dicing as no induced damage technique for low-k dielectric materials with Cu interconnects and well suited into 3D integration technology [1]. Even for a complex multi patterned dies as small as 1x1 mm on DAF tape with Disco’s Hasen cut,
laser ON/OFF control capability, die separation with clear unit gaps after stealth dicing can be well established [2]. W.H. Teh et al demonstrated stealth dicing optimization and defect elimination for dicing before grind application as well as thin die strength enhancement for NAND memory wafers [3]. S. Takyu et al proved that stealth dicing has very wide advantage for WLCSP with dicing through tape even with a backside protection film. Stealth dicing not only helps to eliminate die crack but also improved cost with a much narrower street width requirement [5]. This can also be true and much applicable with MEMS devices. However, similar and those mentioned, many papers have also written elaborate explanation of how stealth dicing works but a few have discussed its application/issues/challenges in MEMS devices. It seems edge chip cracks are common as S. Shao et al have tried to investigate and determine the causes of failure from different areas with an aid of FEA modeling and showed that the laser processing has the most significant effect on die stress [5].

In order for complex, thin fragile membranes to maintain its structure during singulation, there is a need of proper dicing process step. Stealth dicing is the best singulation technology to go for MEMS wafers because it is now a well-established dry process, it has cost reduction implications and it allows damage free processing. However, like any other process there are also difficulties that needs to be understood and overcome.

This paper will help to show and bring out the potential problems by demonstrating approaches to address this issues. It will cover the following four methodologies for MEMS design considerations.
1. MEMS wafer with inevitable saw street metallization.
2. SOI wafers with different device and carrier thickness.
3. Wafers with low device resistivity < 1ohm-cm:
4. Narrow trenched dicing saw street.

Upon each simulation, observations of results were made by physical visual inspection of separation and thru microscope to check straightness of cut, extent of damage on active region and damage to fragile structures.

EXPERIMENTAL

In stealth dicing, an infrared wavelength laser beam internally penetrates and modifies a tiny layer within the wafer by utilizing temperature dependence of absorption coefficient of the wafer creating a crack initiation and eventual separation by a subsequent tape expansion process [6]. A typical stealth dicing set-up is shown on Fig. 2 which is normally called front-side irradiation.

Another approach is by backside laser irradiation wherein the wafer surface is placed facing the chucktable protected by a porous sheet (see Fig. 3).

In this experiments, both methods of irradiation will be employed to suit the type of test vehicle wafer using Disco DFL7361 with SDE06 Engine series. After laser process, wafers are separated with a Disco die separation system, DDS2300 series. In all experiments, a suitable transparent stealth dicing tape is used to mount the 8inch size wafers on a ring frame.

I. MEMS with Saw Street Metallization

Laser is blocked by a metal layer such as Cu and not able to create internal damaged layer.

As such, it is highly recommendable for the saw street saw street to be free of any blocking metallization for stealth dicing. However, Cu is difficult to etch and other metals removal could result to additional steps incurring an increase in cost. We have designed an experiment to study both irradiation method using a metallized saw street wafer as shown on Table 1 and determine on what extent the stealth dicing is capable of singulating wafers with inevitable saw street metallization.
Table 1. Experiment on wafer with metal on saw street

<table>
<thead>
<tr>
<th>S/n</th>
<th>Wafer Type</th>
<th>Saw Street Description</th>
<th>Method of SD Irradiation</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Bare Silicon (Baseline)</td>
<td>Bare Silicon, 725 µm thick</td>
<td>Front-side Irradiation</td>
</tr>
<tr>
<td>2</td>
<td>With Metal, 1mm x 1mm die size</td>
<td>0.7µm Al/1µm stack of thin film, Si 725 µm thick</td>
<td>Front-side Irradiation</td>
</tr>
<tr>
<td>3</td>
<td>With Metal, 1mm x 1mm die size</td>
<td>0.7µm Al/1µm stack of thin film, Si 725 µm thick</td>
<td>Backside Irradiation</td>
</tr>
</tbody>
</table>

II. SOI Wafer and III. Doped wafer with Low Resistivity

Silicon on Insulator (SOI) are widely used in MEMS fabrication to create low stress and high reliable cantilevers and beams. On the other hand, highly doped wafers are common to enhance the electrical characteristic and functionality of the device. However, other than SD process recommendation of pure silicon on saw street, wafers should have resistivity of more than 1 Ω-cm for the infra-red laser to be transmitted on the internal layer. In this paper, we had prepared an experiment as shown in Table 2 to understand as well as validate Stealth Dicing capabilities for highly doped SOI MEMS wafers.

Table 2. Experiment on SOI and Highly doped wafers

<table>
<thead>
<tr>
<th>s/n</th>
<th>Wafer Type</th>
<th>Saw Street Material Stack</th>
<th>Wafer Resistivity, Ω-cm</th>
<th>Trench Width x Depth</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Si Full substrate</td>
<td>SiO2 / SiN</td>
<td>&lt; 1 to 0.01</td>
<td>400A Al2O3, 2µm Stack of dielectric, 725µm Si</td>
</tr>
<tr>
<td>2</td>
<td>20µm SOI</td>
<td>20µm Si / 2 µm SiO2</td>
<td>0.01                    &gt; 1</td>
<td>300µm x 100µm</td>
</tr>
<tr>
<td>3</td>
<td>30µm SOI</td>
<td>30µm Si / 2 µm SiO2</td>
<td>0.01                    &gt; 1</td>
<td></td>
</tr>
</tbody>
</table>

Substrate with high resistivity and low resistivity are processed with front-side and backside irradiation process and determine penetrability of infrared. SOI wafers are prepared with different thickness of device with a SiO2 insulator of 1–2µm thickness. The device layer was doped and the resistivity is below the recommended level for infrared beam to penetrate. Silicon substrate having the required resistivity of more than 1 Ω-cm is expected to have no issue with IR penetration.

IV. Trenched Dicing Saw Street

It was noted that for laser to be fully absorbed by the material it is best to have a polished surface. Infrared is affected by rough surfaces such that it could deflect some light beams in other direction. In this section, it will not be about roughness but to a much greater surface unevenness, a deep trench on the the saw street of the wafer. A 100µm width, which is a typical value for a so called narrowed saw street technology, and a trenched depth of 100µm, SOI wafers can be trenched up to the BOX layer or beyond the insulator. For this vehicle, device silicon layer and all of its thin stack are etched beyond the SiO2 insulator. Fig. 5 shows a trenched dicing saw street of 100µm and 100µm depth.

Fig. 5 – Trenched Dicing Saw street

In comparison, another wafer with opening trench width of 300µm was prepared. This experiment will demonstrate a solution on how uneven wafer surface due to deep trench saw street can be overcome by stealth dicing.

Table 3. Experiment on Deep Trenched Saw Street

<table>
<thead>
<tr>
<th>s/n</th>
<th>Wafer Description</th>
<th>Trench Width x Depth</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>400A Al2O3, 2µm Stack of dielectric, 725µm Si</td>
<td>100 µm x 100µm</td>
</tr>
<tr>
<td>2</td>
<td>Substrate thickness</td>
<td>300µm x 100µm</td>
</tr>
</tbody>
</table>

RESULTS AND DISCUSSIONS

I. MEMS with Saw Street Metallization

Laser characterization performed on the bare silicon wafer is shown on Fig 6. This was done to demonstrate mainly the effects of power parameter at constant typical value of laser frequency which is good enough to represent the wafer with the metal in case of failure in separation. Obviously all runs were able to separate the bare silicon wafers.

Fig. 6 – Second round selection experimental results
Same set or recipe, was tried on the wafer with metal however even with the most power and number of pass, the laser was not able to penetrate and create a separation using front-side irradiation process. Even further increasing the power and defocus amount only results to apparent ablation but it still failed to create an impact on the Aluminum layer, see Fig 7 (a). This proves again that SD front-side irradiation is not applicable for metalized saw street also as seen on the infrared scope, infrared was not able to pass thru the Aluminum layer. On the third leg, backside irradiation fires mainly on the silicon while the metal is far from the other end.

II. SOI Wafer and III. Doped Wafer with Low Resistivity

Laser beam penetration is difficult due to low transparency of highly doped wafer for both backside and topside irradiation approach as seen on Fig. 8 on a full silicon low resistivity wafer. High frequency and power can be employed but as the laser beam goes deeper on the silicon, the infrared was dissipated and absorbed by the bulk of low resistivity silicon until it cannot create a damage on the silicon. However, it is observed that even with fully doped low resistivity wafer, infrared can create a damage up to 160µm. Therefore it can be said that SOI with low resistivity device would be able to penetrate on the remaining Silicon substrate. This was proven on the next leg.

![Front Side Irradiation](image1)
![Backside Irradiation Result](image2)

**Fig. 7 – Second round selection experimental results**

Therefore, as what was observed on the bare silicon wafer, the bulk of silicon was already separated without the infrared laser touching on the metal layer. Fig 7 (b) shows the metal after separation during tape expansion. The result of the experiment proved that stealth dicing is applicable for MEMS with metallized saw street.

It was observed on the 20µm and even on the 30µm SOI wafer that it is possible to separate even with front-side irradiation as shown on Fig. 9 below.

![Laser Irradiating on Low Resistivity wafers](image3)

**Fig. 8 – Laser Irradiating on Low Resistivity wafers**

![Laser Irradiating on Low Resistivity wafers](image4)

**Fig. 9 30µm SOI SD Laser Internal Layer**

Employing both front-side and backside irradiation process will create internal damage on the full low resistivity wafer at the right thickness by further optimizing laser intensity and number of laser pass. Therefore there is still a possibility to fully utilize stealth dicing technology for this kind of applications.

IV. Trenched Dicing Saw Street

Having a blockage of laser intensity from the top surface street layer and tapered laser beam requires wider saw street trench opening. This was the observation from the results of 100µm and 300µm opening width. With the 100µm deep saw street and 100µm opening width, front laser damage is evident but the laser could not get thru the bulk of the silicon using front-side irradiation because of the injection angle of the infrared light. However, there was no evident backside penetration damage. Internal damage from top to backside of wafer is important for the separation of the unit. Further increasing of laser intensity only creates further damage on the top side, shown in Fig. 10, without much effect on the backside as there are only 2 passes observed while there are supposed to have 7 passes. This phenomenon was not seen when the trench width was opened to 300µm.

![100µm Trench top side ablation](image5)

**Fig. 10 100µm Trench top side ablation**

As demonstrated, if front-side irradiation does not usually work with the standard stealth dicing recipe, backside irradiation can be of great help. This is true if the front surface fragile membranes and components can withstand a contact with another material and subjected to holding vacuum if bakside irradiation is chosen. Thru the course of this evaluations, particles and fragments silicon remnants has been found on the porous chuck. As
validated, there were fragile components that was damage from cantilevers and thin membranes. Front-side irradiation is still the best choice at normal circumstances, therefore the real challenge to MEMS stealth dicing is still how to protect the fragile components in the front surface during stealth dicing.

CONCLUSIONS
Stealth dicing was proven to be the technology that has a solution to provide for the prevailing and evolving issues of conventional dicing methods even with the complexities of MEMS wafer applications. As a result of this study, vagueness on the capability of stealth dicing was given clarity and was not limited to the initial stated wafer requirement of an ideal condition. It is necessary to irradiate metalized saw street from the backside and that separation of this thin film metal layers could be possible. Similarly, SOI wafers can be singulated as well as highly doped low resistivity device wafers on a high resistivity substrate. It also revealed that saw street with deep trench may require wider trench opening width.

In summary, this paper has demonstrated the feasibility of stealth dicing on the following wafer configurations: (1) MEMS wafer with inevitable saw street metallization, (2) SOI wafers with different device and carrier thickness (3) Wafers with low device resistivity < 1ohm-cm and (4) Trenched dicing saw street.

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