Investigation on Reliability of Embedded Ultrathin Sensor Chip in Organic Substrate Under Drop Impact Loading by Stresses Monitor and FEM Simulation

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***Abstract*— Reliability of the embedded ultrathin device in the organic substrate packaging is one of the major concerns during its applications. In this paper, drop impact tests were conducted to the embedded ultrathin stress sensor chip in the organic substrate. Stresses were monitored with the embedded stress sensor chip based on silicon piezoresistive effects. Dynamic explicit finite element model with the input-G method was built up to investigate the stress and strain behaviors of the embedded chip and solder bump. The drop impact simulation model was validated by the experimental stresses monitoring result. It indicated that the discrepancy of the maximum normal stress σ_{11} at the center of embedded stress sensor chip from experimental and numerical simulation results could be within 30%. Based on the validated model, the effects of material properties and structural parameters on the stress and strain responses were studied with the numerical simulation results. The maximum normal stress σ_{11} at the embedded sensor chip and the equivalent plastic strain of the solder bump were selected as the indexes for the comparisons and optimizations. The experimental and numerical simulation efforts can provide design guidelines for the embedded ultrathin chip in the organic substrate packaging.**

***Index Terms*— Drop impact test, embedded packaging, finite element simulation, ultrathin stress sensor chip.**

I. INTRODUCTION

EMBEDDED packaging integrating both active and passive components into a single high density substrate, which can provide an effective solution to the system on package, has been paid more and more attention due to the demands of the high density, miniaturization, multifunctions, high performance, and low cost of the semiconductor industry [1]–[5]. The reliability of the embedded devices in the organic substrate packaging is one of the major concerns during its applications.

A novel thermosetting resin with a low elastic modulus, low dielectric constant, and low dielectric loss for the embedded passives and actives integral substrates was developed in [6]. The results show that the embedded passives and actives integral substrates have good reliabilities during the reflow process and thermal cycling test. Finite element model of the embedded chip into the substrate was built up in [7] to study the effects of chip thickness, chip location, chip shape, solder bump, and material properties on the stress level under the thermal loading from 150 °C to 25 °C. The heat dissipation and thermal stress of the active embedded chips in the organic substrate were investigated through the numerical simulation in [8]. The drop impact reliability of the high density embedded substrate is also one of the key issues for its mobile applications. However, there is still lack of references could be found on drop impact reliability assessment for the embedded chip on the organic substrate packaging.

In this paper, we applied the stress senor chip combined with the numerical simulation to study the drop impact reliability of embedded ultrathin chip in the organic substrate. The stress sensor based on the silicon piezoresistive effects was used for monitoring the stresses under the drop impact loading. The stress and strain behaviors of the embedded ultrathin chip and solder bumps were also investigated dynamic explicit finite element simulation with the input-G method. The effects of material properties and structural parameters on the stress and strain responses of the embedded ultrathin sensor chip and solder bump were investigated.

II. STRESS SENSOR AND EMBEDDED PACKAGE

The developed silicon piezoresistive stress sensors were placed orthogonally for the measurement of the parallel and perpendicular components of the applied stress, as shown in Fig. 1. Four sensor rosettes were fabricated at different locations on a 5-mm × 5-mm chip, which has 36 I/Os with 0.5 mm in pitch. The manufacturing processes and calibration approach for the silicon piezoresistive stress sensor have been described in [9]–[11].

The 50-μm thickness stress sensor chip embedded into a JEDEC drop impact test board is shown in Fig. 2. Fine stress sensor chips were embedded on the PCB, which was located at U2, U4, U8, U12, and U14, respectively. And, the other locations on PCB were the dummy chips. The assembly

Manuscript received August 27, 2013; revised February 16, 2014; accepted May 13, 2014. Date of publication June 20, 2014; date of current version July 31, 2014. Recommended for publication by Associate Editor C. J. Bailey upon evaluation of reviewers' comments.

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Digital Object Identifier 10.1109/TCPMT.2014.2328015

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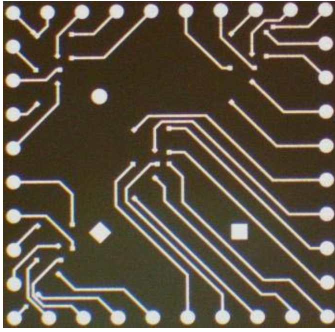

Fig. 1. Optical picture of stress sensor based on the piezoresistive effects.

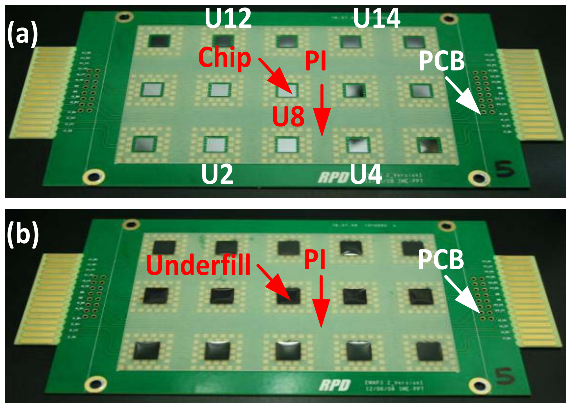

Fig. 2. Drop impact test board with ultrathin stress senor chips (a) after the flip chip bonding and (b) after the embedded process with underfill material.

TABLE I
STRUCTURAL DETAILS OF THE EMBEDDED ULTRATHIN STRESS SENSOR CHIP IN DROP IMPACT TEST BOARD

Component	Dimensions
Stress sensor chip	5 mm×5 mm×0.05 mm
Test board	132 mm×77 mm×1 mm
Solder bump diameter/pitch	200 μm/500 μm
Solder bump standoff	40 μm

and encapsulation processes are as follows. First, the stress sensor chips were bonded onto the copper pads inside the cavities of the printed circuit board (PCB) using the flip chip bonder (FC150). The cavities were fabricated by the polyimide (PI) coating on the PCB surface. Then, it was reflowed with the conventional lead-free solder reflow temperature profile. The assembled stress sensor chip on the PCB is shown in Fig. 2(a). After that a conventional underfill material was used to fill the cavity and the gap between the sensor chip and substrate, as shown in Fig. 2(b). The SnAgCu solder bumps with 200 μm in diameter and 40 μm in standoff were used as the interconnections. The structural specifications of the embedded stress sensor chip in the drop impact test board are listed in Table I. Fig. 3 shows the cross section of the embedded ultrathin stress sensor chip in the PCB test board after the underfill material curing at 150 °C. It shows that the ultrathin stress sensor chip was fully covered by the underfill material.

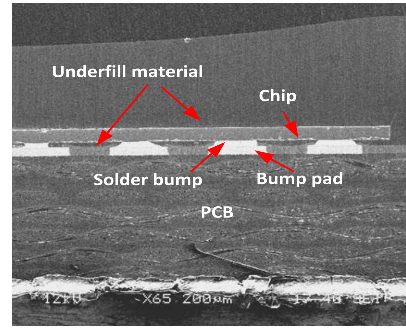

Fig. 3. SEM picture of the crosssection of the embedded ultrathin stress sensor chip in the drop impact test board.

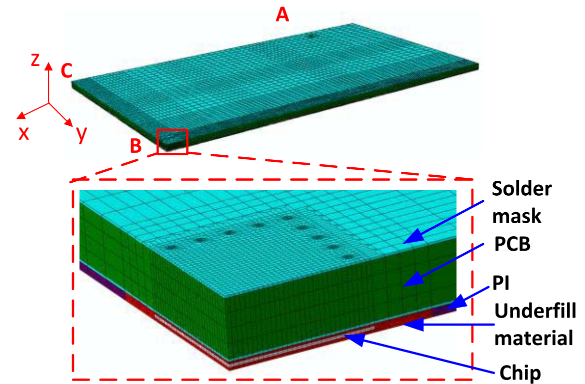

Fig. 4. Finite element model of drop impact test for the stress sensor chip embedded in the PCB board.

III. DROP IMPACT FEM MODELING AND VALIDATION

In order to further understand the stress and strain behaviors under the drop impact loading for the reliability design of the embedded substrate packaging, numerical simulation is an effective tool. In this paper, a quarter 3-D finite element model of the embedded stress sensor in the drop test broad was established, as shown in Fig. 4. The embedded ultrathin sensor chip package at the center of PCB was built up in detail according to the geometry dimensions described in Table I. And, the embedded sensor chip packages at the other positions on the drop impact test board were simplified as an equivalent structure. Then, coarse elements can be meshed on these packages in order to reduce the dynamic simulation task of the drop impact.

The drop impact tests of the embedded ultrathin sensor chip in the organic board were carried out according to the JEDEC standard JESD22-B111 under the loading of a half sine shock pulse with the amplitude of 1500 g and pulse width of 0.5 ms. The input-G method which directly applies the acceleration loading on the bolt holes of the PCB was demonstrated to be an effective way to simulate the drop impact test [12]–[17]. In our simulation model, 1500-g acceleration within 0.5 ms was directly applied onto the four bolt-holes on the PCB. And, a velocity of −4.77 m/s along the Z-direction was applied to the whole test board as the initial condition. The symmetry boundary conditions were applied on the cutoff edge of the quarter model. The dynamic explicit nonlinear

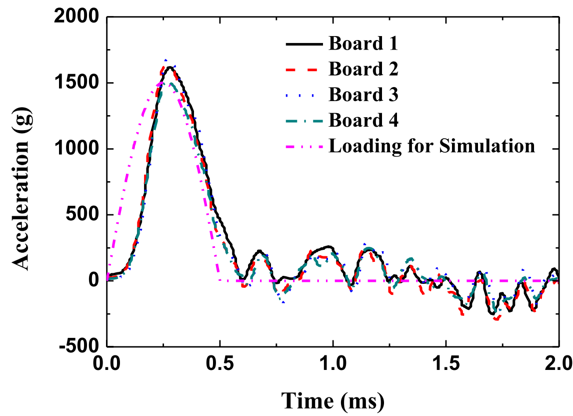

Fig. 5. Acceleration pulses of drop impact tests of different boards and the accelerations pulse applied in the numerical simulations.

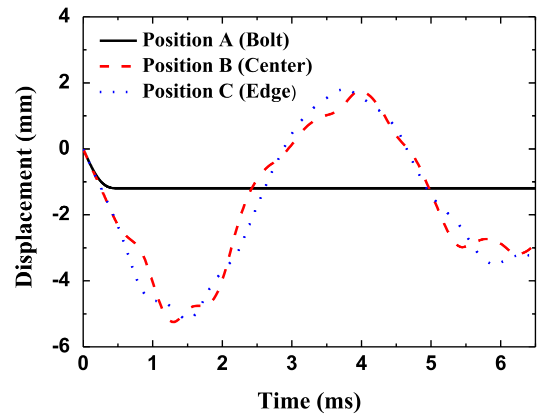

Fig. 6. Displacement evolutions of the different positions on the PCB during the drop impact test.

TABLE II
MATERIAL PROPERTIES USED FOR THE DROP IMPACT SIMULATION MODEL

Materials	Density Kg/m^3	Elastic Modulus (GPa)	Poisson's Ratio	Yield Stress (MPa)
Si	2329	131	0.28	-
Cu	8950	117	0.35	120
PI	2200	4	0.35	-
PCB	2000	25/x, y 10/z	0.11/x, y 0.39/z	-
Underfill	1900	6	0.31	-
Solder mask	1300	2.4	0.32	-
SnAgCu(305)	7390	40	0.35	rate dependent[18]

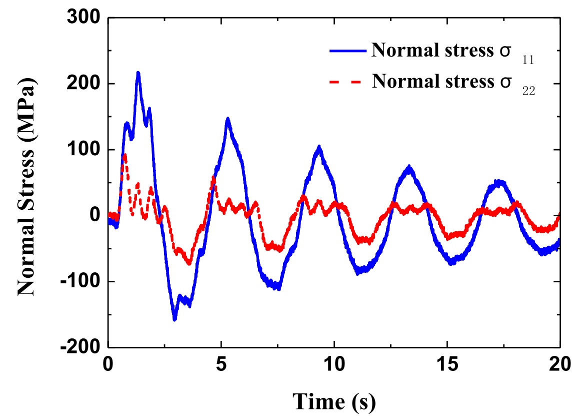

Fig. 7. Evolutions of normal stresses in X-direction and Y-direction at the center of embedded stress sensor chip during the drop impact test.

procedure of the commercial software Abaqus 6.12 was used for the drop impact simulation. The element C3D8 was used for the dynamic explicit simulation.

The anisotropic material properties of the drop impact test board were considered in the model. The rate-dependent elastic-plastic material properties of solder bumps were taken into consideration [18]. The yield stresses of the SAC 305 under the strain rates 0.5, 1, 50, 100, 200, and 300 are 73, 77, 109, 124, and 130 MPa, respectively. And, the copper has the elastic-plastic behavior. The yield stress of copper was assumed as 120 MPa. Bilinear plastic model was used and the tangent modulus was assumed as 11 000 MPa. The other materials in the embedded package model were assumed to have the linear elastic properties. The material properties used for the model are listed in Table II.

In order to validate the developed drop impact model, the stress behaviors at the center of sensor chip from the numerical simulation results were compared with those from the drop experimental results. The Avexx shock tester instrumented with an accelerometer was used for drop impact test. The height and pressure of the Avexx System was varied until the accelerometer attached onto the drop table detected a half sine shock pulse with an amplitude of 1500 g and width of 0.5 ms. The acceleration pulses from different drop impact test boards are shown in Fig. 5. It can be seen that the acceleration pulse amplitudes are ~1500 g and the widths are 0.5 ms. The acceleration pulse applied at the bolt-holes of the test board in the simulation is also shown in Fig. 5.

The displacement evolutions of the different positions (position A is located at the bolt-hole, position B is located at the center of test board, and position C is located at edge of test board) of the drop test board are shown in Fig. 6. It can be seen that the deflection of the center and edge of test board is cycling under the drop impact loading. The deflection at the bolt-hole position becomes constant after 0.5 ms.

During the drop impact tests, the signals from the stress sensor at the center of embedded chip were monitored. The stress monitoring results during the drop impact tests are shown in Fig. 7. It can be found that the normal stress σ_{11} along the X-direction is much higher than the normal stress σ_{22} along the Y-direction, which is due to that the deflection along the longitude direction of the drop test board is higher than that in width direction. The maximum normal stress σ_{11} at the center of embedded chip occurs during the first deflection cycle. The normal stresses reduce with time due to the dumping effects of the drop impact system.

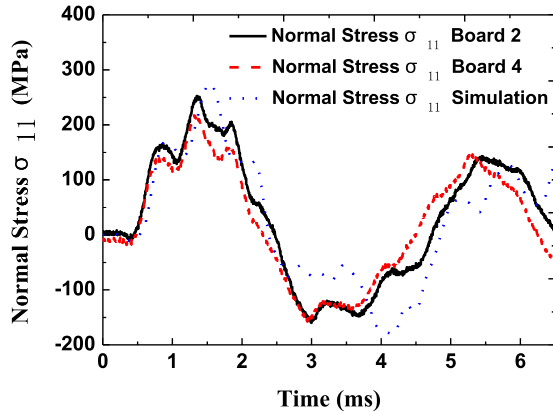

Fig. 8. Evolutions of the normal stresses in X-direction at the center of stress sensor chip embedded with underfill from the experiment and numerical simulation results.

The normal stresses σ_{11} at the center of embedded ultra-thin stress sensor chip from both experiment and simulation are compared in Fig. 8. The maximum normal stress σ_{11} from the simulation is ~276 MPa and the maximum normal stresses σ_{11} from the experimental test board 2 and 4 are ~251 and 217 MPa, respectively. The difference between the experimental stress curves of test board 2 and 4 might be due to the defects such as small voids and delamination induced by the fabrication processes. Therefore, by compared of the maximum normal stress σ_{11} from simulation result with experimental results of board 2 and 4, the discrepancies were found to be within 9.96% and 27.1%, respectively.

The normal stress σ_{11} evolution curve from the simulation is fitted the experiment results quite well before 2.5 ms. However, there are some discrepancies from 2.5 to 4 ms. The sources of the discrepancies may be due to the damping factor used in the simulation model is not the same as the experiment. The rate-dependent material properties of the other materials, such as copper, underfill, PCB may also contribute to the discrepancies. Based on this drop impact model, the parametric studies can be conducted to optimize the material selections and structural designs for the embedded ultrathin thin device in the organic substrate packaging.

IV. Parametric Study

In order to investigate the effects of material properties and structural parameters on the stress level of embedded ultrathin chip and reliability of solder bumps, different material properties and structural parameters were selected for the parametric study. The range of the material properties and structural parameters used for the parametric study are listed in Table III. The elastic modulus of underfill, thickness of PCB, standoff of solder bump, and thickness of embedded chip was selected as the factors. Three levels of each factor were considered in the parametric study. The basic case was defined for the parametric study in order to vary different structural and material property parameters. The structural parameters of basic case are: thickness of PCB 1 mm, standoff of solder ball 40 μm, and thickness of embedded chip 50 μm. The elastic modulus of underfill of basic case is chosen as 6 GPa.

TABLE III
Factors and Levels of the Material Properties and Structural Parameters for the Parametric Study

Factors	Levels		
Elastic modulus of underfill	1 GPa	6 GPa	15 GPa
Thickness of PCB	0.5 mm	1 mm	2 mm
Standoff of solder bump	40 µm	80 µm	120 µm
Thickness of embedded chip	50 µm	100 µm	200 µm

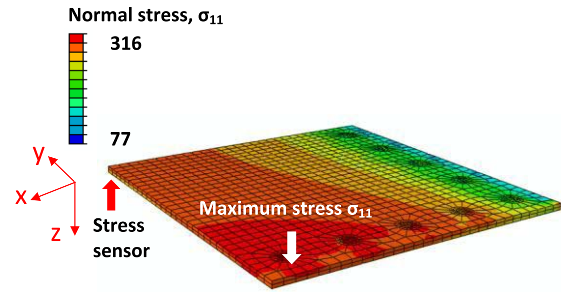

Fig. 9. Distribution of normal stress in X-direction of embedded stress sensor chip after 1.5 ms of drop impact test.

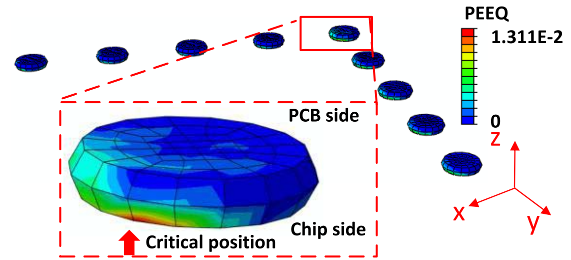

Fig. 10. Equivalent plastic strain distribution of the solder bumps embedded with underfill after 6.5 ms of drop impact test.

Under the drop impact loading two issues must be considered for the embedded ultrathin device in the organic substrate. The first one is the stress level on the embedded ultrathin chip, which might cause the cracking failure. The second one is the reliability of solder bumps. The plastic strain might be induced under the drop impact loading, which can cause the fracture failure.

Fig. 9 shows the normal stress σ_{11} distribution of the embedded stress sensor chip after 1.5 ms of drop impact test. It can be found that the maximum normal stress σ_{11} locates at the edge of chip surface opposite to the stress sensor side. The maximum normal stress σ_{11} at the chip edge of 316 MPa is higher than that at the center of chip surface on the stress sensor side which is 276 MPa.

In order to reduce the complication of simulation task, only 6.5-ms step time was applied to the simulation model. Fig. 10 shows the equivalent plastic strain distribution after 6.5 ms of drop impact test of solder bumps in the package embedded with underfill. It can be found that the critical solder bump located at the diagonal corner of the solder bumps array. The maximum plastic strain happens to the chip side of the critical solder bump. The maximum equivalent plastic strain of the critical solder bump after 6.5-ms drop impact test is 1.311%.

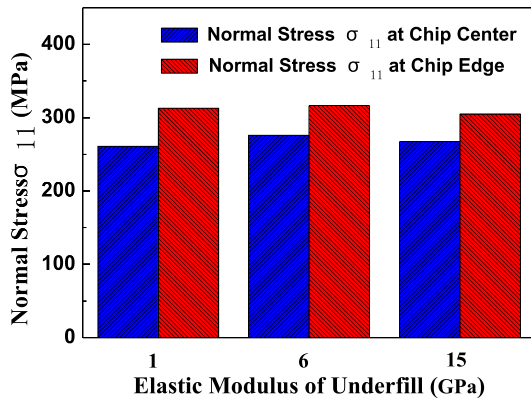

Fig. 11. Effects of underfill elastic modulus on the normal stress in X-direction at the center and edge of embedded stress sensor chip.

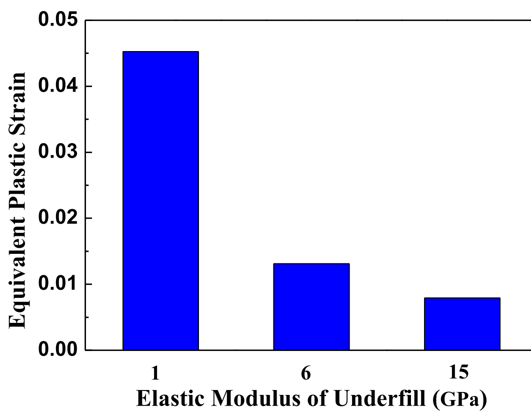

Fig. 12. Effects of underfill elastic modulus on the equivalent plastic strain of solder bump.

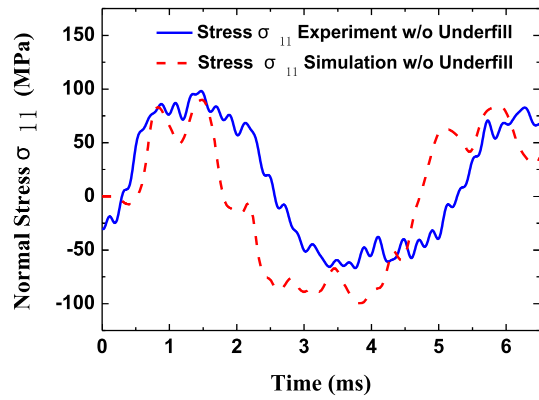

Fig. 13. Evolutions of normal stresses in X-direction at the center of stress sensor chip embedded without underfill from the experiment and simulation results.

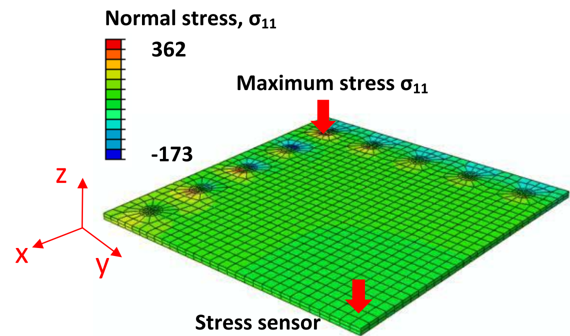

Fig. 14. Distribution of normal stress in X-direction of embedded stress sensor chip after 1.5 ms of drop impact test of the case embedded without underfill.

In order to make the comparison and optimization for the parametric study, the maximum normal stresses σ_{11} at the center and edge of the embedded stress sensor chip and the maximum equivalent plastic strain of solder bump after 6.5-ms drop impact test were selected as the indexes.

V. Results and Discussion

The effects of elastic modulus of underfill on the stress level of embedded thin chip and the equivalent plastic strain of solder bump are shown in Figs. 11 and 12, respectively. It can be found that the effects of elastic modulus on the stress level of embedded chip are limited. The maximum equivalent plastic strain of the solder bump decreases from 4.53% to 0.79% when the elastic modulus of underfill increases from 1 to 15 GPa. The underfill with higher elastic modulus provides a good protection to solder bump under the drop impact loading. However, the elastic modulus of underfill does not affect much on the stress level of embedded ultrathin chip. Therefore, in order to increase the reliability of solder bump, underfill with higher elastic modulus is recommended.

Fig. 13 shows the evolutions of normal stresses σ_{11} at the center of stress sensor chip embedded without underfill from the experimental and simulation results. It can be seen that the simulated stress evolution is consistent with the experimental result, which also provides a validation of the simulation model. It also indicates that the normal stress σ_{11} of 85 MPa at the center of stress sensor chip embedded without underfill is much lower than that embedded with underfill which is 251 MPa (experimental results).

Fig. 14 shows the normal stress σ_{11} distribution of embedded stress sensor chip of the case embedded without underfill after 1.5 ms of drop impact test. It can be found that the maximum normal stress σ_{11} occurs at the diagonal corner edge of chip surface on the stress sensor side, which is different to the case with underfill, as shown in Fig. 9. The locations of the maximum normal stress σ_{11} happening on the embedded ultrathin chip are different of the cases embedded with and without underfill.

Figs. 15 and 16 show the effects of underfill on the stress level of embedded chip and the equivalent plastic strain of solder bump (simulation results). It can be found that the maximum normal stress σ_{11} at the center of embedded chip reduces dramatically from 276 to 83 MPa when no underfill was used for embedding, which is consistent to the stress sensor monitoring result. However, the maximum normal stress σ_{11} located at the edge of embedded chip increases form 316 to 362 MPa. As shown in Fig. 16, the maximum equivalent plastic strain of solder bump increases dramatically from 1.31% to 22.7%. Therefore, underfill is required for

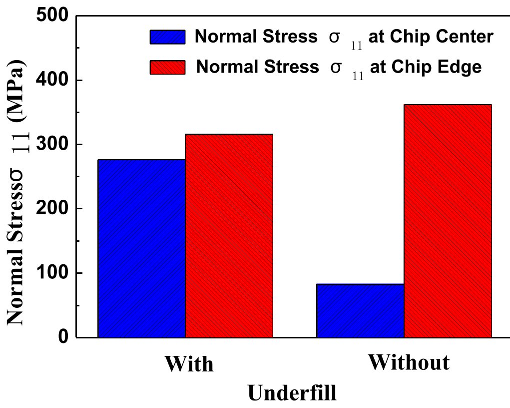

Fig. 15. Effects of underfill on the normal stress in X-direction at the center and edge of embedded stress sensor chip.

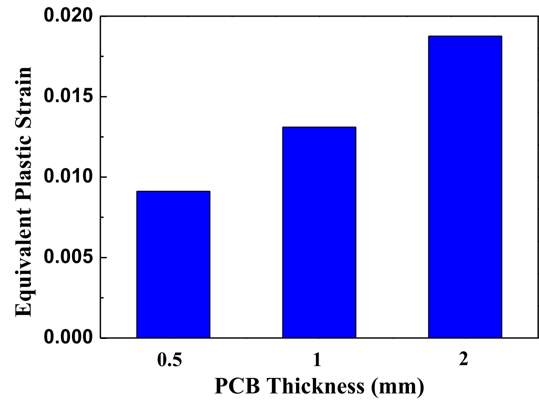

Fig. 18. Effects of PCB thickness on the equivalent plastic strain of solder bump.

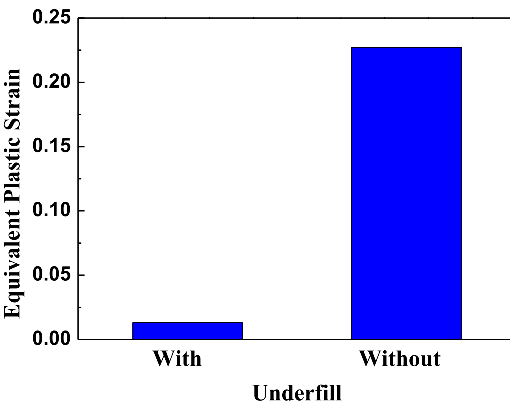

Fig. 16. Effects of underfill on the equivalent plastic strain of solder bump.

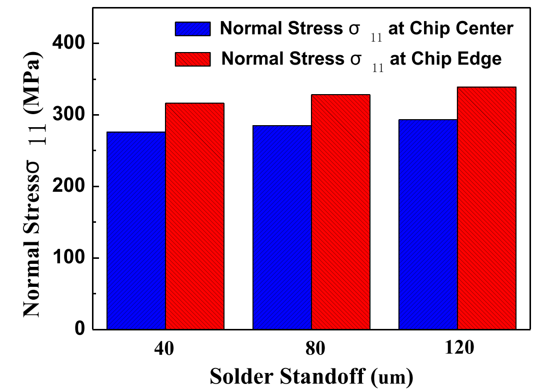

Fig. 19. Effects of solder bump standoff on the normal stress in X-direction at the center and edge of embedded stress sensor chip.

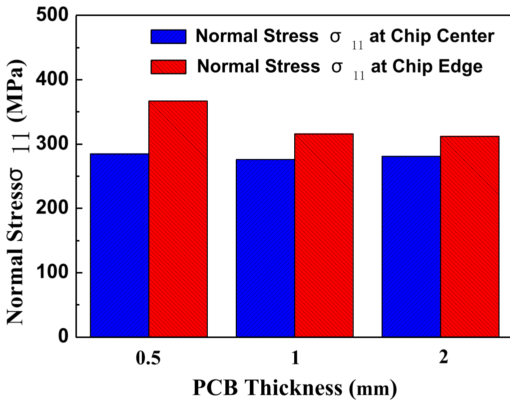

Fig. 17. Effects of PCB thickness on the normal stress in X-direction at the center and edge of embedded stress sensor chip.

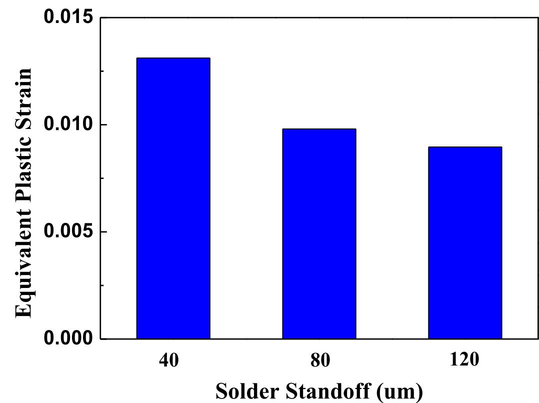

Fig. 20. Effects of solder bump standoff on the equivalent plastic strain of solder bump.

enhancing the reliability of solder bumps of the embedded packaging under the drop impact loading.

The effects of PCB thickness on the stress level of embedded chip and the equivalent plastic strain of solder bump are shown in Figs. 17 and 18, respectively. It can be seen that the normal stress σ_{11} at the edge of embedded chip reduces from 367 to 312 MPa when the thickness of PCB increases from 0.5 to 2 mm. The effects of PCB thickness on the normal stress σ_{11} at the center of embedded chip are limited. However, the maximum equivalent plastic strain of solder bumps increases from 0.9% to 1.88% when the thickness of PCB increases from 0.5 to 2 mm.

Figs. 19 and 20 show the effects of solder bump standoff on the stress level of embedded chip and the equivalent plastic strain of solder bump. It shows that the effects of solder bump standoff on the stress level of embedded chip are limited. The normal stress σ_{11} at the edge of embedded stress sensor chip increase slightly from 316 to 339 MPa with increasing

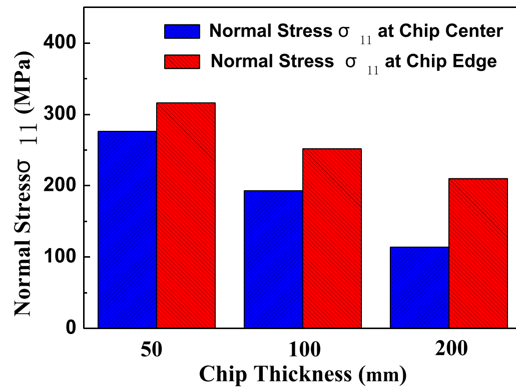

Fig. 21. Effects of embedded chip thickness on the normal stress in X-direction at the center and edge of embedded stress sensor chip.

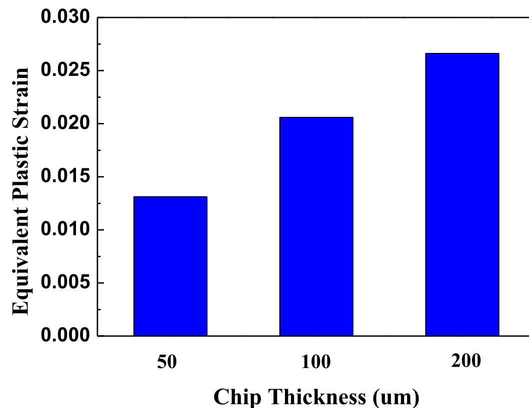

Fig. 22. Effects of embedded chip thickness on the equivalent plastic strain of solder bump.

of solder bump standoff from 40 to 120 μm. However, the maximum equivalent plastic strain of solder bump decreases from 1.31% to 0.89% when the solder bump standoff increases from 40 to 120 μm.

The effects of embedded chip thickness on the stress level of embedded chip and the equivalent plastic strain of solder bump are shown in Figs. 21 and 22, respectively. It can be found that the maximum normal stress at the edge of embedded chip increases dramatically from 210 to 316 MPa when the chip thickness reduces from 200 to 50 μm. The normal stress at the center of embedded chip also increases from 144 to 276 MPa when reducing of chip thickness. Therefore, the stress control of the embedded ultrathin chip is critical. The increasing of chip thickness can help to reduce the stress level of embedded chip. However, it is harmful to the reliability of solder bumps. As shown in Fig. 22, the maximum equivalent plastic strain of solder bump increases from 1.31% to 2.66% when the embedded chip thickness increases from 50 to 200 μm.

VI. Conclusion

In this paper, drop impact tests were conducted to the embedded ultrathin stress sensor chip in the organic board. The stresses were monitored with the embedded stress sensor chip under the drop impact loading. Dynamic explicit finite element model was built up to investigate the stress and strain behaviors of the ultrathin chip and solder bumps. Parametric studies were also conducted to predict the effects of material properties and structural parameters. Some key results were summarized as follows.

1) The drop impact simulation model was validated by the stress monitoring results. The discrepancy of the maximum normal stress σ_{11} at the center of embedded stress sensor chip from experimental and simulation results could be within 30%.
2) The underfill with higher elastic modulus can provide a protection to solder bumps. Embedded without underfill will increase the stress level of embedded chip and also induce dramatic plastic strain to solder bumps.
3) Increasing PCB thickness can help to reduce the stress level of embedded ultrathin chip. However, it is harmful to the reliability of solder bump.
4) The effects of solder bump standoff on the stress level of embedded chip are limited. The reliability of solder bump can be enhanced when solder bump standoff increases.
5) The maximum normal stress σ_{11} on the embedded chip decreases dramatically with increasing of chip thickness. However, the equivalent plastic strain of solder bump increases by $\sim$2 times when the embedded chip thickness increases from 50 to 200 μm.

Acknowledgment

The authors are thankful for the experimental support works from the stuff R. Rajoo, C. S. Selvanayagam *et al.* in Institute of Microelectronics, A*STAR, Singapore.

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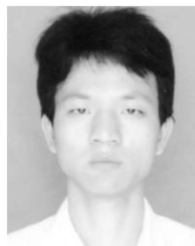

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