Cu/Dielectric hybrid bonding among Glass and Si

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***Abstract*— Chaplets and advanced packaging technologies play a pivotal role in meeting the diverse and demanding requirements of data-intensive workloads, by offering solutions that encompass performance, power efficiency, form factor, and cost-effectiveness. These package architectures demand a higher interconnect density among chiplet's to package substrate. Conventional organic and ceramic substrates are more apparent in scaling the electrical wire, due to signal integrity, radiality, and manufacturing challenges. Glass substrates are becoming a prominent replacement for conventional package substrates due to their high thermal, and mechanical stability with ultra-low surface flatness. In this endeavor, a fine-pitch (~6 µm) Cu/dielectric hybrid bonding process among glass to silicon substrates has been demonstrated at a low temperature of ~⩽ 250 ° C, with N_2 plasma treatment. The detailed investigation of the selection of glass substrates and challenges associated with processing it in the process line. The surface inspection resulted in an oxide surface roughness to be <0.3nm and Cu dishing controlled to < 5nm on both glass and silicon wafers fabricated with optimized process control. Furthermore, 90% void-free bonding was observed using interface acoustic imaging (C-SAM) and Cu-Cu grain growth was observed by cross-sectional FIB-SEM inspection. These investigations are expected to benefit future trends in advanced packaging with glass substrates.**

Keywords—Glass substrates, hybrid bonding, Fine-pitch.

I. INTRODUCTION

Over the years, technological advancements have enabled the transformation of large computational systems into portable handheld devices [1]. This shift has been facilitated by the reduction in the size of transistors on a single electronic chip within computational systems, commonly known as systems on a chip (SOCs) [2]. While traditional SOCs have offered a more compact and cost-effective solution with increased computing capacity as scaling has progressed, they are now approaching physical dimensional scaling limits. The extreme dimensional scaling has led to process complexity and increased RC delay, making it less than ideal for heterogeneous integration. Despite these challenges, contemporary applications such as artificial intelligence (AI) and the Internet of Things (IoT) require computational systems that boast high performance, a small footprint, and integration with diverse functionalities [3-5]. Meeting these demands is steering the electronics industry toward advanced packaging solutions.

Three-dimensional heterogeneous integration (3D HI) technology is gaining increased appeal for the next generation of electronic packaging [6-8]. It offers flexibility in multifunctional integration, decreases RC delay using TSV interconnects, and can minimize the footprint through vertical integration. Moreover, there is a growing need for higher I/O density to enhance the performance of applications such as 3D high bandwidth memory stacks (HBM) and CMOS-backside illumination (BSI) sensors [9]. The utilization of Cu/dielectric hybrid bonding is emerging as a crucial factor in achieving greater interconnect density within stacked dies. In addition, the interconnect scaling requirement is also critical among the stacked dies to package substrate [10]. However, the conventional ceramic or orgonic packages suffer from poor thermal mismatch, limiting interconnect density, poor electrical performance for high-speed and high-frequency applications, and do not support compact form factors for advanced HI [11]. In addition, these substrates have processing complexities with the back end of the line (BEOL) process line and show reliability issues due to the mismatch in the thermal expansion coefficients of various materials incorporated on it, and not a cost-effective material. To overcome these limitations, researchers and engineers are exploring new package substrate materials,

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advanced packaging techniques, and innovative design approaches that can better accommodate the demands of heterogeneous integration.

On the other hand, compared to the organic substrates now in use, glass substrates have superior mechanical, physical, and optical qualities that enable the assembly of larger chiplet complexes (referred to as "system-in-package") and greater scalability. Furthermore, glass substrates are more attractive due to their manufacturability with tunable CTE, profoundly flat and smooth/lower surface roughness to sub-nm, excellent chemical durability, low total thickness variation (TTV), and warpage properties. In addition, Glass substrates have the dimensional stability required for highly tight layer-to-layer interconnect overlay, as well as the ability to withstand higher temperatures and provide 50% less pattern distortion and ultra-low flatness to enhance depth of focus in lithography [12,13]. These distinctive features enable a 10x enhancement of interconnect density on glass substrates [14]. Furthermore, ultra-large form-factor packages with extremely high assembly yields are made possible by glass's superior mechanical qualities [15]. Along with this, glass become the major substrate in the packaging field, as interposers and RF fields due to its low electrical and coupling losses [16]. However, glass wafer processing in conventional cleanroom fabrication facilities and fabricating the fine-pitch interconnect nodes remain unexplored.

In such aspect, this paper demonstrates the glass wafer processing in BEOL fabrication line with its associated challenges and fabricating a fine pitch (~6 µm) pitch Cu/dielectric surface on glass using the damascene process has discussed in detail. Following, a wafer-level fine-pitch (~6 µm) bonding process between the glass to silicon has been demonstrated. Various surface characterizations before bonding and interface characterizations after bonding have been investigated and are discussed in detail in the following sections.

II. Experimental Protocol and Challenges Associated with Glass Wafer Processing.

The 300 mm process line toolset has been utilized in the entire experimental demonstration. A 300 mm diameter, p-type (100) silicon and glass wafers with double-sided polished substrates have been used for processing. The glass wafers with compatible coefficient of thermal expansion (CTE) with Si have been procured from Corning Inc. Before processing these glass wafers an efficient cleaning is required as discussed in II.A. Fig. 1(a to f) shows the schematic of the damascene process sequence for creating bond Cu/dielectric surface on both silicon and glass substrates. Before the glass wafer processing an opaque layer has been deposited at the back side. Afterward, the dielectric layer deposition using the PECVD process with, PR coating, and development using SUSS track and exposure using ULTRATECH stepper tools. The stepper mask has been designed with a 6 µm pitch with a 3 µm pad size. Following, the Inductively coupled plasma (ICP) etch tool was used for dielectric layers etching, and an in-house PR stripper for PR removal on the dielectric. Afterward, the PVD process was utilized for depositing the barrier and Cu seed layer respectively, and electrochemical plating/deposition was done using the ECD tool. The resulting Cu overburden followed by barrier layer removal has been removed by polishing with the CMP tool with endpoint detection. After obtaining the required surface, the bonding process with precise alignment was carried out using the EVG Gemini FB XT tool. Fig 1(g and h) shows the wafer-to-wafer hybrid bonding process. The bonded wafers are annealed at high temperatures to enhance the dielectric bond strength and make the Cu-Cu interconnections.

As the glass substrates have lower Yong's modulus as compared with silicon, its investigation in terms of warpage is necessary after each process step, due to wafer handling systems being highly warpage dependent. Maintaining the warpage to the minimum acceptable level is more important. Towards its measurement, FSM 128L has been utilized. Following, the

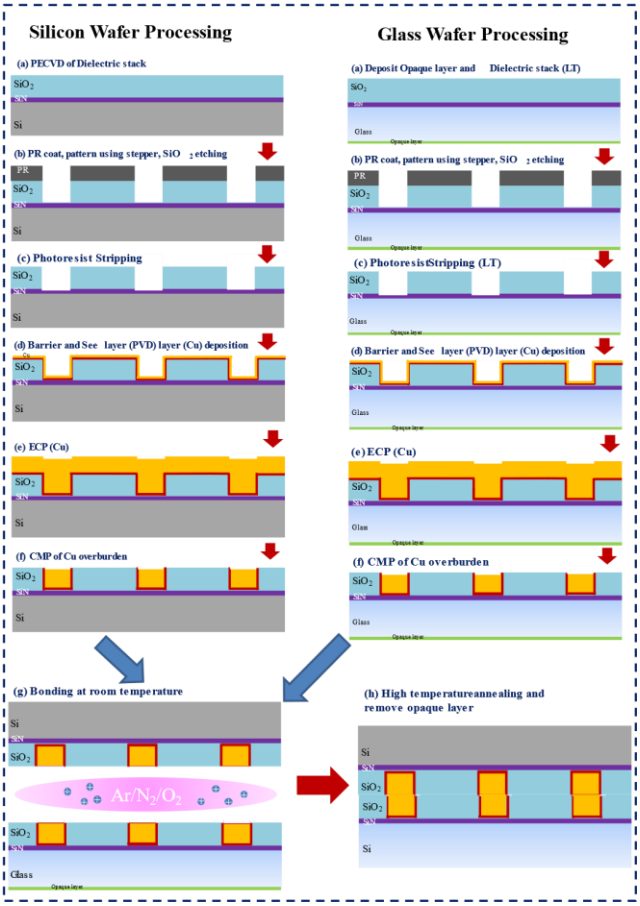

Fig. 1. Schematic of damascene process fabrication on silicon and glass wafers for fine pitch hybrid bonding.

surface roughness and Cu to oxide dishing is the major requirement for hybrid bonding, in such aspect, a fully automated inline atomic force microscopy (AFM) – InSightAFP by Bruker, has been utilized. Afterward, for interface inspection, a c-mode acoustic microscopy for wafer level voids and bonding interface quality a focused ion beam scanning electron microscopy (FIB-SEM) was used.

A. *Challenges associated with working glass wafers.*

- The majority of silicon wafer process tools cannot detect transparent substrates in the BEOL clean room process line, thereby necessitating the deposition of an opaque layer for tool accessibility.

- The thorough investigation of glass properties such as warpage and total thickness variation (TTV) on bare glass substrates, along with deposition layers incorporating optical/laser transparent layers, is crucial to eliminate the need for opaque layers and enhance equipment compatibility.
- Efficient cleaning procedures for glass wafers are imperative, as inadequate cleaning has been associated with increased voids at the bonding interface.
- Warpage compensation strategies must be carefully executed to facilitate uninterrupted processing of glass wafers, especially considering their lower Young's modulus (73.6 GPa, less than half of silicon's Young's modulus). [17].
- Effective solutions are required to enable the processing of wafers in high-power plasma chambers, such as those used in dry etching.
- Wafers with greater bow/warpage margins may be necessary when working with glass substrates.
- Optimal process control is essential for maintaining critical dimensions of features while processing wafers in high-power plasma chambers.

III. Results and Discussion

A. *Cleanliness of the glass wafer surface using blanket-bonded glass to silicon wafers.*

The Void-free bonding is necessary for the high electrical and mechanical reliability of stacked wafers. The voids at the bonding interface could be formed by either chemical (precursor outgassing from dielectrics or gaseous byproducts while condensation reaction while bond formation) or physical voids (particles, trapped air while bonding wave propagation or surface nonuniformities). The presence of the contaminants on the glass surface may lead to the surface adhesion of the following process layers. It suggests an appropriate study on the cleanliness of the glass surface, even though the proposed hybrid bonding process could be performed among the oxide dielectrics. A direct bonding process with blank Si wafers has been implemented to check the cleanliness of the glass surface following interface C-SAM inspections before and after annealing.

Fig. 2(a) and 2(b) show the C-SAM image of the direct bonding of glass and Si without external cleaning of glass, except for the plasma and DIW rinse before and after annealing, respectively. Similarly, Fig 2 (c, d) for cleaning protocol-1 and Fig 2 (e, f) for cleaning protocol-2. As there were no interlayers at the bonding interface, and no new void formation after high-temperature annealing could suggest a negligible chemical void. The physical voids are the main reason for the void formation at the bonding interface if the glass wafers cannot be cleaned. These physical voids might be either organic contaminants or surface adsorbed particles...etc. need to be further investigated. However, the wafers treated with better chemical protocol resulted in a well-bonded interface without

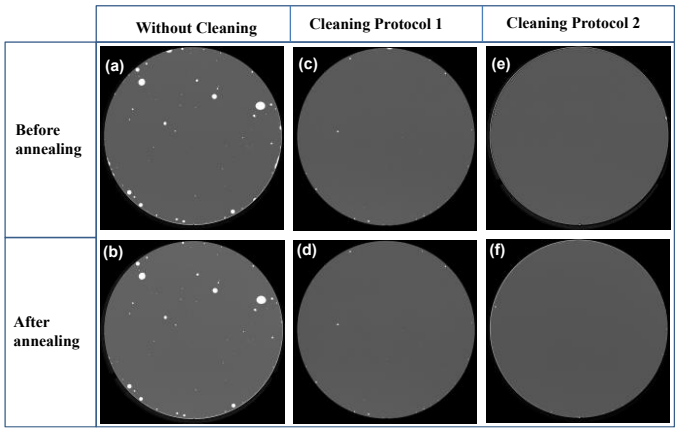

Fig. 2. C-SAM inspection of blanket bonding interface of glass and silicon before and after annealing at, (a,b) without cleaning. (c,d) with cleaning protocol-1. (e,f) with cleaning protocol-2.

interface voids. It suggests a well-cleaning protocol is necessary on glass wafers before processing them for any other deposition processes.

B. *Bow control for glass wafers in the damascene process.*

Most of the current tools are set with a bow/warpage margin for silicon wafer handling. The bow/warpage of the wafers directly depends on the elastic modulus of the materials. As, the glass materials have lower elastic modulus compared with Si, the bow/warpage change could be higher as compared with the Si, while a similar process has been performed. While executing all the process fabrication, we make sure the warpage is under control as shown in Fig. 3, by utilizing the appropriate compensation mechanism.

C. *Surface preparation for hybrid bonding.*

Surface morphology is a key requirement for hybrid bonding. As the bonding among the dielectrics is to be formed **in the first place, metal dishing is adequate for the wafers. The** quantification of these requirements of surface roughness and dishing has been inspected using the automated 3D AFM. The optimized CMP process used to control the dishing of Cu to oxide of < 5nm on the glass surface and 5nm±3nm on the

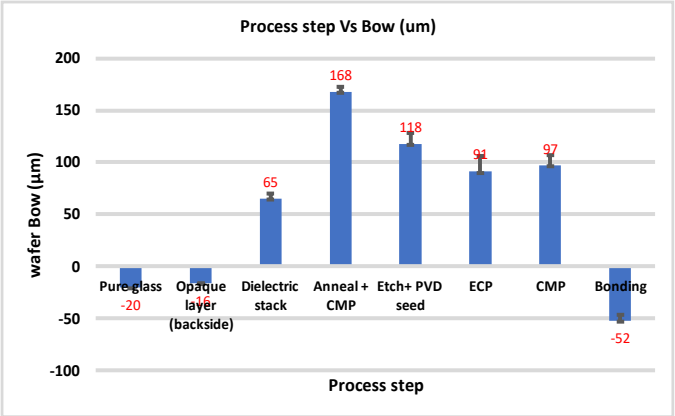

Fig. 3. Wafer bow variation with respect to each process fabrication process step.

silicon surface as shown in Fig. 4. In addition, the roughness on the dielectric surface has been maintained to < 0.2nm on both glass and silicon wafers. With the help of optimization in the CMP process, the corner rounding.

D. Bonding Interface inspection.

A void-free bonding is necessary for reliable interconnects. The wafers with optimized dishing and controlled surface roughness are bonded using the N_2 plasma activation followed by water rinsing and with appropriate alignment at room temperature. The wafer surface after the opaque layer removal at the backside of glass in Fig 5 (a), and observation of bonded interface with the naked eye after bonding with Si in Fig 5(b). The bonding interface after bonding has been inspected using the C-SAM nondestructive method. It resulted in no voids at the bonding interface except at the systematic design voids as shown in Fig 5(c). However, void-free interface even at the systematic design areas has been observed after post-bond annealing of 250 °C, 2hr as shown in Fig 5(d).

Furthermore, inspecting the misalignment across the glass to Si bonded interface is very facile. It didn't necessitate high-end IR sources like in inspecting the conventional Si-Si bonding interface. An optical method is sufficient to inspect the alignment accuracy across the glass-to-silicon bonding interface. Fig 6(a) shows the bonding interface from the top of the glass surface across the water from the center and four edges around the wafer as mentioned in the respective figure. In addition, the overlay map across the wafer using the EVG overlay tool is shown in Fig. 6(b). The resulting overlay of a maximum of ~1.5um is expected from the stepper alignment accuracy observed at the edge of wafers, however, the accuracy is ~<50nm at the center locations.

Furthermore, the interface inspection using the X-SEM after dicing into 5mmX5mm, as shown in Fig. 6(c). The interface with no interface voids across the Cu pads suggested that process control across all the processes could help achieve the

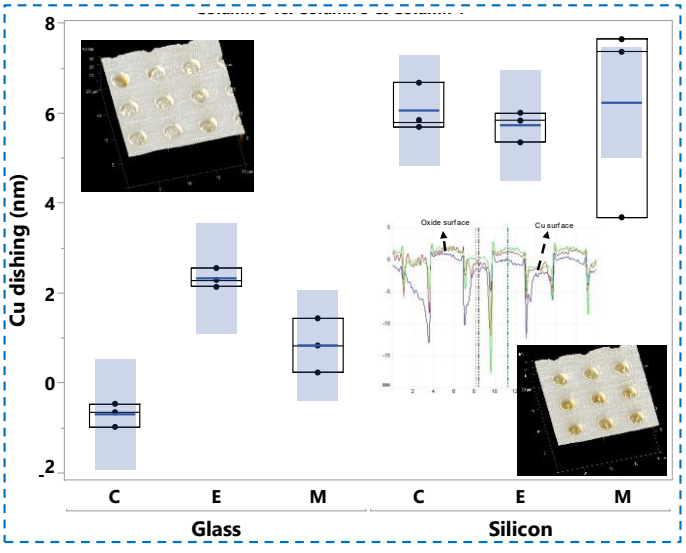

Fig. 4. AFM inspection of Cu dishing at wafer center (C), Middle (M), and Edge (E), on the surface of glass and silicon substrates.

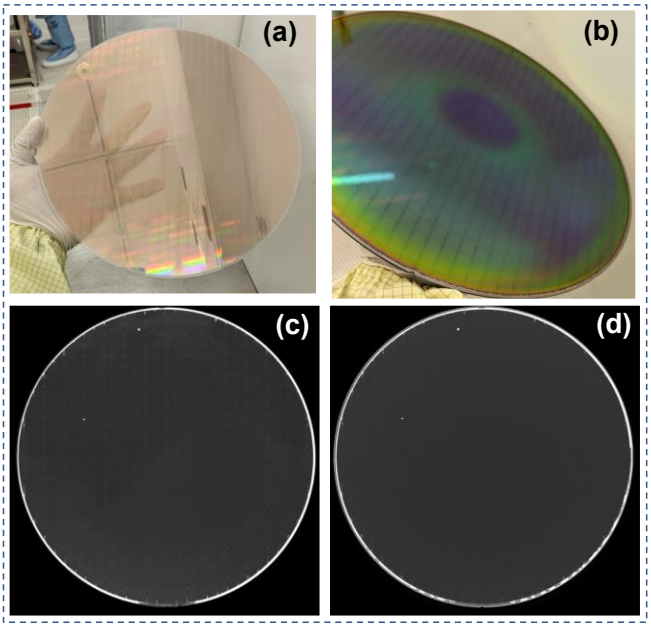

Fig. 5. (a). Glass wafer with no opaque layer with damascene Cu/dielectric surface. (b). Cu/dielectric hybrid bonding among glass and Si. C-SAM interface inspection (c) after bonding, (d) after annealing.

higher reliable interconnects. There was observed an increased pattern size on the glass wafers. It might be due to the efficient path of heat transmitted from the glass substrate to the electrostatic chuck (ESC) used in the etch chamber. In addition, The EDS line scan across the metal pads confirms the continuous Cu elemental at the bonding interface suggesting a reliable interconnect across the glass and Si hybrid bonding.

IV. Conclusion

Glass-to-Si hybrid bonding has been demonstrated successfully at a 6 µm bonding pitch. Challenges associated with glass wafer handling have been explained. The bow control has maintained all tool acceptable limits while executing the damascene process on glass wafers by utilizing the compensation layers. It was observed an efficient cleaning is necessary for glass wafers to get void-free bonding and optimized the cleaning protocol. In addition, minimal dishing has been achieved on both glass silicon wafers for void-free bonding. The reliable interconnect has been achieved even at the thermal budgets of ≤ 250 ˚C, 2hr of post-bond annealing. These investigations will help for future glass substrate integration in future high-performance electric packages.

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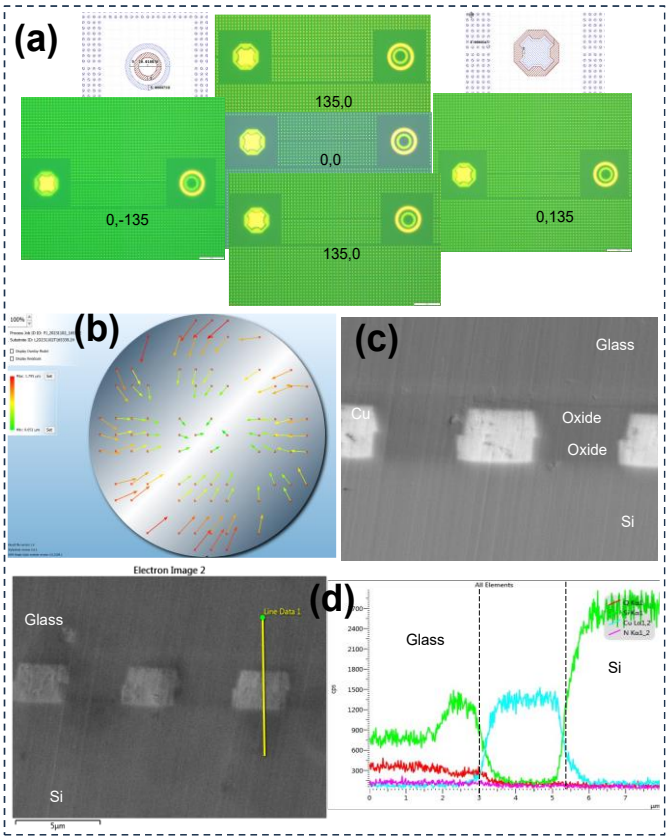

Fig. 6. (a). Optical inspection of alignment of wafers due to its optical transparency. (b). The overlay map was measured using the EVG IR alignment verification tool. (c)The X-SEM of Interface of bonded interface. (d). the line scan and respective elemental map using EDS detection.

C2W applications). The authors also thank A*STAR and the IME-Fab Operations team for their support in development and fabrication.

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