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Near-Threshold Energy and Area Efficient Reconfigurable DWPT/DWT Processor for Healthcare Monitoring Applications

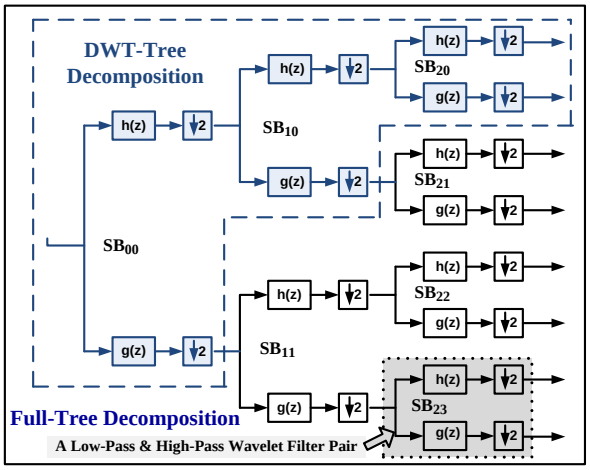
Chao Wang, Jun Zhou, Lei Liao, Jingjing Lan, Jianwen Luo, Xin Liu, and Minkyu Je

***Abstract*—This paper presents an energy and area efficient discrete wavelet packet transform processor (DWPT) design for power-constrained and cost-sensitive healthcare monitoring applications. This DWPT processor employs recursive memory-shared architecture to achieve low hardware complexity while performing required arbitrary-basis DWPT decomposition. By exploiting inherent characteristics of different physiological signals through an entropy statistic engine, the DWPT processor core can be reconfigured to compute multi-level wavelet decomposition with effective time and frequency resolution. Various design techniques from algorithm to circuit levels, including reconfigurable computing, lifting scheme, dual-port pipeline processing, near-threshold operation, and clock gating, are applied to achieve energy efficiency. With a 0.18-µm CMOS technology, at 0.5 V and 1 MHz, the DWPT core only consumes 26 µW for performing 3-level 256-point DWPT decomposition with entropy statistic calculation. When integrated in an ARM Cortex-M0 based biomedical SoC test platform, the DWPT processor achieves processing acceleration by three orders of magnitude and reduces energy consumption by four orders of magnitude compared to CPU-only implementations.**

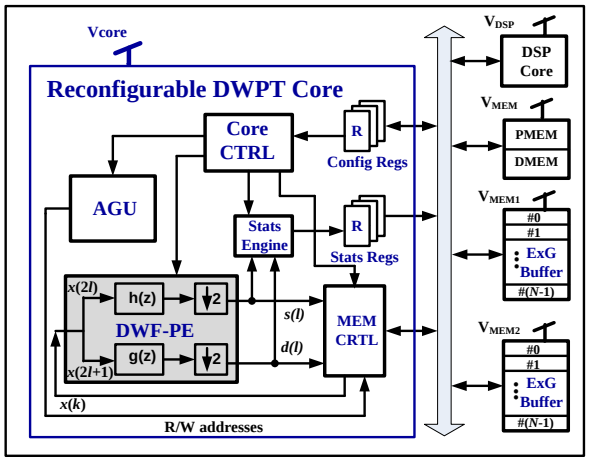
***Index Terms*—DWPT, DWT, Near-Threshold Operation, Reconfigurable Computing, Healthcare Monitoring**

I. Introduction

Driven by advances in medical sensors and CMOS circuits, health sensing and monitoring devices have emerged in biomedical applications. Recently, advanced healthcare sensor nodes adopt low-power DSP/CPU cores and hardware accelerators to integrate more monitoring functions and achieve optimum performance [1-4]. However, this trend imposes even more stringent constraints on power consumption, size, and cost, because the required more advanced signal processing such as digital filtering, discrete transforms, etc. Specifically, due to better time-frequency resolution and energy-compactness features, discrete wavelet transform (DWT) [5] has been adopted and implemented in recent healthcare sensors to perform front-end denoising, event detection, and data compression [11-13]. However, there are several issues for stringent power-constrained, size-limited, and cost-sensitive healthcare monitoring applications. First of all, the designs in [11-13] only implement a DWT dedicated for a specific physiological application, e.g. the ECG detection in [12]. So these DWT engines cannot be reused or are difficult to optimize for other physiological signal processing. Second, some of the prior works [11-13] haven't utilized latest effective techniques, such as lifting scheme and ultra-low-voltage operation, to implement or optimize their designs. Thus, the energy consumption and silicon area are not minimized. Third, the



(a)



(b)

Fig. 1. (a) Direct-mapping architecture, and (b) reconfigurable recursive architecture for multi-level DWPT.

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existing methods haven't addressed the boundary treatment issue in frame-based signal processing, or still use sample-based continuous processing method, which is likely to be redundant and not energy-efficient for long-term healthcare monitoring. At last, these engines can only perform DWT decomposition with a fixed time-frequency resolution.

As a generalization of DWT, discrete wavelet packet transform (DWPT) provides a much more flexible time and frequency decomposition and outperforms its subset DWT [5-10], but at the cost of significantly higher computation and complexity, as show in Fig.1 (a). It is very challenging to design efficient DWPT processor, and therefore there is almost no prior art reporting a DWPT processor design to our knowledge, especially for healthcare monitoring applications.

This brief present near-threshold reconfigurable DWPT processor design for DSP/CPU core based healthcare monitoring applications. Design methods and techniques are investigated and optimized from system level, algorithm level, architecture level, down to circuit level, to achieve area and energy efficiency. The proposed design can be reconfigured to perform multiple-level decomposition with best time-frequency basis. The near-threshold DWPT processor can achieve energy saving by orders of magnitude compared to the CPU-only implementation. As far as we know from the literature, this is the first reported near-threshold reconfigurable DWPT processor design for healthcare monitoring applications.

II. DWPT Architecture & Circuit Design

A. Reconfigurable DWPT Architecture

As illustrated in Fig. 1 (a), a *J*-level DWPT can be direct-mapped into a tree-structured filterbank [5], in which at each decomposition level, there are 2^j (j=0, 1, …, J – 1) low-pass and high-pass wavelet filter pairs, of which each decompose input signals in two subbands at the next level, also called subband (SB) filtering denoted by SBji (i=0, …, 2^j-1). The direct-mapping (DM) architecture [12-13] has a high hardware complexity of (2^J – 1) and J filter pairs, for J-level DWPT and DWT, respectively. In contrast to the fast pipeline architectures in [14-16], the recursive DWPT architecture is well suited for the emerging size-limited and cost-sensitive healthcare monitoring applications with sampling rates ranging from tens of Hz to tens of kHz. The folded pipeline architecture in [14-15] consumes significantly more hardware resources due to J filer pairs (PEs) required by J-level decomposition, and also suffers lower hardware utilization especially for the best-basis decomposition implemented by bypassing a few bands of signals through the rest subband filtering. These signals still have to stream through the PEs with other subbands of signals to be further decomposed due to the interleaving subband filtering, which will result in redundant data switching and energy consumption. By taking advantage of aggressive voltage scaling only on logic, the pipeline architecture may achieve much more energy saving than the memory-shared recursive architecture, but at the cost of significantly more silicon area. In this study, to achieve area and energy efficiency, the proposed reconfigurable DWPT processor adopts the single-PE recursive architecture to sequentially compute the multiple subband filtering at different levels with a single filter pair, consuming only about 33.3% of the logic gates by the pipeline architecture for 3-level DWPT, but with a hardware utilization close to 100%.

As depicted in Fig. 1 (b), the proposed recursive DWPT architecture consists of a reconfigurable DWPT core and shared memory banks. The reconfigurable DWPT core is comprised of a core controller, a register bank, an address generation unit (AGU), a statistic engine, and a discret wavelet filter processing element (DWF-PE). Configured through the register bank by a host (i.e., a DSP/CPU core), the DWPT core can be reused to utilize just one DWF-PE to compute multi-level decomposition on various physiological signals stored in the memory banks. By applying lifting scheme in wavelet filter design, the in-place implementation can reduce the memory requirement to buffer the intermediate data during the computation [14]. Dedicated AGU circuit is designed to provide correct memory R/W control for the data buffering.

Based on predefined scenarios or statistic information (i.e., entropy statistics) computed by the statistic engine, the DWPT core can be configured to perform multi-level decomposition with a best basis of time-frequency resolution suitable for different physiological signals [5-6]. The DWPT core is designed to operate in two major modes: (1). the full-tree DWPT decomposition mode with enabled statistic engine to collect real-time signal statistic information; (2). the best-basis DWPT decomposition mode with disabled statistic engine for only performing a specific-basis decomposition. Enabled by the reconfigurable core, reconfigurable DWPT computation can be employed for various physiological signal processing tasks, e.g., different physiological data compression, to achieve better compression efficiency [5-6]. To get the sparsest representation for a specific physiological signal, the DWPT core can be configured to the full-tree decomposition mode to compute entropy information for the best basis searching, either for only one time at the start of a specific physiology data compression, or a few times during the data compression to update the statistics regularly. The original data frame used for computing statistics by full decomposition must be stored in another frame buffer for final best-basis decomposition once the best basis is determined. With the best basis, the DWPT core will be configured into the best-basis mode to perform decomposition. In this way, the energy consumption can be saved by reducing redundant computation but at the same time best-basis data compression is achieved by the reconfigurable computation.

B. Lifting-Based Wavelet Filtering with Dual-Port Memory Access & Pipeline Processing

To minimize energy consumption, lifting-based wavelet filter design is utilized to reduce the dynamic power consumed by the required arithmetic operations. Compared with the convolution method used in [13], the lifting-based D4 (Daubechies-4) wavelet design [5] described by the equations in Fig 2 (a) reduces required multiplication and addition operations by 62.5% and 33.3%, respectively, which can result in significant

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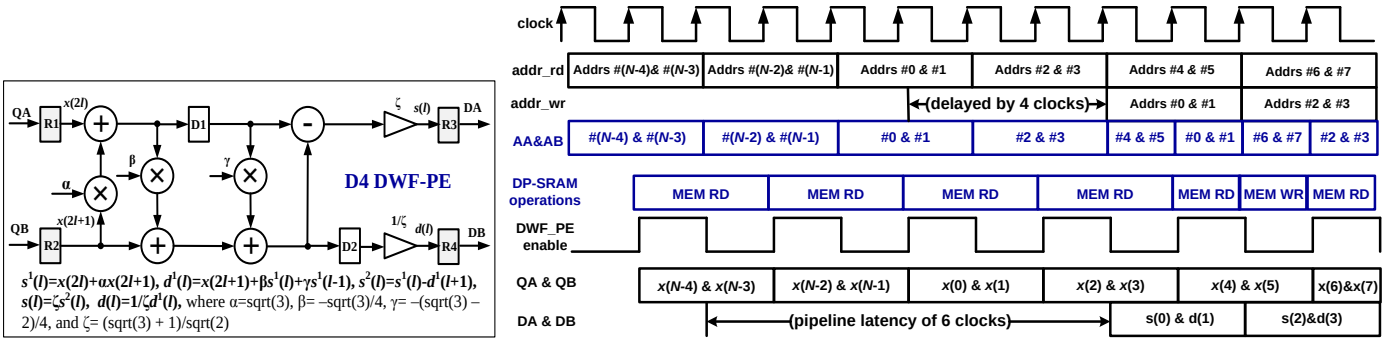

$s^1(l)=x(2l)+\alpha x(2l+1)$, $d^1(l)=x(2l+1)+\beta s^1(l)+\gamma s^1(l-1)$, $s^2(l)=s^1(l)-d^1(l+1)$, $s(l)=\zeta s^2(l)$, $d(l)=1/\zeta d^1(l)$, where α=sqrt(3), β= –sqrt(3)/4, γ= –(sqrt(3) – 2)/4, and ζ= (sqrt(3) + 1)/sqrt(2)

(a) (b)

Fig. 2. (a) Circuit diagram of the lifting-based D4 DWF-PE; (b) Pipeline timing diagram of DP-SRAM access and D4 DWT-PE processing at the start of a subband filtering.

energy saving. To enable efficient pipeline processing and in-place memory access, the direct-mapping circuit of the lifting-based D4 wavelet filter as shown in Fig. 2 (a) can be used in the proposed architecture as the DWF-PE to interact with a Dual-Port SRAM (DP-SRAM) based frame buffer. Fig. 2 (b) describes the pipeline processing of two-port memory read/write operations and D4 wavelet filtering.

As shown in Fig. 2 (b), the overall pipelining latency is six clock cycles contributed by the R/W pipeline registers and two internal filter delay registers. Interleaving memory access mechanism is employed to interleave one pair of read operations with another pair of subsequent write operations to avoid R/W conflicts and maximize the hardware utilization, as illustrated in Fig. 2 (b). For each subband filtering, the utilization of the DP-SRAM bandwidth and DWF-PE is up to 100%. The processing throughput is one wavelet coefficient per clock cycle in average for every D4 wavelet subband filtering. So the computation time for one subband filtering SB*ji* is $(2^{k-j}+6)$ clock cycles, where $N=2^k$, N is the frame length and k is an integer larger than j. For 3-level 256-point full-decomposition DWPT, the total computation time is around $(2^8/2^0+6)+(2^8/2^1+6)\times 2+(2^8/2^2+6)\times 4=810$ clock cycles. As shown in Fig 3, clock gating is also implemented by DWF_PE_enable signal to eliminate redundant switching so as to minimize the energy consumption in the DWF PE.

C. Address Generation & Best-Basis Configuration

Fig. 3 shows the control and address generation circuitry designed to supervise the DWF-PE to compute multi-subband filtering, recursively. The controller consists of a butterfly counter, a group counter, and a stage counter designed to keep track of which pair of input data samples, in which subband filtering (SB*ji*), and at which decomposition level, are being processed. With this information, the AGU can generate correct in-place memory R/W addresses for each subband filtering at different levels [14-15]. To deal with the boundary extension issues [5], the periodization method is implemented by using forward cyclic addressing method as described by the equation of *addr_periodized* = *addr* – *L*, where addr ∈ [0, 2^{k-j} - 1], $N=2^k$, N is frame length, and L is the filter tap number , e.g., L = 4 for D4 wavelet, as shown in Fig. 2 (b). This cyclic addressing method resolves the boundary issue of frame-based DWPT filtering so that event-driven signal processing with clock/power gating techniques can be applied to achieve ultra low energy for continuous healthcare monitoring [3].

To enable a specified-basis DWPT decomposition, a group counter control circuit is designed to use the information of group count and stage count to calculate the step of the next group counter increment. As depicted in Fig. 4, after starting a

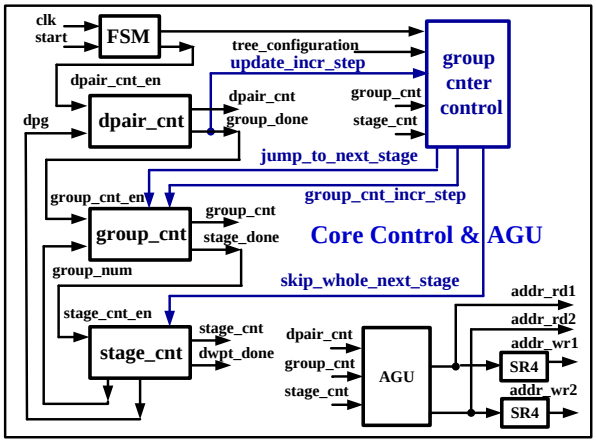

Fig. 3. Block diagram of the Group Counter Controller for subband filtering prediction.

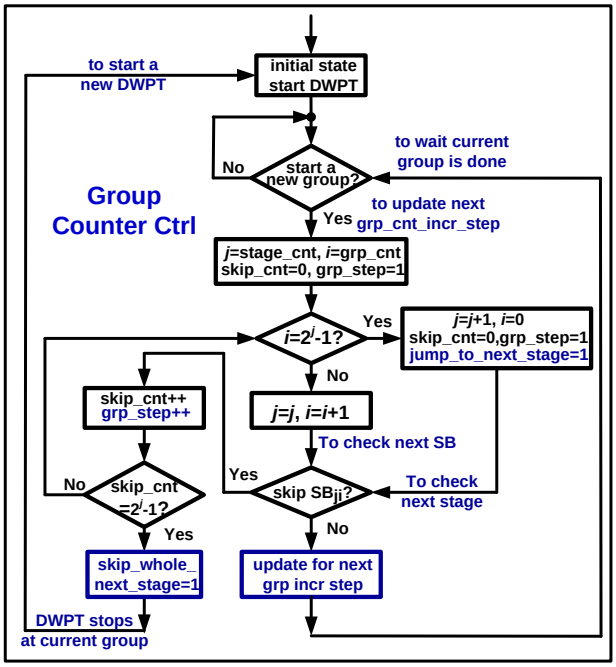

Fig. 4. Flow chart of the Group Counter Controller for subband filtering prediction.

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subband filtering of *stage_cnt*-th group of data at *grp_cnt*-th level, the group counter control circuit will start to predict what the next subband filtering is by checking the next or next few groups of control bits *skip_subband_ji*, and update the corresponding group counter increment step. Once one subband filtering is skipped, both the skip counter and group step counter will increment by one. Thus, a specific subband filtering or even a whole level of decomposition can be skipped depending on control bits *skip_subband_ji*. In this way, configurable DWPT decomposition with arbitrary tree structure can be computed in an efficient manner without any redundant data computation or movement [15-16], so that the required energy consumption can be minimized.

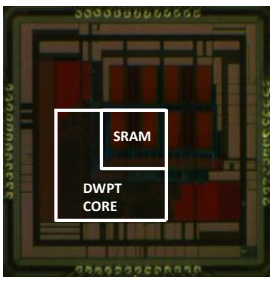
D. Near-Threshold Operation with Ultra-Low-Voltage Level Shifting

Due to the well-balancing among energy consumption, performance and variability, near-threshold operation has been adopted to maximize overall energy efficiency in this research. A 0.18-µm standard CMOS technology is used to implement the near-threshold DWPT processor. The processor has three power domains at a standard I/O 3.3V, a nominal 1.8V, and a near-threshold 0.6V, for I/O pads, commercial memory, and DWPT core logic, respectively. The voltage for the core logic can be scaled down from 1.8V to 0.6V. To implement the ultra-low-voltage and multiple power domain design, near-threshold logic cells and level shifters characterized at 0.6 V are used. The near-threshold cells are the logic cells with small delay and variation at ultra low voltages selected from the 0.18-µm standard cell library. The level shifter is a current-mirror based level shifter [17] optimized for enabling fast and energy-efficient level conversion from 0.6 V to 1.8 V between the core logic to the memory and I/O pads.

III. EXPERIMENT RESULTS & DISCUSSION

To verify the proposed reconfigurable DWPT processor architecture and circuit design, a 256-point 3-level D4 DWPT test chip was implemented and fabricated in a 0.18-µm CMOS technology. Fig. 5 shows the die photography with a total die area of 0.95 mm^2, and the DWPT core area is 0.53 mm^2. The design specification summary is also presented in Fig. 6. The DWPT core can work functionally from 1.8 V down to 0.5 V.

Table I presents the comparison between the proposed DWPT design and the state-of-the-art DWT designs. Our design is the only DWPT design which can perform multi-level decomposition with configurable time-frequency resolution. The DWT accelerators in [12-13] are designed by the DM architectures, in which *J* (4 and 6, respectively) wavelet filter pairs are implemented to occupy significantly more silicon area than single-PE recursive architecture designs, with shared memory banks in a DSP/CPU-core based biomedical processor. The recursive Symmlet-4 DWT engine in [11] consumes lesser silicon area and lower power for same voltage and frequency but it requires much longer computation time due to its ALU-based sequential computation architecture. The convolution-based D4 DWT in [13] consumes more computation power because it requires significant more arithmetic operations than lifting-based methods. By adopting lifting scheme and near-threshold operation, our DWPT processor consumes minimized power in performing full-tree decomposition of a 256-point random signal and entropy statistic calculations at 1MHz. With voltage scaling from 1.8 V to 0.5 V, the power consumption of our DWPT core is reduced by around 10× to 26 µW. The average power of the commercial SRAM at 1.8 V is 102.5 µW. Considering to adopt a near-threhold SRAM design at 0.5 V to replace the commercial memory, an estimated power reduction of 7× can be achieved [18], resulting in an average power consumption of 14.6 µW. So the estimated overall power consumption at 0.5 V would be around 40.6 µW.



Test Chip Summary	
Technology	0.18µm
Voltage	0.5~1.8V
Data width	16-bit
Frequency	1~20MHz
Gate count	14K
SRAM	512Byte
Power	128.5µW
Area	0.95mm²

Fig. 5. Die photograph and design summary of the test chip.

To quantify how the DWPT processor achieves energy efficiency over conventional microcontroller solution, we integrated the DWPT core into an ARM Cortex-M0 based biomedical SoC test platform with the memory-shared architecture as described in Fig. 1 (b). The SoC platform was implemented by the ultra-low-voltage design flow as described in Section II. B. Based on the 1.8-V standard cell library and 0.6-V near-threshold cell library, post-layout simulations have been carried out to estimate the time and energy required to perform DWPT decompositions of a 256-point random signal. Table II presents the comparison between using the ARM Cortex-M0 CPU to execute compiled C codes only and with the DWPT core. The SoC system can operate at 20 MHz at 1.8 V,

TABLE I. COMPARISION WITH THE STATE-OF-THE-ARTS

Params	[13]	[12]	[11]	This work
Process	90nm	180nm	180nm	180nm
Voltage	0.5V~1V	1.8V	1.3V	0.5V~1.8V
Data width	9-bit	16-bit	10-bit	16-bit
Wavelet	Convolution-based D4 wavelet	Quadratic-spline wavelet	Lifting-based Symmlet4 wavelet	Lifting-based D4 wavelet
Funct	6-level DWT based seizure epileptic detector	4-level DWT based QRS detector	4-level DWT processor	3-level DWPT processor with statistic engine
Freq	1.5kHz~1MHz	1MHz	6.4MHz	1~20MHz
Power	88µW* (0.5V,1.5kHz) 117.3mW# (0.5V,1MHz)	176µW@ (1.8V,1MHz)	76µW* (1.3V, 6.4MHz)	26µW@ (Core), 14.6µW* (RAM) (0.5V,1MHz)
Area	-	1.10mm^2	0.22mm^2	0.53mm^2 (Core) 0.42mm^2 (RAM)

* circuit simulation result; @silicon measurement result; # normalized simulation result in 180nm CMOS technology.

while it is only able to run up to 2.2 MHz at 0.6 V.

Assume the 256-point data is a frame of ECG signal sampled at 360 Hz, the CPU-only version is not able to perform real-time processing within the frame duration of 0.71 second at 0.6 V. This means that in order to enable energy-efficient near-threshold operation, a CPU-based biomedical processor must adopt efficient accelerators such as the proposed DWPT design to compensate performance loss due to aggressive voltage scaling, when performing computation-intensive and power-hungry DSP tasks including the DWPT. The simulation results show that the proposed DWPT design provides processing acceleration by three orders of magnitude, and achieves energy saving by four orders of magnitude, in the listed decomposition tasks. Although the CPU-only solution can be further improved by optimizing the C codes or employing hardware multipiers, the DWPT solution still can achieve orders-of-magnitude energy saving, contributed by the hardware acceleration and near-threshold operation.

TABLE II. COMPARISION WITH THE CPU-ONLY SOLUTION

DWPT Decomposition Tasks	CPU-Only Conventional Solution			Proposed DWPT Acceleration Solution		
	VDD	Time	Energy	VDD	Time	Energy
Full-tree decomposition	1.8V	0.5s	7.56mJ	0.6V	0.54ms	0.589μJ
DWT-tree decomposition	1.8V	0.31s	4.9mJ	0.6V	0.17ms	0.192μJ

Considering different physiological data processing tasks, 3-level best-basis decomposition is required in the biomedical SoC test platform, to perform ECG/EEG compression or EEG spike classification. As shown in Fig. 1 (b), different channels of ECG and EEG signals acquired from external sensors are directly buffered into the memory banks via the DMA, while the DSP core and the DWPT core are in sleep mode to save power. Once a predefined number of data samples have been accumulated, the DSP core will wake up to perform signal processing tasks by itself or by on-chip accelerators. When a few frames of acquired or processed data are ready in the memory bank, the DWPT core will be configured and activated by the DSP core via the registers to perform reconfigurable DWPT computation, as previously described in Section II.A. As shown in Table II, the DWPT core design can contribute energy saving by up to 35%, by reconfiguring the core from the full decomposition mode to collect statistic information, to different best basis decomposition according to the best basis search result, e.g., the DWT-tree decomposition.

IV. CONCLUSION

This paper has presented a first reported near-threshold reconfigurable DWPT processor design for healthcare monitoring applications. Effective design techniques from the algorithm level to circuit level have been applied to achieve optimized energy efficiency at minimized silicon area. The 0.18-μm 0.53 mm^2 DWPT core only consumes 26 μW at 0.5 V and 1 MHz. Analysis and discussion has been presented to show that the proposed DWPT processor design is an energy and area efficient solution suitable for DSP/CPU core based healthcare monitoring applications.

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