Enhancing Thermal Uniformity in Liquid-Cooled Inverters: Adjoint-Based Optimization of a Manifold Microchannel Coldplate

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***Abstract*— Power electronics inverters are a cornerstone of modern electric vehicle systems, where thermal management has emerged as a key barrier to achieving ambitious power density targets. This study addresses the critical issue of thermal non-uniformity in liquid-cooled inverters containing multiple discrete chips by optimizing coolant flow distribution. A cost-effective thermal test vehicle (TTV) was developed, utilizing stacked platinum ceramic heaters to accurately simulate the thermal behavior of a commercial inverter. Initial experiments with a baseline cooling manifold revealed a significant flow imbalance, resulting in chip-to-chip temperature variations of up to 3.7°C. An adjoint-based shape optimization methodology was employed to redesign the manifold geometry for superior flow uniformity. Experimental validation of the optimized design, tested across three distinct microchannel configurations, confirmed a substantial improvement in thermal performance. The maximum chip-to-chip temperature difference was reduced to approximately 1°C while maintaining high cooling effectiveness and reducing pumping power by 3.4-9.9%. The optimized system demonstrates a viable and manufacturable path toward high-performance thermal management in compact, power-dense inverter designs.**

***Index Terms*— Adjoint methods, Computational fluid dynamics (CFD), Liquid cooling, Microchannel heat sinks, Manifolds, Power inverters, Shape optimization, Thermal management**

I. INTRODUCTION

The rapid electrification of the transportation sector has created unprecedented demands for high-performance power electronics. Automotive inverters, which convert DC power from the battery to the AC required by the motor, are central to this transition. Aggressive power density targets, such as the 100 kW/L goal set by the U.S. Department of Energy, have pushed conventional air-cooling methods to their limits [1]. Modern electric vehicle powertrains require inverters to manage over 150 kW of power within a compact volume, presenting immense thermal management challenges that necessitate innovative liquid cooling solutions capable of dissipating heat fluxes exceeding 300 W/cm² while maintaining device junction temperatures within safe operational limits [2-3]

The critical challenge in multi-chip systems extends beyond the magnitude of heat removal to encompass spatial uniformity. Typical inverter modules contain six or more discrete semiconductor chips arranged on a single substrate, creating spatially heterogeneous heat generation patterns [4]. Unlike single-chip applications where cooling can be concentrated, multi-chip modules require uniform heat extraction across the entire surface. Flow maldistribution within cooling systems leads to localized hot spots and temperature gradients between devices [5], which induce thermal-mechanical stress, accelerate uneven device aging, and ultimately compromise long-term inverter reliability [6]. This study directly addresses these challenges by optimizing coolant manifold geometry to achieve thermal uniformity in realistic multi-chip environments.

Modern high-flux thermal management traces its roots to the pioneering work of Tuckerman and Pease [7], who demonstrated that microchannel cooling could achieve remarkable heat removal rates exceeding 790 W/cm². Subsequent research explored modifications to channel geometry and surface features to enhance heat transfer [8], [9]. The manifold microchannel (MMC) heat sink, proposed by Harpole and Eninger [10], represented a significant breakthrough. By incorporating manifolds to distribute coolant, MMC designs shorten effective flow paths, substantially reducing system pressure drop while improving heat transfer through localized fluid impingement.

This cooling concept has evolved toward direct chip-level integration, where microfluidic channels are fabricated directly into semiconductor wafers, enabling management of heat fluxes surpassing 1 kW/cm² [11-12]. Van Erp et al. [12] demonstrated co-designed electronic and thermal systems capable of achieving power densities of 1723 W/cm² for 0.3×0.3 cm² heat sources with maximum temperature rises of only 60 K at pressure drops of 40 kPa and flow rates of 60 mL/min. Similarly, Drummond et al. [11], [13] developed hierarchical manifold systems managing heat fluxes up to 910 W/cm² under two-phase flow conditions, while Jung et al. [14] demonstrated excellent thermal performance with low pressure drop in embedded MMC designs.

Given the modular nature of MMC designs, subsequent research has focused on optimizing fundamental "unit cells", as shown in Fig.1(a), to enhance thermal performance through

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passive enhancement techniques, including modified microchannel geometries [15-18], incorporating different fin structures [19-23], and applying topology optimization to individual channel sections [24-25]. Ryu et al. [15] used steepest descent methods to optimize geometric parameters, reducing thermal resistance by over 50% compared to conventional designs, while Arie et al. [18] developed computationally efficient hybrid models for multi-objective optimization. Yang et al. [26-27] introduced secondary oblique channels that experimentally reduced both pressure drop and thermal resistance simultaneously. Tang et al. [20] demonstrated that combining diverging manifolds with converging channels could reduce thermal resistance by 19.18%, while Pan et al. [15] explored cylindrical pin-fins instead of rectangular fins, finding improved heat transfer at given mass flux with optimal spacing ratios balancing performance against increased pressure drop.

However, these unit-cell studies typically assume idealized, uniform incoming flow, overlooking system-level flow maldistribution effects that often dominate thermal performance in practice, where fluid makes sharp turns into microchannels [28]. This phenomenon leads to preferential cooling of certain chips while other chips receive insufficient flow and are prone to overheating undermining uniform cooling goals and negating benefits of high-capacity heat sink designs.

Efforts to improve thermal uniformity in MMC heat sinks have centered on optimizing manifold geometry and flow arrangements to counteract inherent maldistribution, as shown in Fig.1(b). Tang et al. [30] employed tapered contracting structures for inlet plenums and manifold channels, resulting in more uniform temperature distributions and reduced maximum surface temperatures by approximately 24 K. Chen et al. [31] evaluated various converging manifold structures, including tapered, parabolic, and elliptical designs, concluding that parabolic profiles offered optimal performance balance through precise convergence rate control. Escher et al. [32] experimentally validated designs with tapered inlets and expanding outlets, achieving total thermal resistance of 0.09 cm^2K/W.

Alternative approaches involve adding structures within manifolds to actively manage flow. Zhou et al. [33] introduced ribs of varying heights, improving flow and temperature uniformity by 84.0% and 63.3%, respectively, while Pu et al. [34] used flow-regulating baffles to enhance flow uniformity by 70.7% and temperature uniformity by 44.6%. Sharma et al. [35] applied this principle specifically for non-uniform heating, using optimized microchannel geometries to throttle coolant flow in low heat-flux areas, reducing chip-wide temperature variation from 10°C to 4°C.

On systemic levels, researchers have reconfigured overall flow paths. Kong et al. [36] found that arrangements with opposing manifold inlets and central vertical outlets provided most uniform flow, reducing thermal resistance by up to 47% and pressure drop by up to 90%. Zhang et al. [37] introduced countercurrent flow regions, decreasing pressure drop by 33.4% while limiting maximum temperature differences to less than 4 K. Yang et al. [38] developed compact double H-type manifolds reducing pressure drop by 56% compared to traditional designs, effectively managing 417 W heat loads for large-area chip cooling.

While these studies demonstrate that manifold geometry and flow arrangement can improve thermal performance, they often introduce practical limitations. Many proposed solutions rely on complex multi-layer arrangements or require large inlet plenums to precondition flow, as shown in Fig.1(c), adding significant volume and manufacturing complexity incompatible with stringent power density requirements. More efficient approaches would integrate plenum and manifold functions into single, compact components. However, designing such components to achieve uniform flow distribution across multi-chip modules presents formidable optimization challenges not easily solved with traditional parameter sweeps.

Advanced computational methods offer powerful alternatives to address this complexity. Two dominant approaches have emerged: topology optimization and adjoint-based shape optimization. Topology optimization addresses optimal material distribution within given design spaces, often yielding free-form, intricate structures unconstrained by conventional geometric primitives [39-40]. While powerful for generating novel concepts, these geometries can present significant manufacturing challenges. Adjoint-based shape optimization operates by refining boundaries of predefined geometries, exceptionally well-suited for improving existing designs by producing smooth, manufacturable modifications while efficiently handling large numbers of design variables [41-43]. The methods are highly complementary— topology optimization excels in conceptual phases while shape optimization excels at detailed design refinement. Since this work aims to improve performance of known manifold configurations for practical applications, adjoint-based shape optimization represents the more appropriate and targeted methodology.

This work aims to bridge the gap between idealized manifold microchannel studies and practical thermal management challenges of multi-die, high-power-density electronics. The scope focuses on manifold shape optimization for single-phase, direct liquid cooling cold plates, with results validated experimentally on a custom-designed thermal test vehicle (TTV) referencing a real commercial six-in-one power modules. The methodology employs a hybrid manufacturing strategy selected for scalability and cost-effectiveness, leveraging high-resolution Stereolithography (SLA) to fabricate geometrically complex, optimized manifolds integrated with copper bases containing microchannels produced via conventional CNC machining. This approach provides a practical, lightweight, and economically viable alternative to monolithic components produced via metal additive manufacturing methods such as Selective Laser Melting (SLM), combining design flexibility of SLA for complex manifolds with high thermal conductivity and established manufacturability of conventional copper heat sinks. The primary goal is demonstrating robust methodology for

eliminating flow-induced thermal imbalances in realistic multi-chip inverter configurations, thereby enhancing system reliability while maintaining high heat flux removal capabilities.

II. Experimental Setup and Test Vehicle Development

A. Liquid Cooling Test Loop

The testing cold plate incorporates an inlet manifold that divides flow into dual streams, subsequently directing coolant to six SiC chips location as shown in Fig. 2(a). This configuration enables jet impingement directly over chip/hot spot regions, maximizing cooling effectiveness. Following impingement, flow is further directed through microchannels to enhance heat transfer before exiting through outflow streams. The aggregate volume of the SiC MOSFET module and cold plate is estimated at approximately 0.04 liters.

The experimental setup consists of a closed-loop liquid cooling system designed to provide precise thermal boundary conditions and accurate performance measurements, as shown in Fig. 2(b). The system incorporates a gear pump (Fluid-o-Tech FG309) to circulate deionized water at a controlled temperature through the test section. Inlet temperature control is maintained using a precision water bath (Julabo DD450, with M+R in-line Pt100 sensor, ±0.01 °C stability) coupled with a plate heat exchanger to ensure stable thermal boundary conditions.

Flow rate measurement is accomplished using a turbine flow meter (McMillan 106-7D) positioned upstream of the test section, while pressure drop across the cold plate is monitored using a differential pressure transducer (Omega MMDWB10WBIV5K3MC0T1A2CE, range 0-2.5 kPa, ±0.08% accuracy). Inlet temperature is measured and feedback-controlled by the aforementioned inline PT100 RTD sensor positioned immediately upstream of the cold plate inlet.

Temperature measurements from the TTV are acquired using a high-precision data acquisition system (Keysight DAQ970A, DAQM900A for resistance measurements employing four-wire resistance measurement to eliminate lead wire effects, and DAQM901A for remaining measurements). Electrical power is supplied by a programmable power supply (Keysight E36155A) with four-wire sensing capability to ensure accurate voltage delivery despite contact resistance variations. All power wires connected to heaters are maintained at equal lengths, with wire resistance from power supply to heater measured at less than 0.1 Ω compared to heater resistance values exceeding 13 Ω at room temperature (increasing at higher temperatures), ensuring >99% of heat generation occurs at the heaters. During testing, all components are insulated using closed-cell foam to minimize parasitic heat losses and maintain temperature stability.

B. Thermal Test Vehicle Assembly

Development of a representative thermal test vehicle presented unique challenges in simulating both thermal and geometric characteristics of real inverter chips. Commercial high-temperature platinum heaters (H540 S, DIN EN IEC 60751 standard) were selected for their excellent temperature stability and sensing accuracy. Each heater features a 3.1×2.1 mm effective heating area on an Al_2O_3 substrate, closely matching the chip size of the referenced power module, WolfPACK (CCB021M12FM3) [44]. Thus, a chip heating power of 20.5 W corresponds to a heat flux of 315 W/cm².

As shown in Fig. 3, the TTV design employs a novel stacked configuration where two identical heaters are assembled with platinum elements facing each other, separated by a phase-change thermal interface material (TIM, Honeywell PTM7950, 0.1 mm sheet). This arrangement allows the top heater to function as a controllable heat source while the bottom heater serves as an integrated temperature sensor, providing direct measurement of chip-level temperatures without external sensors. This arrangement also reduces the distance between heater and sensor compared to temperature sensor solution in the original power module, where sensors are located at the heater periphery. Using estimation with lumped analysis, in worst-case scenarios when no compression is applied to the TIM, the estimated Thermal Time Constant (τ) is approximately 0.0172 s, with time to reach 99.9% of final temperature being 0.12 s, guaranteeing fast response time for the TTV potentially suitable for dynamic test scenarios [45].

The assembly process begins with soldering Pt wire connections of chips to the PCB board designed referencing the power module layout. A 0.1 mm-thick silicone pad is placed between the PCB and lower chips. Phase-change TIM is applied between heater elements, followed by temporary assembly with a smooth, flat AlN pressure plate on top. The assembly is then heated to 60 °C under controlled pressure for 2 hours to ensure proper TIM cure and establish mechanical adhesion between components after cooling down. The silicone pad at the bottom prevents mechanical damage to chips during this process.

After curing, the temporary AlN plate is removed and replaced with a copper heat spreader/lid using fresh TIM (Shin-Etsu X-23-7921-5) applied between surfaces. This final assembly provides both mechanical protection and enlarged thermal contact with the cold plate. Additionally, thermal gap filler (Techinno Fill-gel 800) can be added to fill the voids between Pt wires of heaters and the top lid as a safety measure, allowing excess heat conducted to Pt wires to dissipate, preventing melting or PCB damage. PTFE PCB was used in building all TTVs for heat resistance and fire retardancy. The cold plate and TTV stack configuration is shown in Fig. 4, with multiple TTV assemblies fabricated and tested to verify repeatability of this assembly process.

C. Temperature Calibration and Validation

Accurate temperature measurement is critical for thermal uniformity assessment, requiring careful calibration of integrated platinum temperature sensors. Calibration is performed in-situ using the test loop with the TTV mounted to the cold plate under no-power conditions. Inlet temperatures are varied from 20 °C to 90 °C in 10°C increments, with 3-hour equilibration periods at each setpoint to ensure thermal stability indicated by the inline PT100 is within ±0.02 °C.

As shown in Fig. 5, platinum sensors demonstrated excellent linearity across the full temperature range, with R^2 value of fitted curve exceeding 0.9999. While commercial grade PT100 sensors of required size were not available for direct comparison, a Class 1 Type-T thermocouple was positioned adjacent to a chip in the TTV during calibration to provide independent temperature verification. Differences between platinum sensors and thermocouple measurements were within ±0.5°C, confirming at least Class 1 accuracy for the integrated sensors.

D. Thermal Performance Testing Protocol

Cold plate performance evaluation follows a testing matrix covering both flow rate (0.5-2.0 L/min) and heating power of 13.3W, 16.7W, and 20.5W for each chip (80W, 100W, and 123W total power), corresponding to 14.0V, 16.0V, and 18.0V supplied voltage. Power control is maintained through constant voltage supply, with total power variations of ±1W readily detectable due to temperature-dependent resistance characteristics of the heaters. Each test condition includes a 1-hour stabilization period followed by 2 minutes of data acquisition at 1 Hz sampling rate to capture steady-state performance. Both calibration and thermal tests are conducted with program-controlled automated test equipment (ATE) to eliminate human error and ensure optimal repeatability.

III. Methodology and Numerical Optimization

A. Initial Flow Distribution Analysis

Thermal imbalance in multi-die modules originates from non-uniform coolant distribution within supply manifolds. Consequently, the primary optimization objective was achieving uniform mass flow distribution at manifold outlets. A decoupled optimization strategy was employed, focusing exclusively on the manifold's fluid domain to isolate dominant fluid dynamic mechanisms and enable rapid design iteration, which would be computationally prohibitive if the full conjugate heat transfer model with microchannel flow regions were included in the optimization loop.

The manifold's internal fluid volume was extracted from CAD models. The original geometry was defined by lofting inlet, outlet, and intermediate elliptical profiles, chosen to facilitate smooth shape modifications during optimization. To mitigate entrance and exit effects, the computational domain was extended 10 mm upstream and 30 mm downstream from the manifold. The inherent symmetry of the design permitted simulation of only one-quarter of the full domain, significantly reducing computational cost, as shown in Fig. 6.

The flow field was modeled assuming steady, incompressible, laminar flow, governed by the Navier-Stokes equations:

$$\nabla \cdot u = 0$$
$$\rho(\mathbf{u}\cdot\nabla)\mathbf{u} = -\nabla p + \mu\nabla^2\mathbf{u} \tag{1}$$

where u is the velocity vector, p is static pressure, ρ is the fluid density, and μ is the dynamic viscosity.

A mass flow rate of 0.5 L/min was specified at the inlet. Outlets corresponding to downstream microchannels were modeled as constant-pressure boundaries. This simplification focuses optimization on manifold-induced flow maldistribution. The governing equations were solved numerically using a pressure-based solver with the SIMPLEC algorithm for pressure-velocity coupling. A second-order upwind scheme was used for spatial discretization of momentum equations, with convergence residuals set to 10^{-5} for both velocity and continuity.

A mesh independence study was conducted using polyhedral elements to ensure numerical solution accuracy. As detailed in Table I, pressure drop across the manifold was evaluated for six mesh densities. The solution obtained with Mesh #5 (377k cells) deviated by only 0.18% from the finest mesh (#6). The mesh is shown in Fig.7 (a). Note that the elliptical profile used in the "original design" was parameterized to create 100 sets of Design of Experiments (DOE) designs, with the final candidate selected for best uniformity as a common parameter optimization approach for comparisons as well.

TABLE I
MESH INDEPENDENCE STUDY RESULTS

Mesh Ref.	Cell Count	Pressure Drop Deviation
#1	53k	-35.92%
#2	78k	-26.49%
#3	86k	-11.10%
#4	110k	-7.35%
#5	377k	**Baseline**
#6	1.24M	-0.18%

B. Adjoint-Based Shape Optimization

Shape optimization was performed using a gradient-based discrete adjoint method to efficiently compute geometric sensitivities. For a given objective function J and a vector of design parameters c (representing mesh node coordinates), the total sensitivity is given by:

$$\frac{dJ}{dc} = \frac{\partial J}{\partial c} + \tilde{\mathbf{q}}^T\left(\frac{\partial \mathbf{R}}{\partial c}\right) \tag{2}$$

where R are the residuals of the discretized Navier-Stokes equations and $\mathbf{q}$ are the adjoint variables. The adjoint variables are obtained by solving the linear adjoint system:

$$\left(\frac{\partial \mathbf{R}}{\partial \mathrm{q}}\right)^T \tilde{\mathbf{q}} = -\left(\frac{\partial J}{\partial \mathrm{q}}\right)^T \tag{3}$$

This discrete adjoint formulation bypasses the computationally prohibitive direct calculation of flow sensitivities and ensures mathematical consistency with the primal flow solver.

The optimization was framed as a multi-objective problem. The manifold outlet was partitioned into n discrete sub-regions, where n was progressively increased from 3 to toward an upper limit during the optimization to refine control over local flow features. N = 10 was selected in this study to achieve a compromise between computational efficiency and optimization efficacy. For each sub-region i, the volumetric flow rate, Q_i was defined as an observable:

$$Q_i = \int_{Ai} \mathbf{u}\cdot\mathbf{n}\,dA \tag{4}$$

At each design iteration, the algorithm identified sub-regions with minimum, $Q_{min,}$ and maximum $Q_{max,}$ flow rates. These two observables were then targeted simultaneously. A target change (step size) was specified for each—an increase for $Q_{min,}$ and a decrease for Q_{max}—to drive both values toward the mean flow rate, Q_{avg}.

The overall iterative optimization algorithm proceeds as follows:

(1) The Navier-Stokes equations were solved for the current geometry to establish the flow field.

(2) Separate adjoint solutions are computed to find the unique sensitivity gradients for Q_{min} and Q_{max} with respect to the surface mesh node positions.

(3) A single geometric deformation vector, Δc, is computed.

(4) This deformation is applied to the geometry using a radial basis function for smooth mesh morphing.

This cycle was repeated for approximately 200 iterations until the objective function converged, or geometric constraints (minimum wall thickness) were reached. The geometric comparison between the original design and the optimized design is shown in Fig. 7(c).

IV. Results and Analysis

A. Optimization and Flow Uniformity

The optimization domain was restricted to internal manifold surfaces, preserving inlet and outlet geometries for compatibility with upstream and downstream cold plate components. The optimization process was conducted in Ansys Fluent adjoint solver with full automation of the iterative procedure via Ansys pyFluent.

Fig. 8(a) presents the velocity magnitude profile at the manifold outlet (not the extension outlet in the simulation domain, as shown in Fig.6(c)). The adjoint-based optimization successfully redistributed internal manifold flow: the high-flow region initially concentrated near the manifold center was redistributed toward the periphery, significantly improving flow uniformity. This improvement is quantified in Fig. 8(b), which shows flow rates passing through each of the 19 sub-regions or channel units (corresponding to 0.5 mm channel width microchannels used in the design). The optimization yielded a 35.4% reduction in standard deviation of flow rates across all outlet channel units. Notably, the flow rate to channel units covering the outermost chip region (C6) increased by 135.8%, while flow to the over-saturated central region (C5) decreased by 16.2%.

The optimization was terminated when further geometric modifications were limited by manufacturing constraints (minimum feature size for 3D printing) and the onset of detrimental recirculation zones that would increase pressure drop penalties. The optimized shape was converted to CAD models and fabricated using SLA 3D printing, as shown in Fig. 7(b), with 5 μm resolution and 50 μm layer thickness to balance fabrication cost and geometric fidelity.

B. Experimental Validation and Thermal Performance

Experimental measurements of fabricated designs validated optimization effectiveness. The uncertainty of thermal resistance measurements was calculated to be 0.039 °C/W, primarily attributed to instrumentation. Additional uncertainty arose from variations in manual TIM application and assembly processes—a 10 μm TIM thickness difference corresponds to approximately 0.08 °C/W, or a temperature difference of 1.68 °C at 20.5 W.

Three different microchannel geometries were fabricated using precision slitting saws to investigate interaction between manifold design and fin structure. Channel widths of 0.5 mm, 0.3 mm, and 0.2 mm were created with corresponding fin widths of 0.3 mm, 0.3 mm, and 0.2 mm respectively, limited by manufacturing capabilities.

As shown in Fig. 9, channel width reduction from 0.5 mm to 0.2 mm resulted in proportional increases in heat transfer surface area, with corresponding improvements in overall thermal performance. However, denser fins also increase flow restriction; therefore, pumping power for the 0.2 mm sample is also 30% higher than that for the 0.5 mm sample. Conversely, the optimized design reduces pumping power by 3.8% for the 0.5 mm sample at 1.9 L/min and 9.9 % at 0.7 L/min, and pumping power by 3.4% for the 0.2 mm sample at 1.9 L/min and 5.5% at 0.7 L/min respectively. The lowest specific average thermal resistance, $R_{th.avg}$, achieved was 9.3 °C·mm^2/W for the 0.2 mm sample with the original manifold, and 9.8 °C·mm^2/W for the optimized manifold at 1.9 L/min flow rate, reflecting a 5.1% trade-off in the cooling performance. It should be noted that while the optimization objective was to achieve uniform flow distribution across the entire outlet, only three discrete chips were instrumented in this experimental test; therefore, thermal uniformity analysis is limited to these measurement locations.

C. Thermal Uniformity Improvements

The large lateral distance differences among chips C4, C5, and C6 along the y-axis provides a basis for assessing flow uniformity within a single flow stream. Experimental results demonstrated significant thermal uniformity improvements across all test conditions. As shown in Fig. 10, for the original manifold, the maximum chip-to-chip temperature difference, $\Delta T_{\max}$, reached as high as 3.7 °C. The optimized manifold reduced $\Delta T_{\max}$ to approximately 1 °C across all tested microchannel configurations (Table II). To investigate the robustness of the optimization under varying loads, Fig. 11 presents the thermal resistance spread, ΔR_{th}, calculated from the measured temperature spread, $\Delta R_{\text{th}} = (T_{\max}\text{-}T_{\text{fluid}}) / Power - (T_{\min}\text{-}T_{\text{fluid}}) / Power = \Delta T_{\max} / Power$, as a function of flow rate across all tested power levels for both original and optimized manifolds. The data reveals that the optimized design maintains a consistently low $\Delta R_{\text{th}} \approx 0.05$ °C/W, significantly lower than the baseline, regardless of the input power. This indicates that the improvement in thermal uniformity is a structural characteristic of the optimized flow field and is not an artifact of specific operating conditions. This stability suggests that the benefits of the optimized manifold will persist and likely become more critical at the substantially higher power levels typical of full-scale automotive inverters.

To establish the quantitative link between manifold-level flow redistribution and the measured chip-level thermal uniformity improvements, the complete thermal resistance network from coolant to chip is analyzed in the following section.

TABLE II
SUMMARY OF THERMAL UNIFORMITY IMPROVEMENT (AT 1.9 L/MIN, 20.5W PER CHIP)

Microchannel Width	**ΔT_{max} (Original)**	**ΔT_{max} (Optimized)**
0.2 mm	3.0 °C	0.9 °C
0.3 mm	3.7 °C	0.9 °C
0.5 mm	2.8 °C	1.1 °C

D. Analysis of the Thermal Resistance Stack and Its Impact on Uniformity

While Fig. 10 clearly demonstrates that the optimized manifold improves thermal uniformity, it is essential to rigorously analyze the link between improved flow distribution and the final measured chip temperatures through the complete thermal resistance network from the cooling fluid to the chip surface, as illustrated in Fig. 3(a). This network consists of several components in series:

$$R_{th.total} = R_{th.coldpate} + R_{th.TIM2} + R_{th.Lid} + R_{th.TIM1} \quad (5)$$

where $R_{\text{th.coldplate}} = R_{\text{th.conv}} + R_{\text{th.base}}$. Here, $R_{\text{th.conv}}$ represents the convective thermal resistance from the coolant to the cold plate wall, $R_{\text{th.base}}$ is the conductive resistance through the copper cold plate base, $R_{\text{th.TIM2}}$ is the resistance of the thermal interface material between the cold plate and the heat spreader/lid, $R_{\text{th.lid}}$ is the conductive resistance through the copper lid, and $R_{\text{th.TIM1}}$ is the resistance of the thermal interface material between the lid and the chip.

Flow maldistribution in the baseline manifold directly causes spatial variation in the local heat transfer coefficient, h, which creates significant variation in $R_{\text{th.conv}}$ across different microchannel units. The other resistances in the stack ($R_{\text{th.base}}$, $R_{\text{th.TIM2}}$, etc.), while substantial, are primarily associated with solid-state conduction and material interfaces. The experimental methodology was designed to minimize variability in these factors by using a single, carefully assembled TTV with consistent TIM application and uniform mounting pressure for all tests (baseline and optimized). Therefore, these resistances can be assumed to remain relatively constant at each chip location throughout the experiments.

To quantify the contributions, thermal resistance values were estimated for a representative chip location based on the geometric and material properties described in Section II. The solid-state resistances (base + lid) contribute approximately 0.01 °C/W, while the interface resistances (TIM1 + TIM2) contribute approximately 0.77 °C/W. The total thermal resistance, $R_{\text{th.total}}$, for all tests was in the range of approximately 1.6 °C/W. The remaining component, convective resistance, therefore accounts for approximately 0.8 °C/W.

From this simplified one-dimensional analysis, interface resistances contribute significantly to the overall thermal resistance. However, the convective resistance is also a substantial component and is the only component directly influenced by fluid dynamics. Spatial variation in this foundational convective boundary condition propagates through the thermal stack, manifesting as the temperature differences measured at the chips.

Therefore, while absolute chip temperatures are a function of the entire thermal stack, the non-uniformity in temperature (ΔT_{max}) is primarily driven by non-uniformity in coolant flow distribution. By optimizing the manifold to homogenize flow distribution, the root cause of thermal imbalance at the convective boundary is directly addressed, leading to the significant and measurable improvements in chip-level thermal uniformity demonstrated in the experimental results.

With good temperature uniformity and plenty of cooling budget to reach the typical maximum allowable junction temperature of 150 °C for SiC power modules (corresponding to estimated heat flux densities of approximately 800 W/cm²), scenarios of temperature spikes or overshoot on any chips due to cooling maldistribution can be eliminated. This suggests strong potential for meeting aggressive thermal management requirements in power electronics applications.

It is important to note that while the total cooling capacity of the system is high (resulting in low absolute junction temperatures in this test), 'excess' capacity does not inherently resolve thermal non-uniformity. The baseline design, despite having identical cooling capacity and pumping power to the optimized design, exhibited a 3.7°C spread solely due to flow maldistribution. In high-voltage traction inverter applications where heat fluxes exceed 300 W/cm², the convective resistance component becomes increasingly dominant. Under such conditions, the flow imbalances observed in the baseline design would translate to dangerous junction temperature gradients, accelerating device degradation. Therefore, optimizing the flow distribution is not redundant; it is a critical requirement for ensuring the reliability of high-power density modules where thermal margins are minimal.

V. CONCLUSION

This study demonstrated that non-uniform manifold flow is a primary driver of thermal imbalance in multi-chip modules and validated adjoint-based optimization as an effective tool for mitigating it. A cost-effective thermal test vehicle was developed that confirmed the dominance of manifold-level flow distribution over local fin geometry in determining chip-to-chip temperature variations.

The adjoint-based shape optimization successfully redistributed coolant flow, reducing the standard deviation of outlet flow rates by 35.4%. This directly translated to improved thermal performance, with measured chip-to-chip temperature variations decreasing from a maximum of 3.7 °C to approximately 1 °C. These gains were achieved across multiple microchannel geometries and were accompanied by modest reductions in pumping power (3.4-9.9%), indicating a robust and efficient design. The resulting system demonstrates capability to manage high heat fluxes while maintaining thermal uniformity, providing a strong foundation for systematic thermal design of next-generation power electronics.

The demonstrated approach provides a foundation for systematic thermal design optimization in next-generation power electronics systems. Future work should focus on validation with actual inverter hardware, investigation of transient thermal behavior, and extension to alternative coolants and operating conditions.

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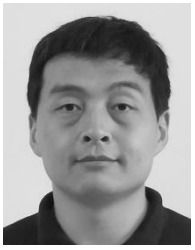

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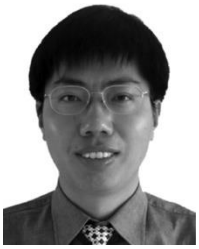

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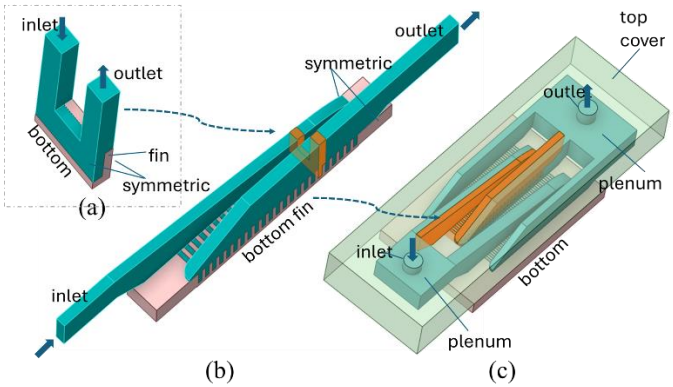

Fig. 1 Schematics of the MMC cooling concept. (a) A unit cell showing fluid impingement and flow through a single microchannel. (b) A unit stream illustrating the flow of liquid from a manifold stream to multiple microchannels. Tapered contracting and expanding structures for inlet and outlet sections were implemented to enhance flow uniformity. (c) A typical MMC cold plate assembly with inlet/outlet manifolds and the microchannel array. Both inlet and outlet plenums were adopted to precondition flow.

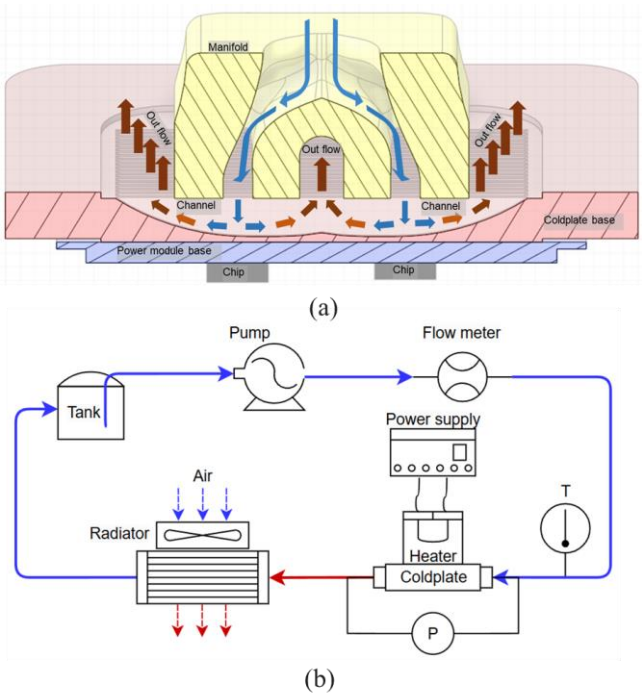

Fig. 2 System-level schematics. (a) The proposed flow path for the dual-stream cold plate, showing coolant distribution to the discrete chip locations. (b) Diagram of the closed-loop liquid cooling system used for experimental testing and validation.

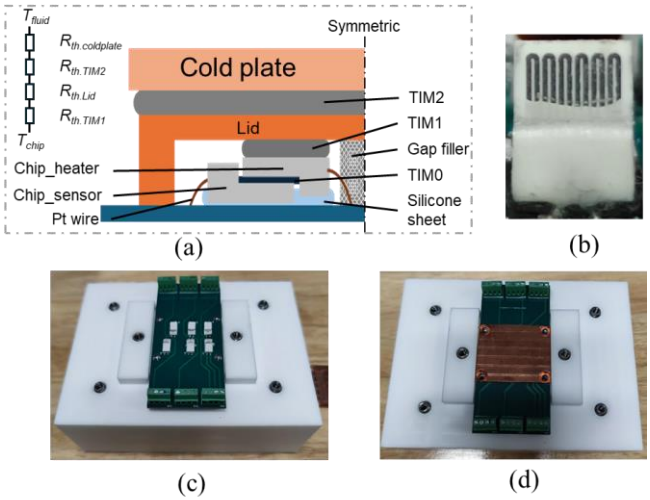

Fig. 3 Thermal Test Vehicle assembly process. (a) Schematic of the stacked heater-sensor configuration. (b) The platinum heater chip, with the top insulation layer partially removed to show the serpentine heating element. (c) The six heater-sensor pairs assembled on the custom PTFE PCB. (d) The final TTV assembly with the copper heat spreader mounted.

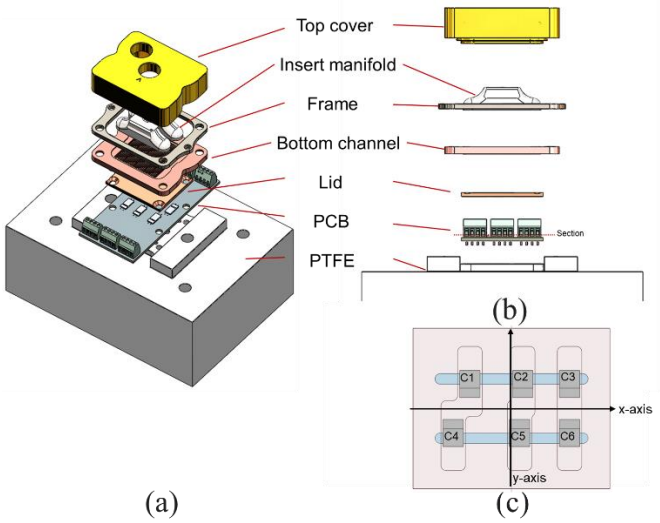

Fig. 4 Cold plate and TTV assembly views. (a) Isometric view of the complete test assembly. (b) Side view showing the stacked components. (c) Bottom cross-sectional view illustrating the fluid region (blue) and the relative positions of the chip locations (C4, C5, C6) with respect to the cooling stream inlet.

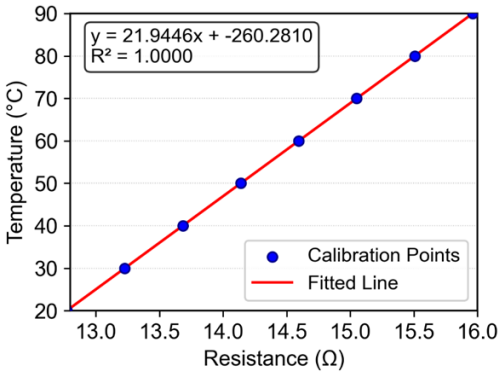

Fig. 5 In-situ temperature calibration curve for a representative integrated platinum sensor. The plot shows measured resistance versus reference temperature, demonstrating excellent linearity ($R^2 > 0.9999$) across the operating range.

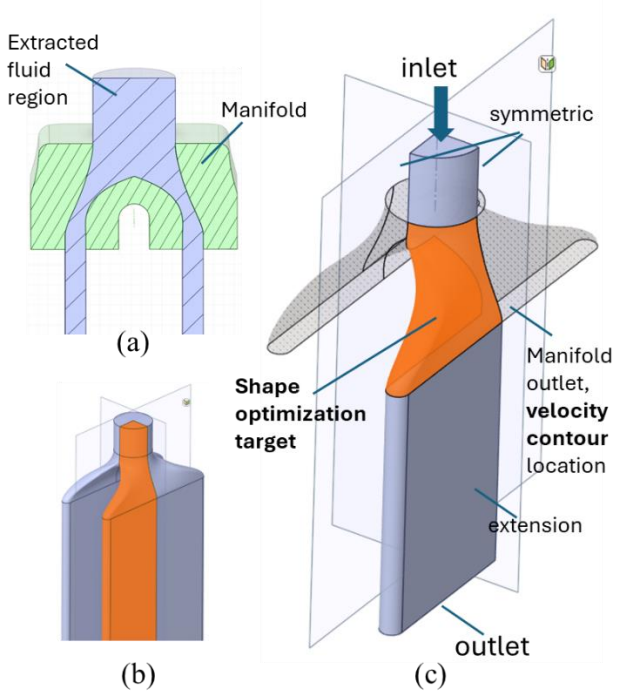

Fig. 6 Computational domain for the numerical optimization. (a) The extracted internal fluid region of the manifold. (b) The full simulation domain including the 10 mm inlet and 30 mm outlet extensions to mitigate boundary effects. (c) The one-quarter symmetry model used for simulation. Yellow surfaces indicate regions targeted for shape optimization.

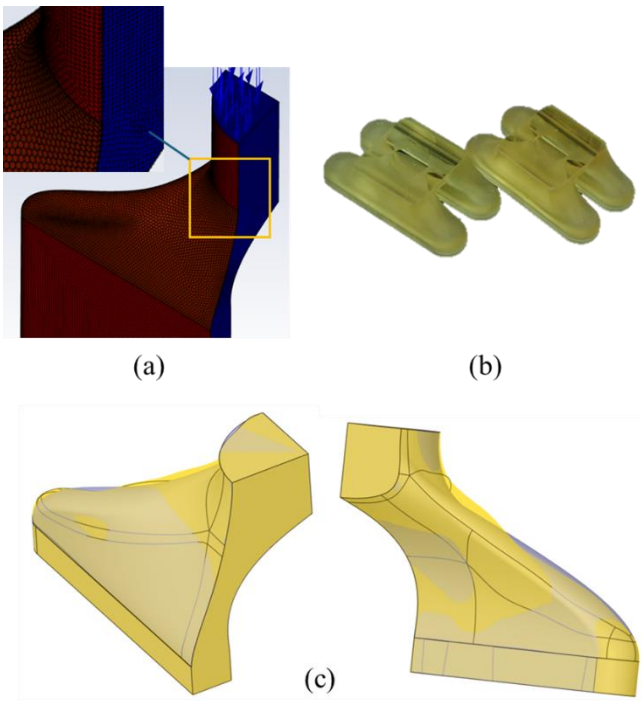

Fig. 7 Mesh and fabricated component for the numerical and experimental work. (a) The generated polyhedral mesh (377k cells) used for the CFD analysis. (b) The optimized manifold fabricated using high-resolution SLA. (c) The comparison of the original (in gray color) and optimized design (in yellow

transparent color) in terms of overlapped geometry) from two view directions.

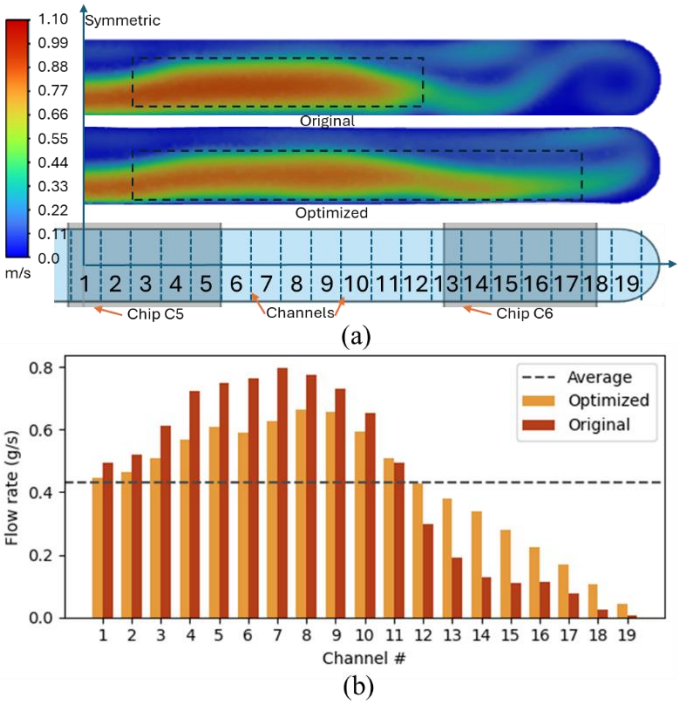

Fig. 8 Simulated flow uniformity results comparing the original and optimized manifold designs. (a) Velocity magnitude contours at the manifold outlet, with the relative locations of the chips and sub-regions/channel units overlaid. (b) Volumetric flow rate distributed to each of the 19 sub-regions/channel units, quantifying the 35.4% reduction in flow rate standard deviation achieved by the optimization.

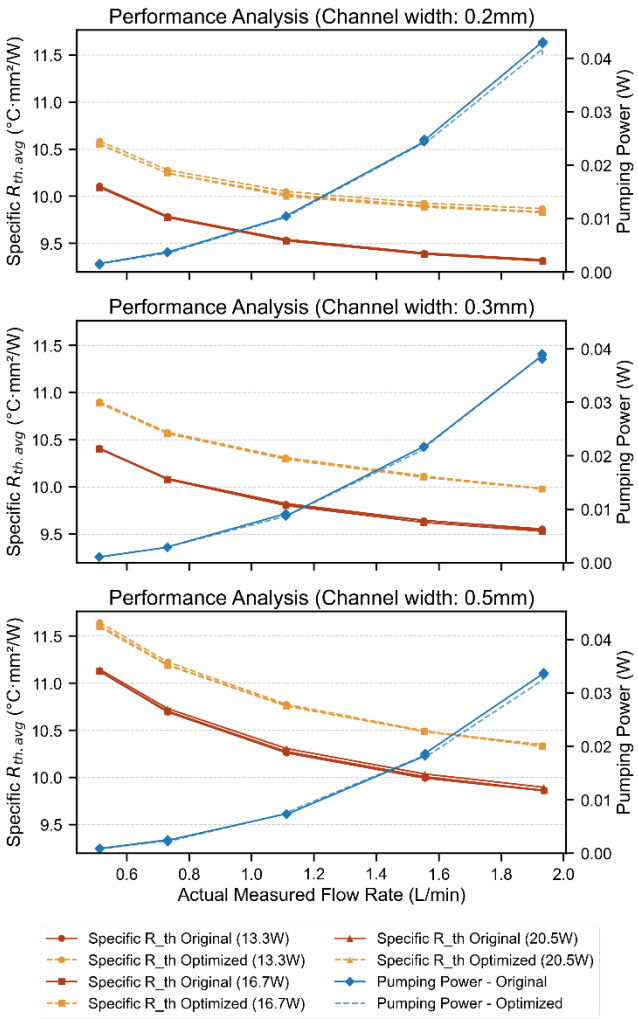

Fig. 9 Experimental performance comparison of the original and optimized manifolds across three microchannel configurations. The plots show (left-axis) specific average thermal resistance and (right-axis) required pumping power as a function of flow rate(bottom-axis).

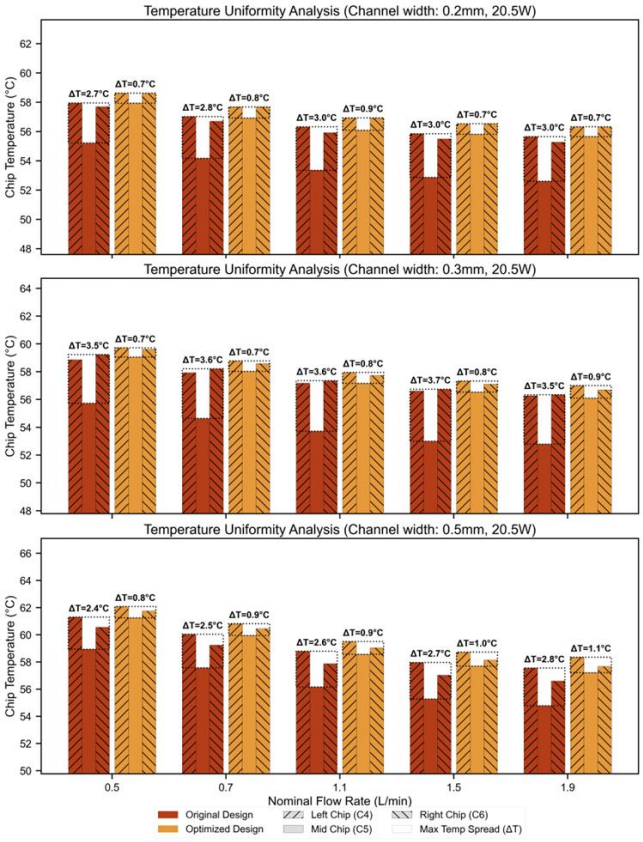

Fig. 10 Experimental validation of thermal uniformity improvement. The plot shows the measured steady-state temperatures for chips C4, C5, and C6 under a 20.5 W per-chip heat load with channel width of 0.2 mm, 0.3 mm, and 0.5 mm. The optimized manifold significantly reduces the maximum temperature difference $\Delta T_{\max}$ across all three microchannel geometries.

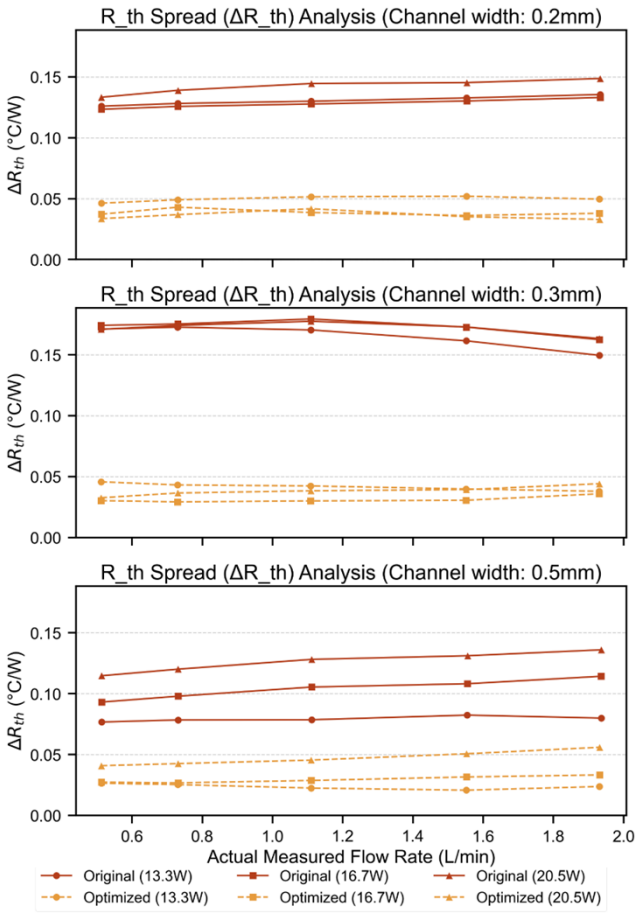

Fig. 11 Experimental analysis of chip-to-chip thermal resistance uniformity. The plot shows the thermal resistance spread ΔR_{th} as a function of flow rate for both original and optimized manifolds. Data points are presented for all three microchannel configurations (0.2 mm, 0.3 mm, 0.5 mm) across all tested power levels (13.3W, 16.7W, 20.5W per chip). The optimized design consistently demonstrates $\Delta R_{\text{th}} \approx$ 0.05 °C/W regardless of operating conditions.