In-Sensor Computing Realization Using Fully CMOS-Compatible TiN/HfO_x-based Neuristor Array

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ABSTRACT

With the evolution of artificial intelligence, the explosive growth of data from sensory terminals gives rise to severe energy-efficiency bottleneck issues due to cumbersome data interactions among sensory, memory, and computing modules. Heterogeneous integration methods such as chiplet technology can significantly reduce unnecessary data movement, however, they fail to address the fundamental issue of the substantial time and energy overheads resulting from the physical separation of computing and sensory components. Brain-inspired in-sensor neuromorphic computing (ISNC) has plenty of room in such data-intensive applications. However, one key obstacle in developing ISNC systems is lack of the compatibility between material systems and manufacturing processes deployed in sensors and computing units. This study successfully addresses this challenge by implementing fully CMOS-compatible TiN/HfO_x-based neuristor array. The developed ISNC system demonstrates several advantageous features, including multi-level analogue modulation, minimal dispersion, and no significant degradation in conductance (@ 125°C). These characteristics enable stable and reproducible neuromorphic computing. Additionally, the device exhibits modulatable sensory and multi-store memory processes. Furthermore, the system achieves information recognition with a high accuracy rate of 93%, along with frequency selectivity and notable activity-dependent plasticity. This work provides a promising route for affordable and highly efficient sensory neuromorphic systems.

The advancement of artificial intelligence (AI) and the Internet of Things (IoT) has resulted in a tremendous increase in the volume of data generated by complex sensory systems.[1,2] A substantial portion of this data is unstructured and contains redundant information. In order to facilitate efficient processing of this data in data-intensive applications, it is crucial to perform low-level sensory pre-processing tasks. These tasks involve selective extraction of valuable data by means of noise suppression, background extraction, filtering, feature enhancement, and other techniques.[3,4] This initial processing step allows for more effective high-level processing. In traditional von Neumann computing architectures, analogue sensory data must undergo analogue-to-digital conversion (ADC) in order to be processed. The converted data is then temporarily stored in memory before being transferred to local computation units or cloud-based systems for digital computations. However, due to differing functional requirements and manufacturing technologies, the sensory systems and computing units are physically separated. This physical separation introduces significant energy inefficiencies due to the complex data interactions required between the sensory, memory, and computing modules.[5,6]

In order to address the challenges posed by the physical separation of computing and sensory components, near-sensor computing architectures have been proposed. These architectures aim to position sensory devices at the outer edges of computer systems, primarily through the use of heterogeneous integration technologies such as planar system on chip (SoC), 2.5D/3D heterogeneous integration, chiplet, and others.[7,8] The objective is to enable the execution of specific computational tasks at the sensory terminals, thereby reducing unnecessary data communication. However, it is important to note that these technologies do not fundamentally resolve the energy efficiency and latency issues associated with the physical separation of computing and sensory components. To overcome these challenges, in-sensor-memory (ISM)

computing technology has emerged. This technology integrates sensing (S), memory (M), and computing (C) functions into a single device, eliminating the need for physical isolation. As a result, the interactive data transmission between SMC modules is greatly reduced, leading to substantial improvements in computing performance. Furthermore, the demand for next-generation computing systems requires the ability to perform an astounding 10^{18} ops/s.[9] Even if a supercomputer based on the conventional von Neumann computing architecture were capable of achieving this level of performance, it would consume an astonishing 20-30 MW of power and necessitate a powerful cooling system.[10]

The human brain, a remarkable system in nature, possesses extraordinary capabilities such as massive parallelism, robust fault tolerance, adaptability, and self-learning. These attributes enable the brain to effectively perform complex tasks. Notably, the power consumption of the human brain, despite carrying out approximately 10^{15} ops/s, is a mere 20 W, with the temperature maintained at around 37°C.[11,12] These remarkable features motivate the exploration of brain-inspired neuromorphic computing as a solution to the computing bottleneck encountered in conventional von Neumann computing architectures.[13] Traditional deep neural network (DNN) architectures based on silicon technology have extensively utilized standard 6T-SRAM bitcell arrays (BCA)[14] to facilitate neuromorphic computing. However, the inherent digital nature of these architectures limits their efficiency. To build highly efficient neuromorphic computing systems, analog processing becomes imperative.[15] In-memory neuromorphic computing, leveraging emerging memristor devices, has emerged as a promising approach.[16,17] These devices, characterized by two-terminal resistive switching memories, offer multiple analog resistance states, tunable biological-emulated characteristics, high symmetry and linearity, high speed, low

operation energy, small footprint, and scalability. Successful demonstrations of such in-memory neuromorphic computing have been reported.[18-25]

Numerous neuromorphic devices based on organic semiconductors, quantum dots (QDs), 2D materials, perovskites, and other emerging materials have been extensively reported in the literature.[26-34] These devices, however, often rely on interface/bulky traps for their functional mechanisms, which remain challenging to control. To advance the field of next-generation computing, it is crucial to explore the application of well-established semiconductor technology, such as Si-compatible materials (e.g., TiN, HfO_x). One of the significant challenges in building in-sensor-memory (ISM) neuromorphic computing systems lies in the domain of in-sensor (IS) computing, where material systems and manufacturing processes between sensory and computing units are incompatible. While there have been notable achievements in IS computing for image recognition,[35] the development of neuromorphic computing architectures for olfactory perception, sound localization, speech recognition, and tactile sensing is still ongoing.

In this study, we present fully COMS-compatible neuristors that offer enhanced scalability, processability, and efficient integration of bionic perception, such as nociception, and computation within a single device. This research demonstrates a promising homogeneous design strategy for affordable and efficient sensory neuromorphic systems, capable of multifunctional operations. By leveraging Si-compatible materials and advancing ISM technology, our work lays the groundwork for the future development of sensory neuromorphic systems with improved affordability, efficiency, and versatile capabilities.

RESULTS AND DISCCUSSION

Neuristor Fabrication and Sensory Function Demonstration

Sensation and perception are critical for survival and the initiation of intelligence. For instance, "tactile" allows us to evaluate contact parameters such as shape, surface texture, stiffness, and temperature. The realization of artificial perception holds the potential to greatly enhance the adaptability of existing electronic systems. Nociceptors, commonly known as pain receptors, serve the vital function of detecting noxious stimuli that could potentially lead to tissue damage. The similar sensory perception capacity of our TiN/HfO_x/HfTiON/TiN device to that of human sensory neurons was effectively demonstrated. **Figure 1(a)** illustrates the nociceptive process in the human body.[36] When the human body is exposed to noxious stimuli such as injury, heat, pressure, and others, an inflammatory soup is released, leading to an enhanced discharge of nociceptors located at the end of the axons of human sensory neurons.[37] When the intensity of a noxious stimulus surpasses the nociceptor's threshold, a response signal is generated by the nociceptor and transmitted to the spinal cord and motor neurons, activating avoidance behavior, specifically muscle contraction. **Figures 1(b) and 1(c)** display an optical image of our 6-inch wafer-scale

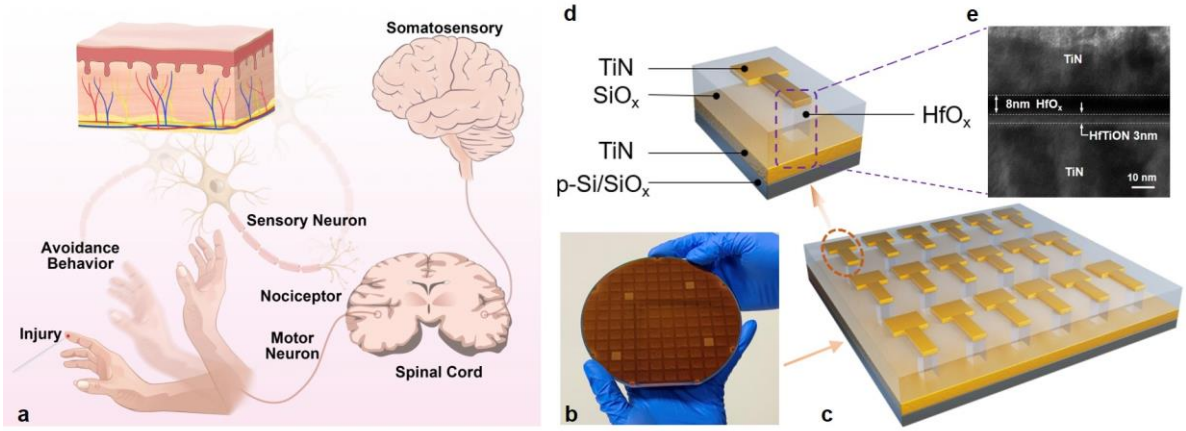

Fig. 1 (a) Schematic diagram of the human reflex. When a stimulus is received from the skin at the finger, action potentials in sensory neurons are sent to the gray matter of the spinal cord. Sensory neurons in the spinal cord make direct synaptic connections with motor neurons. If the signal is strong enough, it can trigger action potentials in the motor neurons, causing the hand-withdrawn reflex. In addition, the hand-withdrawn reflex is a spinal reflex whose reflex nerve center is located in the spinal cord but is still controlled by the higher central nervous system (brain). (b) Photograph of a 6-inch wafer with TiN/HfO_x/TiN neuristor arrays. (c) Schematic diagram of the memristive device array, which is a vertical structure. (d) Zoom-in view of the device, which consists of the HfO_x active layer and the SiO_x insulating region. (e) A cross-sectional high-resolution transmission electron microscopy (HRTEM) image of the TiN/HfO_x/HfTiON/TiN stacked structure.

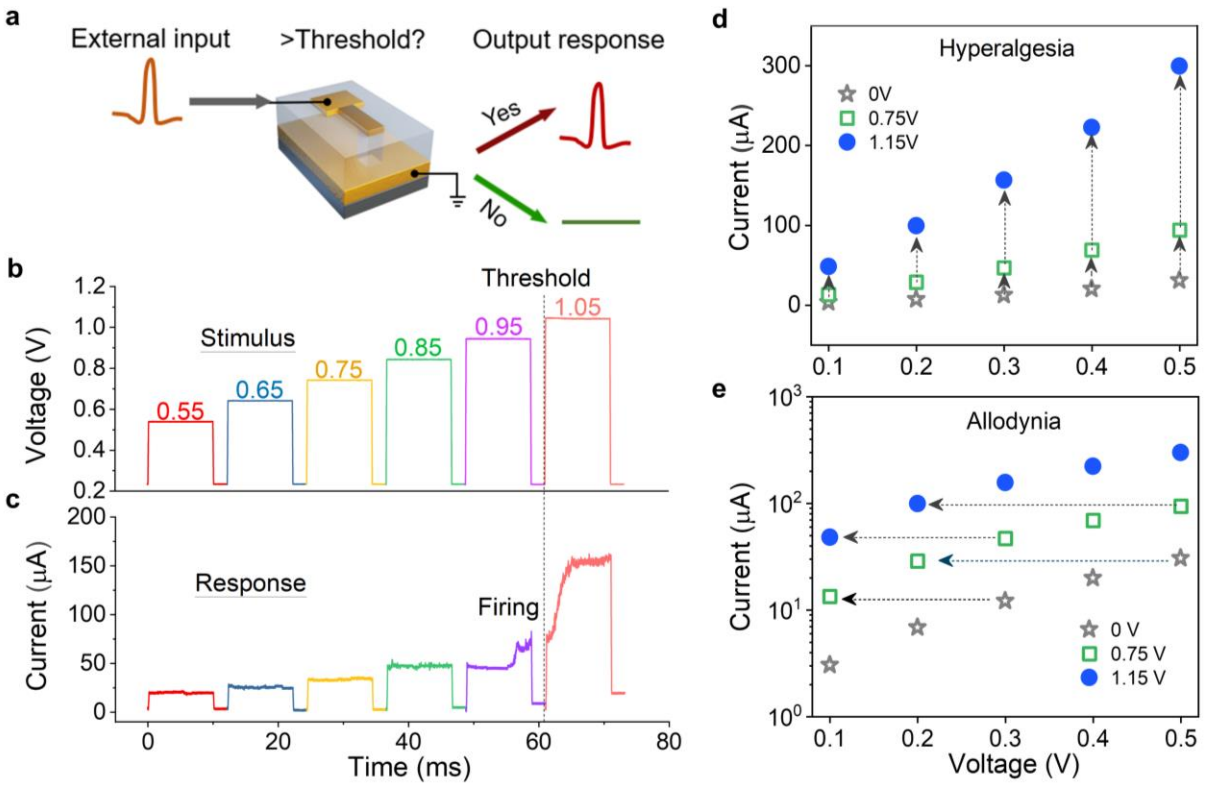

Fig. 2 (a) The working mechanism of the nociceptor in human system, and the threshold intensity-dependent electrical response in bionic devices. (b), (c) The threshold property of the nociceptive behavior is measured by varying the external electrical (pulse duration: 10 ms) intensity from 0.55 to 1.05 V. Demonstration of hyperalgesia and allodynia features. The maximum output current for different injury pulse amplitudes at (d) linear scale and (e) log scales. At the same injury pulse, the threshold voltage is shifted to a lower end and the current intensity is increased, simulating allodynia and hyperalgesia effects in a nociceptor.

electronic neuristor and a schematic diagram depicting neuristor arrays on the wafer, respectively. Additionally, **Figures 1(d) and 1(e)** provide a schematic diagram illustrating the structure of a discrete neuristor from the array and a high-resolution cross-sectional transmission electron micrograph showcasing the active region of the discrete device, which comprises an approximately 8 nm HfO_x layer and a bottom interfacial layer (IL) of approximately 3 nm in thickness. The bottom IL plays a critical role in the device's reliability by capturing and releasing oxygen ions in response to external stimuli. X-ray photoelectron spectroscopy analysis of the HfO_x layer (**Figure S1**, Supporting Information) reveals an Hf:O ratio of 1:1.6, indicating the presence of a non-stoichiometric (oxygen-deficient) layer. This oxygen-deficient layer is essential for facilitating fast

diffusion of oxygen ions within the oxide, enabling our neuristor to rapidly respond to external stimuli.[19]

The working principle of our electrical neuristor closely resembles its biological counterpart, as depicted in **Figure 2(a)**. When an external stimulus surpasses the threshold of the electrical neuristor, the device is triggered, resulting in the generation of an output current. This process mimics the human body's perception of pain when exposed to harmful stimuli.[38] Conversely, if the stimulus applied to the electrical neuristor falls below the threshold, the device remains in its original state, and no output current is generated, indicating that the external stimulus is not considered "harmful".[39] This threshold phenomenon results from the spontaneous rupture of the oxygen ions conductive filaments. **Figures 2(b) and 2(c)** demonstrate the generation of current in the device when various voltage pulses are applied. A significant output current can be observed at 1.05 V, indicating the full firing of the neuristor. These results validate the threshold-intensity characteristic of the electrical nociceptor. When the applied pulse is not sufficiently vigorous, the disconnection of conductive filament leads to a lower current. Conversely, if the amplitude of the applied pulse exceeds the nociceptive threshold, a higher current is observed. Additionally, **Figures 2(d) and 2(e)** exhibit other key sensitization features of an abnormal nociceptor, such as allodynia and hyperalgesia. Notably, the "injured" nociceptor subjected to noxious stimuli with high voltage amplitudes of +0.75 and +1.15 V produces a higher output current compared to the "uninjured" nociceptor (0 V), showcasing enhanced pain sensitivity to noxious stimuli, which serves to protect the damaged area from further injury.[36] The distinctions in the output current under three different states arise from the partial formation of oxygen-vacancies-rich filaments caused by the 0.75 V and 1.15 V pulses. Furthermore, the activation mechanism of the bio-nociceptor depends not only on the intensity (threshold) of the stimulus but also on its duration

and the number of repetitions.[40] Similar behavior is observed in our electrical nociceptors. The device is triggered after the 1st (or 5th) voltage pulse of 1.05 V (or 0.95 V) with a pulse width of 10 ms, as shown in **Figures 3(a) and 3(b)**, and a noticeable increase in output current is observed after post-triggering. This phenomenon can be attributed to the formation of oxygen-vacancies-rich conductive filaments within the active layer, connecting the top and bottom electrodes. It is worth mentioning that when the pulse width is reduced to 500 µs, the device is triggered only after the 12th voltage pulse of 0.95 V (**Figure 3(c)**). These findings indicate that as the pulse width narrows for a given voltage pulse amplitude, the number of voltage pulses required to trigger the device increases. The output current (or response intensity) remains steady or slightly increases with subsequent noxious stimul (**Figure 3(a)**), demonstrating a characteristic similar to the "no adaptation" property of bio-nociceptor.[41]

Analogue Memory Characteristic

Repeatable analog resistance switching, characterized by consecutive increases or decreases in current and the presence of multiple resistance states, was achieved over 80 DC switching cycles by sweeping the voltage positively from +0.60 to +1.15 V or negatively from −1.00 to −1.55 V in steps of +/-50 mV (**Figure 4(a)**). This characteristic clearly demonstrates that the conductance of

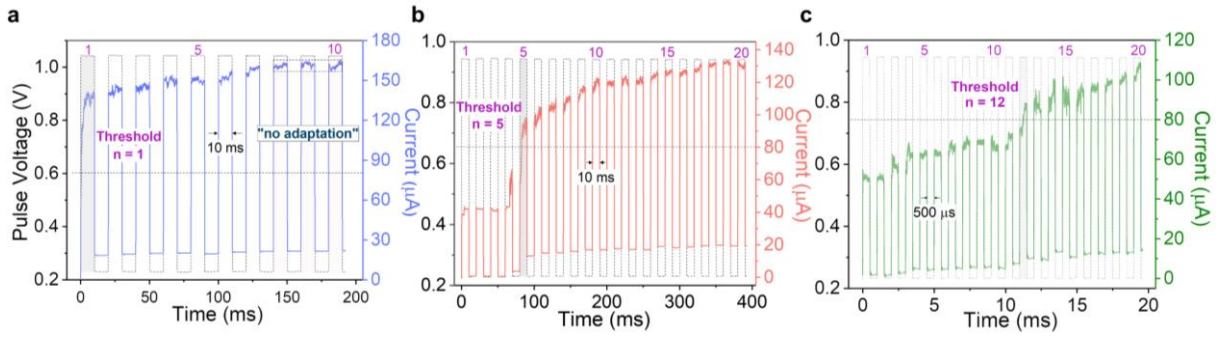

Fig. 3 A sequence of voltage pulses is applied to the as-fabricated device with amplitudes and pulse widths of (a) 1.05 V and 10 ms; (b) 0.95 V and 10 ms. Note that the former with 1.05 V is fired at the first pulse, while the latter with 0.95 V is fired only at the 5th pulse. (c) Compared to that in (b), activation is observed at the 12th pulse when the pulse width is reduced (i.e., 0.95 V, 500 µs). This indicates a dependence on the stimulus intensity and pulse width.

neuristors can be manipulated between low resistance states (LRS) and high resistance states (HRS) under different voltage polarities. The statistical endurance properties of the LRS and HRS (read at 0.1 V) are presented in **Figure 4(b)**, revealing stable and reproducible resistive switching with minimal dispersion over the first 500 pulse switching cycles at room temperature. While long-term memory retention tests spanning 10 years are impractical, shorter periods of a few hours or days measured at an elevated temperature of approximately 80°C are commonly employed to extrapolate the device's lifetime up to 10 years using an extrapolation method.[42] In our neuristor, no significant degradation of the memory window was observed at a high temperature of 125°C, as depicted in **Figure 4(c)**, indicating good thermal stability. Furthermore, the variability of switching voltage was characterized, along with the statistical distributions of the cycle-to-cycle (80 switching cycles in a device) and device-to-device (30 devices in an array distributed along a 6-inch wafer) set voltage (V_{SET}) and reset voltage (V_{RESET}), as illustrated in **Figures 4(d) and 4(e)**. The coefficient of variation (C_V), quantified by dividing the standard deviation (σ) by the mean value (μ) (absolute value), is found to be 13.5% and 4.4% (15.7% and 16.2%) for the cycle-to-cycle (device-to-device) variability of set and reset voltages, respectively. Although these values may be considered acceptable as standalone variability figures, it is possible to achieve further improvements in variability by incorporating additional peripheral architectures (e.g., 1T-1R structures). However, such enhancements would come at the cost of increased cell size and process complexity.[43] The cycle-to-cycle variability within a single device can be attributed to the stochastic nature of filamentary resistive switching, whereas the device-to-device variability is

primarily influenced by sample inhomogeneities arising from the fabrication process, including fluctuations in device area, thickness, and the presence of wrinkles, among other factors.

Significantly, the device not only exhibits an analog decrease in conductance but also an analog increase in conductance, as depicted in **Figure 4(f)**. This capability to progressively modulate resistance in both inhibition and potentiation allows for fully analog neuromorphic computing. Consequently, this eliminates the need for a one-transistor-one-resistive memristor (1T-1R) architecture, which is typically employed to modulate analog-like potentiation by controlling current compliance.[44] While it is feasible to modulate analog resistance in potentiation through analog programming within the 1T-1R architecture, this approach entails increased complexity in device fabrication and requires precise programming control accuracy due to the inherent stochastic nature of resistance switching in neuristors. The analog memory characteristics

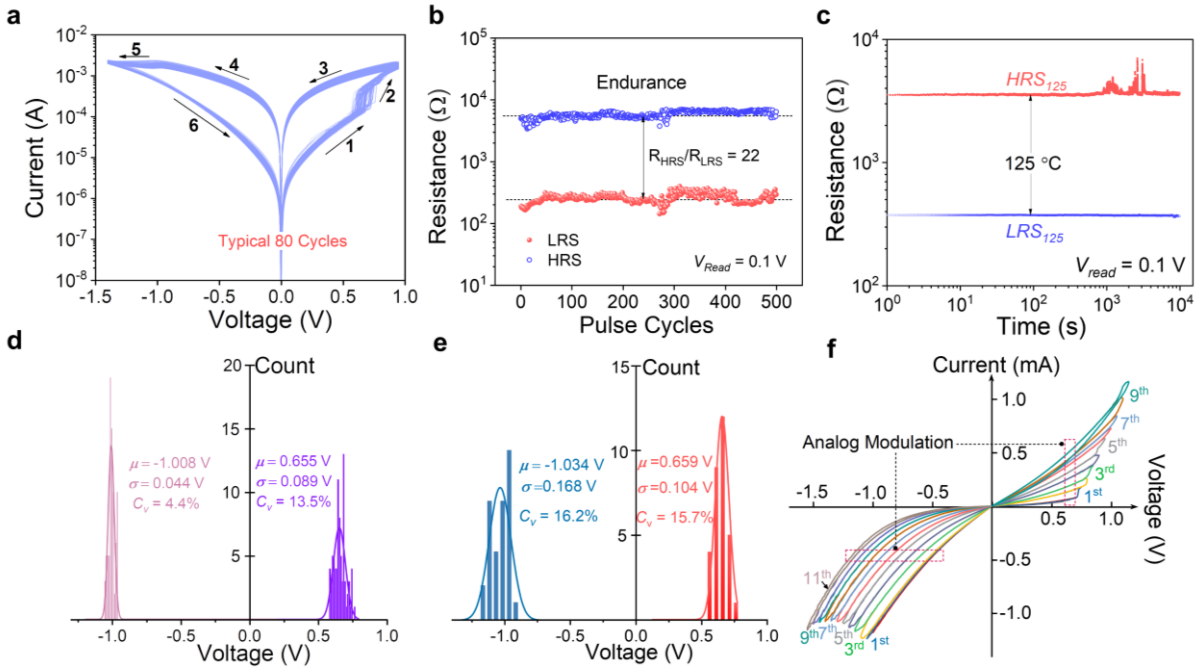

Fig. 4 (a) Representative current-voltage characteristics measured during 500 cycles in one single device. (b) Distribution of high and low resistance states of as-fabricated devices in 500 repetitive cycles. (c) Resistance–time curves measured at 0.1 V show the stable conductance states during high-temperature operation (120°C). (d) Cumulative distribution of device set voltages and reset voltages of 80 cycles in one device. (e) Cumulative distribution of device set voltages and reset voltages of 30 devices in on wafer. (f) Analog modulation characteristics of the bionic device. Current-voltage characteristics of the device during 9 consecutive positive and 11 negative sweeps.

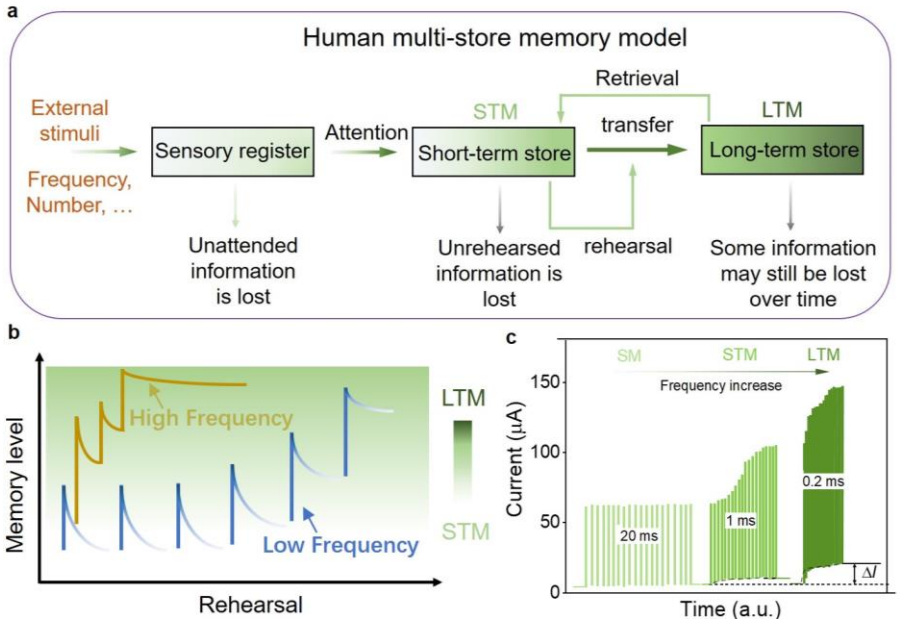

Fig. 5 (a) Schematic illustrations of the multi-store memory formation process in the human brain. (b) The schematic diagram of the multi-store model of memory represents the result that enough attention to enter short-term memory (STM) and a transition to long-term memory (LTM) by frequent rehearsal events. (c) STM to LTM transition in an as-fabricated device triggered by 20 consecutive external voltage pulses. Memory level as a function of pulsed voltage training intervals.

demonstrated in our neuristor make it possible to store analog sensory data and/or data after low-level processing directly in memory without the need for analog-to-digital conversion.

Neuromorphic Computing

The as-fabricated neuristor inherently enables the realization of multiple bio-realistic synaptic functions. In **Figure 5**, a multi-store memory model of the human brain is depicted, which consists of sensory memory, short-term memory, and long-term memory.[45] The neuristor was found to successfully emulate the sensory memory process, not only in the potentiation process shown in **Figure 5(c)**, but also in the depression process (**Figure S2**, Supporting information). Remarkably, after subjecting the neuristor to 3000 cycles of voltage pulses with a pulse width of only 300 ns, it exhibited reliable repetition of long-term potentiation (LTP) and depression (LTD) **(Figure 6(a))**. Additionally, we successfully simulated an essential temporal learning function known as paired-pulse facilitation (PPF), as illustrated in **Figure 6(b)**. PPF refers to a short-term synaptic plasticity process in which transmitter release is enhanced following two successive spaced stimulations.[46,47]

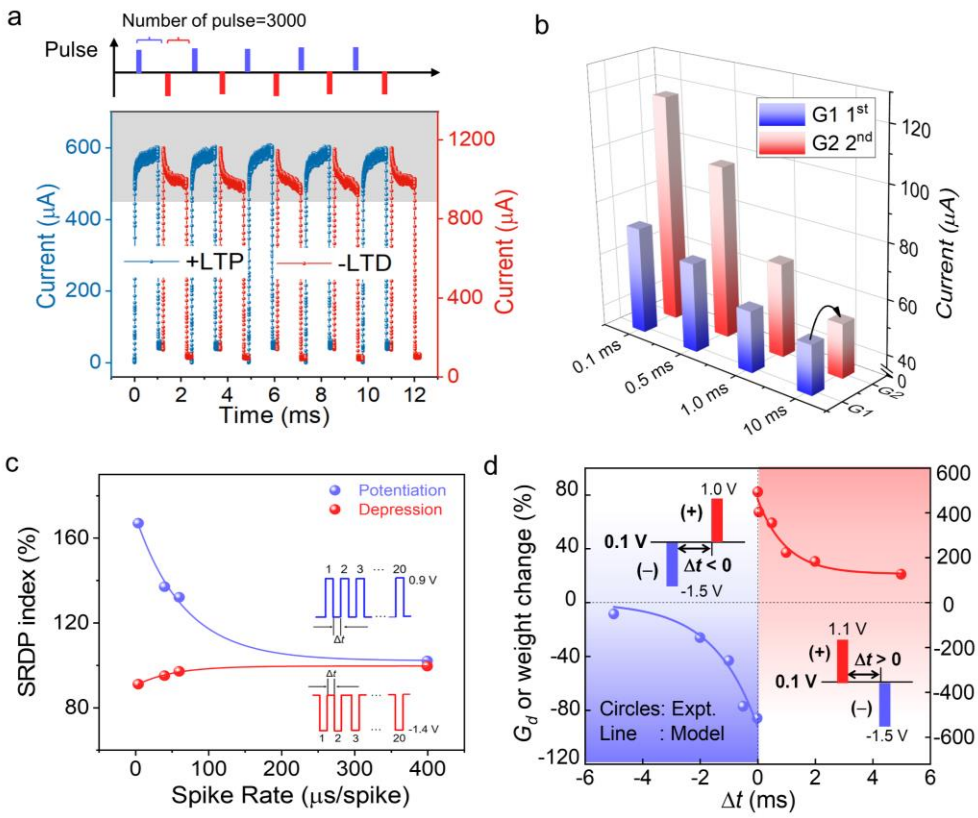

Fig. 6 (a) Reproducible multi-level operation of potentiation and depression in an as-fabricated device. The potentiation of the device is achieved using a 1.1 V/300 ns pulse, and the depression process is produced using a −1.5 V/300 ns pulse. (b) Paired-pulse facilitation of a synapse. The change in device current, induced by two consecutive training pulses under different spiking intervals with a pulse width of 1 ms. Current change increases with decreasing pulse interval. (c) Excitatory/Inhibitory PSC change (%) induced by a train of external pulses (0.9 V/−1.4 V, 100 μs, with intervals of 4, 40, 60, 400 μs) with 0.1 V bias to read the device state, suggesting that higher pulse frequencies result in a more prominent accumulation effect. The fitting lines are approximated by an exponential function. (d) Spike-timing-dependent plasticity behavior implemented using two opposite-polarity voltage pulses pair at the top electrode. Weight change (%) as a function of the relative timing between two pulses.

PPF plays a role in temporary information recognition and decoding within the biological nervous system. When applying a pair of voltage spikes (0.9 V, 1 ms) with varying spike time intervals between the two consecutive pre-synaptic spikes, we observed a clear increase in the post-synaptic current triggered after the second pre-synaptic spike compared to the first pre-synaptic spike. The difference in post-synaptic current diminishes as the time interval increases.

Moreover, synaptic response in biology exhibits inherent frequency selectivity known as spike-rate-dependent plasticity (SRDP), which is considered a conventional learning protocol.[48] SRDP is characterized by the dependence of post-synaptic current (conductance) on stimulus

spiking rate (interval). In our device, we observed SRDP, where synaptic plasticity was enhanced with shorter time intervals during both the potentiation process (+0.9 V) and depression process (-1.4 V). This enhancement was quantified by the gain of synaptic currents (SRDP index: $A_{20}/A_1 \times 100\%$), as depicted in **Figure 6(c)**. The detailed relationship between synaptic plasticity and pulse interval is illustrated in **Figure S3**, showing enhanced synaptic plasticity for 20 consecutive pulse signals with shorter time intervals.

Another important activity-dependent plasticity observed in chemical synapses is spike-timing-dependent plasticity (STDP), which captures the neuromorphic learning and memory processes by adjusting the connection strength between pre-synaptic and post-synaptic neurons based on the relative timing of input and output action potentials, following the Hebbian rule.[49] In neurobiology, the temporal relationship between spikes is encoded locally, e.g., facilitated by the natural decay of Ca^{2+} levels, which serves as an internal timing mechanism. To replicate STDP in hardware, employing similarly straightforward, non-overlapping pre- and post-synaptic pulse pairs, it is essential to incorporate a intrinsic timing mechanism within the synaptic element. The diffusion kinetics of oxygen ions in our neursitor provide a feasible solution to establish this required timing mechanism. The nature of the conductance depends on the sequence of the pre- and post-synaptic pulses. LTP is triggered when the pre-synaptic pulse precedes the post-synaptic pulse ($\Delta t > 0$), while LTD is triggered when the post-synaptic pulse precedes the pre-synaptic pulse ($\Delta t < 0$) (**Figure S4**). Notably, the current responses in LTP and LTD exhibit a consistent correlation with the interval timing in the applied pulse pair, as characterized by the STDP index shown in **Figure 6(d)**, where the resulting output current values decrease with increasing interval timing between pre- and post-synaptic pulses. It is worth mentioning that the STDP learning process was successfully reproduced by simple pulse manipulation, where non-overlapping pre-

and post-synaptic pulse pairs were applied to our neuristors to emulate the natural timing mechanisms in biological systems. This approach without complex pulse engineering or spike overlapping greatly reduces the complexity of peripheral circuitry and algorithm design, offering energy-efficient operation. Additionally, it is noteworthy that reducing the pulse width and amplitude is expected to bring about a corresponding decrease in the relaxation time,[50] which can therefore lead to a reduced time gap Δt during the STDP and foster an increase in the training speed.

Finally, the pattern recognization function of the neuristor was implemented. The post-cropped MNIST handwritten digit images (20×20 pixels) were used as input image data, and a modeled 2-layer multilayer perceptron (MLP) crossbar array served as the performance benchmark (**Figure 7(a)**). The network topology consisted of 400 input signals (400 input neurons corresponding to binarized 20×20 image elements), 100 hidden neurons, and 10 output neurons for predicting the standard digital output.[51,52] Based on the above model, the recognition capability was computed using a dataset comprising 60,000 training images and 10,000 test images, with a batch size of 64 per epoch. As shown in **Figure 7(b)**, a high recognition accuracy of 93% was achieved after 125 training epochs, demonstrating performance on par with other relevant

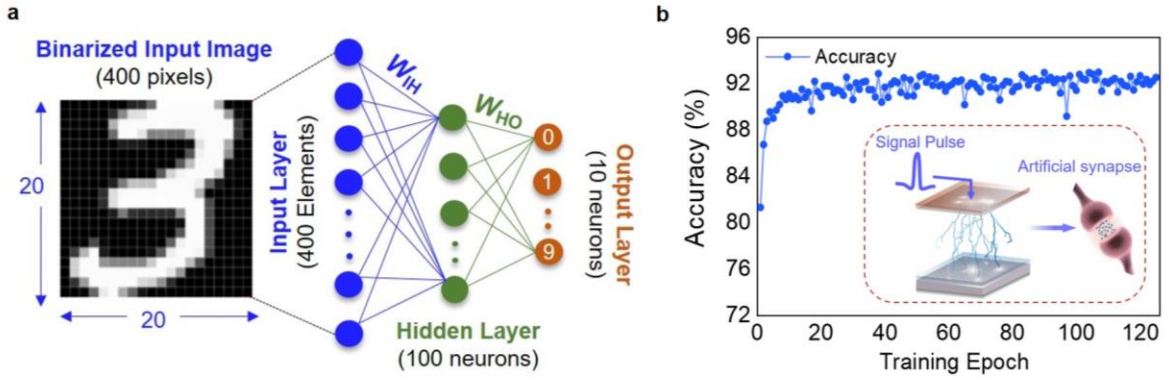

Fig. 7 (a) Schematic illustration of a three-layer neural network for the classification of MNIST handwritten digits. A 20×20 pixel handwritten digital image dataset is used for the training and testing process. (b) Evolution of pattern recognition accuracy as a function of training epochs, where the as-fabricated devices function as analog synapses designed for weight updating.

memristive convolutional neural networks.[53,54] Moreover, this accuracy approached the high level of 94.1% obtained from an ideal synapse, highlighting the efficacy of the proposed neuristor.

CONCLUSION AND OUTLOOK

In summary, this work implements stable and reproducible in-sensor neuromorphic computing based on TiN/HfO_x neuristors, extending Si technology to next-generation computation, a crucial step towards cognitive integration in artificial intelligence systems. All materials in the device are already deployed in the current CMOS process. Our neuristor exhibits multi-level analogue modulation, small dispersion, and no significant degradation in conductance at a high temperature of 125°C. The behavior of bio-nociceptor, modulatable sensory and multi-store memory processes are well imitated in as-fabricated neuristor. Furthermore, we demonstrate highly accurate information recognition, sensitive frequency selection, and significant activity-dependent plasticity by simple non-overlapping pre- and post-synaptic pulse manipulations (emulating natural timing mechanisms). Our results envision that TiN/HfO_x-based neuristors can be attractive candidates for the fabrication of in-sensor neuromorphic computing using current Si technologies, since smart peripheral sensing systems and high-performance computing systems can be achieved on exactly the same active material and process platform.

Artificial perceptual system based on neuromorphic devices is still in their early stages as many challenges should be addressed before fully unlocking the advantages. For instance, the current limited understanding of the underlying biological processes necessitates the development of functional devices that closely resemble biological counterparts. Another pivotal challenge stems from achieving universality. Incorporating computing in sensing demands significant

modifications in processing steps, thereby impacting integration density, particularly in image-sensing applications. Large-scale, low-cost, and reproducible technologies with universally applicable protocols need to be developed for practical applications. Moving ahead, this exciting topic requires further study to bridge the gap between artificial perceptual intelligence technology and the well-established Si industry.

METHODS

Device fabrication

The fabrication flow of our neuristor is given in **Figure S5** (Supporting Information). An around 450 nm SiO_2 isolation layer was first deposited by chemical vapor deposition (CVD) process on Si substrate. A 150 nm TiN bottom electrode was then prepared by DC reactive magnetron sputtering of a Ti target in a mixture of N_2 and Ar gases with the flow rate of 30 and 8 sccm, followed by CVD of SiO_2 with a thickness of 160 nm to serve as the passivation layer. After active area definition (UV lithography and reactive-ion-etching), the wafer was loaded into an atomic layer deposition (ALD) system (Cambridge Nanotech Savannah S200) for HfO_x layer growth at a temperature of 250^oC and a pressure of 0.2 Torr. The precursor was tetrakis (dimethylamino) hafnium and the oxidizing agent was H_2O. After the deposition of top TiN electrode (~ 70 nm) using the same process as that for top TiN electrode, patterning via UV lithography and reactive ion etching was carried out again to form the devices.

Characterization and device measurement

High-resolution transmission electron microscopy (HRTEM) of the active region of the test device shows ~8 nm HfO_x layer and a ~ 3 nm bottom interfacial layer (IL). The memristor sample was prepared using focused Ga ion beam (FIB, FEI Helios 450s) at 30 kV, followed by thinning (to ~ 70 nm) and cleaning at 2 kV beam energy. X-ray photoelectron spectroscopy (XPS) analysis was carried out on separately prepared test samples with a 8-nm HfO_x blanket-deposited over a Si substrate in Thermo Fisher Scientific Theta Probe system equipped with monochromatic, micro-focused Al Kα (1486.6 eV) X-ray source and a hemispherical electron energy analyzer. DC/pulsed (with PMU module) voltage-sweep testing was carried out at room (or 125 ^oC) temperature using a Keithley SCS4200/Agilent B1500A parameter analyzer. The area of test devices are $50 \times 50\ \mu m^2$. Electroforming with a current compliance of 5 mA was performed to achieve a resistive switching effect in our neuristors.

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Competing Interests

The authors declare no competing financial interest.

ASSOCIATEDCONTENT

Supplementary Information

Supporting Information Available: The following files are available free of charge.

Details about the supporting figures S1-S5.

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