Sub-0.5 µm Pitch Scaling of W2W Cu/Dielectric Hybrid Bonding

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***Abstract*— Hybrid bonding, a crucial technique in heterogeneous package integration, holds immense potential for advancing pitch scaling in semiconductor technologies. As three-dimensional (3D) nodes continue to progress, the exploration of novel materials and processes becomes imperative. This study focuses on the investigation of optimal dielectric combinations to maintain wafer integrity during bonding, aiming to achieve higher bond strength with alternative dielectrics limited to thicknesses of a few tens of nanometers. Moreover, the exploration and quantification of the minimum effective bonding area required for conventional oxide dielectrics are essential for successful fusion bonding. In this research, we employed a damascene process sequence to fabricate sub-0.5 µm pitch Cu/dielectric hybrid bonding at the wafer level. Various optimizations were emphasized, including test vehicle design and fabrication processes. Surface and interface analysis techniques were employed to scrutinize critical process steps such as post lithography, etching, electrochemical deposition (ECD), chemical mechanical planarization (CMP), and bonding overlay adjustments, aiming to realize sub-0.5 µm pitch wafer-level Cu/dielectric hybrid bonding. Our findings provide insights into advancing pitch scaling in heterogeneous package integration through meticulous material selection and process optimization.**

Keywords*— *Cu/dielectric hybrid bonding, Fine-pitch, Dielectric stack

I. Introduction

The evolution of electronic devices from cumbersome mainframes to sleek handheld gadgets has been greatly influenced by Moore's Law [1]. This is the prediction that the number of transistors on a microchip will double approximately every two years, driving exponential growth in computing power. This prediction has largely held since its inception in 1965, leading to the miniaturization of computing devices and the development of portable electronics. As technology has advanced, users' expectations have also evolved. Today's consumers demand electronic systems that not only offer enhanced performance but also integrate seamlessly into their lives, making daily tasks more efficient and enjoyable. This demand has led to a focus on improving power efficiency and reducing form factors while maintaining or even enhancing computational capabilities. Users expect their devices to be faster, longer lasting, and more compact than ever before [2].

However, achieving these goals solely through traditional device scaling methods has become increasingly challenging [3]. The limitations of dimensional scaling, such as heat dissipation and signal interference, pose significant barriers to further miniaturization. Moreover, simply shrinking components does not address the need for additional functionalities or larger form factors in some applications. Consequently, exploring alternative approaches to meet these evolving demands, includes innovations in materials science, novel device architectures, and advanced manufacturing techniques [4].

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Three-dimensional (3D) heterogeneous integration has revolutionized system-in-package (SiP) integration, allowing for compact designs with enhanced signal integrity and improved power efficiency [5]. Higher interconnect density enables faster communication between different parts of a chip, facilitating rapid processing and improved performance. This advancement is essential for meeting the demands of modern applications such as artificial intelligence, big data analytics, and high-performance computing. Moreover, as devices continue to shrink in size, achieving higher interconnect density becomes increasingly challenging, requiring innovative solutions in materials science, circuit design, and manufacturing processes. Ultimately, higher interconnect density plays a crucial role in pushing the boundaries of electronic innovation, enabling the development of more powerful and versatile electronic systems.

Hybrid bonding, whether at the chip level or wafer level, is increasingly recognized as a promising approach for realizing higher interconnect densities [6]. Here, the initial bonding of dielectrics across the bonding interface at room temperature is a critical step in ensuring the integrity of bonded wafers, especially at high densities and ultrafine pitches. Conventional dielectric materials often lack sufficient interface bond strength without annealing at elevated temperatures, necessitating further research into new materials to enhance interfacial bonding strength during initial wafer bonding at room temperature [7,8]. Moreover, as the pitch size decreases, the bonding overlay becomes crucial in guaranteeing sufficient dielectric contact area [9]. Designing appropriate pads becomes essential for ultrafine pitches, and the role of chemical mechanical polishing (CMP) is significant in fine-tuning the dielectric corner rounding. Additionally, controlling dishing becomes paramount as the pitch decreases, as maintaining a sufficient metal pad volume to ensure reliable metal-metal contact formation poses a critical process challenge [10]. Uncontrolled dishing could exacerbate difficulties in achieving reliable contact formation, particularly as pitch sizes shrink.

In such an aspect, this paper investigates the challenges associated with sub 0.5 µm pitch wafer level bonding interconnect realization and appropriate solutions. In the following sections a detailed investigation of dielectric selection, its effect on bonding interface with possible higher pattern density/ lower effective boding area, and interconnect pitch design concerning bonding overlay considerations. Following, the challenges associated with the damascene process and bonding overlay optimization to achieve a sub 0.5 µm pitch bonding at the wafer level have been discussed in detail.

II. Material Processing, Fabrication Protocol and Pattern Design

The 300 mm process line toolset has been utilized in the entire experimental demonstration. A 300 mm diameter, p-type (100) silicon wafers with double-sided polished substrates have been used for processing. The wafer surface for Cu/dielectric hybrid bonding has been fabricated using the damascene process, as shown in schematic Fig. 1(a-h). The various process layers were fabricated by following the damascene process, here the dielectric layer deposition was done by using the PECVD process. Following, photoresist (PR) coating and pattern development using TEL track and exposure using Nikon Immersion scanner tools. Afterward, the Inductively coupled plasma (ICP) etch tool was used for the etch mask, followed by dielectric layers etching, followed by an in-house PR stripper for PR removal on the dielectric. Afterward, the PVD process was used for the barrier and Cu seed layer respectively, and electrochemical plating was performed using the ECP tool. The resulting Cu overburden followed by barrier layer removal was performed by using the CMP tool with an endpoint detection mechanism. After CMP, the resulting Cu to dielectric topography assessment was carried out using atomic force microscopy (AFM) – InSightAFP by Bruker. After obtaining the required surface with minimal dishing and lower corner rounding, the bonding process with precise alignment was carried out using the EVG Gemini FB XT tool. Fig 1(g and h) shows the wafer-to-wafer hybrid bonding process. The bonded wafers are annealed at high temperatures of ~350 ˚C for 2hr, to enhance the dielectric bond strength and make the Cu-Cu interconnections. Afterward, for interface inspection, c-mode

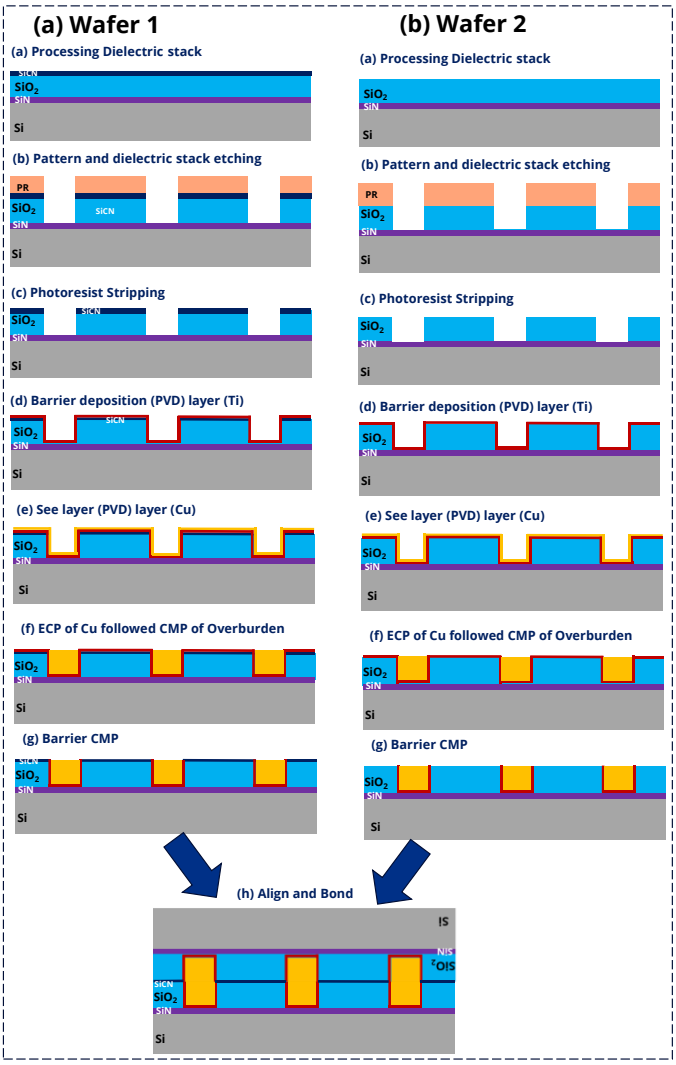

Fig. 1. Schematic of the damascene process for Cu/dielectric hybrid bonding surface fabrication. (a). With SiCN ultrathin dielectric on the conventional dielectric stack. (b). The conventional process.

acoustic microscopy (C-SAM) for wafer level voids and bonding interface quality a focused ion beam scanning electron microscopy (FIB-SEM) has been utilized.

A. *Design of Test structures*

Sub-micron interconnectivity between chipsets necessitates the representation of appropriate manufacturing process technology using industry-standard Computer-Aided Design (CAD) / Electronic Design Automation software for design enablement. CAD software tools are used to prepare the layout design with test structures for the hybrid bonding process flow. Based on the test vehicle, a comprehensive list of layers aligned with the process and design team compiled in layer map and display files in software, encompassing their functions such as serving as conductors, vias, or dielectrics. Layer Stack-up is captured in software characterized by material attributes such as conductivity or dielectric constant. Layout with various test structures of sub-0.5u pitch like Daisy Chain, Kelvin, Comb, and so on with pad, bond internal dimensions (like diameter 120nm,240nm), and inter structure dimensions (like pitch 460nm) specifications are aligned with process and design teams. To meet density requirements, dummy pads are included. Bonder alignment is critical for hybrid bonding; hence design rules are extensively checked with IC standard physical verification software in the design environment before fabrication. The density of the set of layers in the layout with dummy pads is estimated with software to analyze requirements for mechanical stability.

III. Results and Discussion

As discussed, wafer hybrid bonding involves joining two semiconductor wafers by creating strong and reliable bonds between them, enabling the integration of different materials and functionalities onto a single chip. The choice of dielectric material used in this bonding process is critical for achieving high bond quality, ensuring electrical isolation between layers, and enhancing thermal and mechanical stability [11]. A strong requirement towards the optimal dielectric layers for higher interface bond strength at higher pattern densities.

A. *Dielectric stack optimization*

In hybrid bonding, initial bonding occurs among dielectrics through weak hydrogen bonding among surface dangling bonds rather than within the bulk of the film. Ultrathin layers of new dielectrics are utilized to optimize dielectric interfaces. Various ultrathin dielectrics such as SiCN, HfO_2, SiN, and Al_2O_3 are applied at both the TEOS and bonded wafer levels, individually and in combinations, as depicted in schematic Fig 2(a).

One advantage of incorporating ultrathin dielectrics in the conventional damascene process is achieving enhanced bond strength without inducing higher interlayer stresses, from our previous work [12]. Many bonding combinations have shown a higher interface bonding quality of >85%, quantified from resulting C-SAM images. However, bonding strength remains a critical requirement as it directly influences the mechanical strength of bonded wafers. Maszara's blade test [13] is utilized for measuring bond wafer strength. Fig. 2(c) illustrates the resulting bond strengths among wafers with various ultrathin

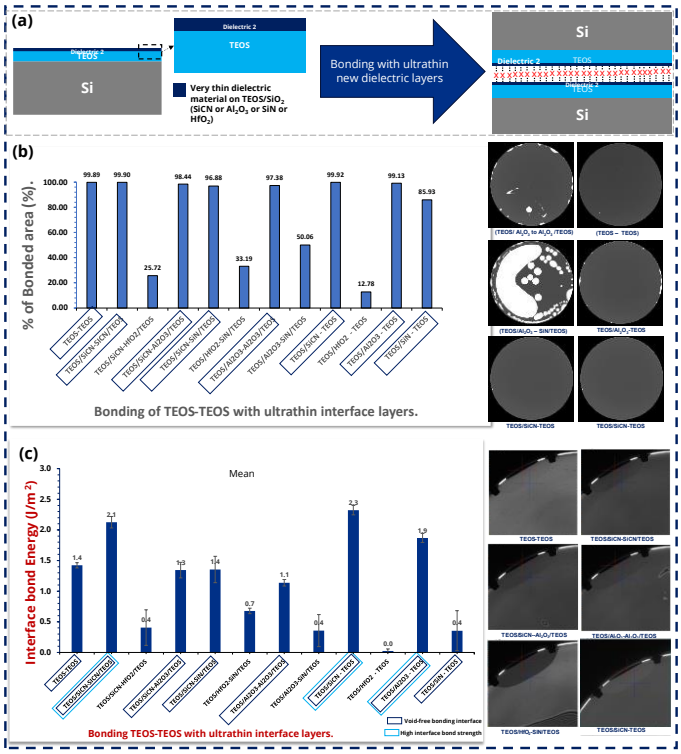

Fig. 2. (a) Schematic of ultrathin new dielectric layer introduction for wafer bonding. (b). The percentage of bonding area concerning the various bonding combinations, inspected by C-SAM shown on the right side. (c). Interface bonding energy for various bonding combinations was measured using Maszara's blade test, a measurement shown on the right side.

layer combinations on TEOS – TEOS surfaces, suggesting that the bonding interface combination of TEOS – SiCN exhibits higher bond strength than all other combinations. Despite literature reporting that SiCN-SiCN forms the stronger bonding interface [13-16], TEOS-SiCN was found to be superior.

The further investigation involves X-TEM analysis conducted at the bonding interfaces of TEOS/SiCN-SiCN/TEOS and TEOS/SiCN-TEOS, as shown in Fig. 3 (a) and (b) respectively. A good correlation was observed with existing literature on the SiCN-SiCN bonding interface, which forms an ultrathin SiO_2 interlayer, confirmed by EELS analysis [14]. However, at the TEOS/SiCN-TEOS bonding interface, an increased carbon concentration was detected at the bonding interface through EELS inspection. This suggests that an ultrathin interlayer of SiCN between TEOS layers could effectively manage water molecules by forming a carbon-rich interlayer, consequently leading to higher bond strength.

B. *Wafer bonding study with the bonding area*

In exploring the minimum bonding area necessary for successful bonding, the experiments were conducted with various pattern densities. Bonding was conducted without any additional interlayers aside from TEOS. Pattern densities with effective bonding areas ranging from 83.4% to as low as 18% were tested. It was observed that the bonding area <18% presented challenges such as delamination or wafer slide-off. This suggests that conventional dielectrics with an effective bonding area of approximately 20% are adequate to retain the

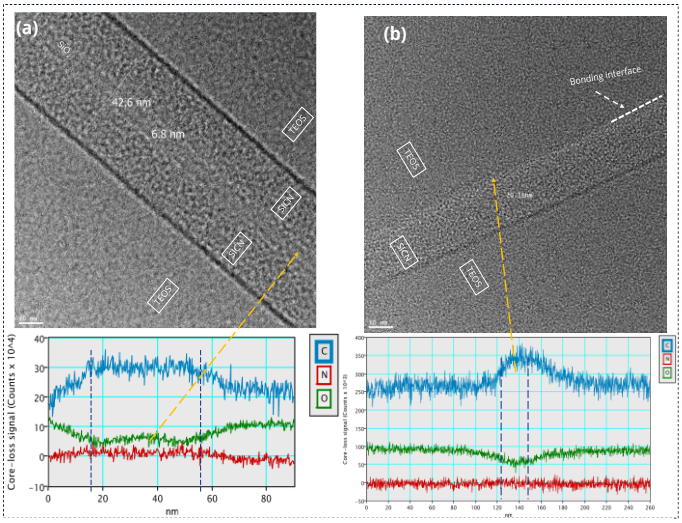

Fig. 3. Cross-sectional TEM and respective EELS inspection of the bonding interface with ultrathin new dielectric layers. (a). TEOS/SiCN-SiCN/TEOS. (b) TEOS/SiCN-TEOS.

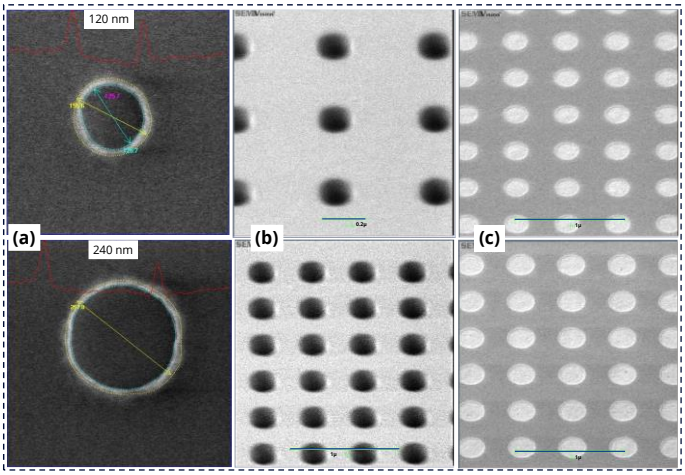

Fig. 4 Surface inspections of the sub-0.5um pitch bonding surface. (a). CD-SEM of 120nm and 240nm CD. (b). DR-SEM inspection of fabricated patterns after etching. (c). DR-SEM inspection after the polishing of Cu overburden.

wafers after plasma treatment followed by wafer hybrid bonding. Similarly, by ensuring that the overall district contact area of hybrid bonding surfaces encompasses at least 20% bonding area, achieved through optimal CMP for lower dielectric rounding, and overlay tuning, could potentially increase the Cu pattern densities to higher than 80% for future hybrid bonding. It suggests a conventional TEOS dielectric bonding could be sufficient for the lower pattern densities with bonding overly tolerances making the overall effective bonding area at least 20%.

C. Wafer preparation for sub-0.5 µm pitch.

According to Fig. 1, the hybrid bonding surfaces have been prepared using the damascene process sequence. The dielectric thickness has been carefully selected through the CMP process, incorporating appropriate stopping layers to facilitate dry etching while ensuring the wafer warpage remains below 50 µm. Design pattern transfer has been executed using an immersion tool, with pattern dimensions of approximately 120nm and 240nm, with a pitch of 460nm. CD inspection of post-photoresist development surface has been conducted using the CD-SEM tool, as illustrated in Fig. 4(a). Following pattern transfer, wafers undergo dry etching with optimized process parameters, followed by in-situ resist stripping. Etched patterns are then scrutinized using the DR-SEM, as displayed in Fig. 4(b). These patterns are subsequently filled with ultrathin Ta barrier and thin seed layers of Cu for electroplating. It was observed maintaining the wafer level uniformity of the Cu overburden helps in achieving the uniform removal of Cu at CMP without leftover on the surface. Subsequently, the wafers undergo CMP polishing, initially with a Cu overburden followed by Ta barrier layers, utilizing the CMP process, Fig. 4(c), depicts the DR-SEM inspection of the polished surface. It was observed maintaining the wafer level uniformity of the Cu overburden helps in achieving the uniform removal of Cu at CMP without leftover Cu islands on the surface.

In addition, the surface properties significantly impact the initial bonding of wafers at room temperatures. These include surface roughness, Cu to dielectric dishing, and dielectric corner rounding which are critical parameters for investigation. AFM investigations have been carried out to assess surface topography. Fig. 5(a) illustrates the Cu dishing values observed for both 120nm and 240 nm pad sizes. The optimized CMP process yields dishing values on the order of approximately $\leqslant$ 1nm $\pm$0.5nm, and an overall surface roughness of < 0.3nm / 4µm^2 area, with a surface including both oxide and Cu pads. Additionally, Fig. 5(b) and 5(c) portray the 3D surface topography and corresponding line maps inspected across the pattern surface. The line map also indicates the presence of dielectric corners rounding to very low from the observation.

D. Interface inspections.

The Cu/dielectric hybrid bonding process between the wafers is carried out immediately following N2 plasma treatment, followed by precise alignment adjustment using various parameters of the bonding tool, such as adjustments to bow and zone pressures. The bonding interface of the post-bonded wafers is examined non-destructively using the C-SAM method, as depicted in Figure 6(a). Upon inspection, a non-bonded region was detected, as mentioned in the figure. To validate the reliability of the bonded interface, these wafers underwent dicing to a die size of 10mm × 10mm. It was observed that no chips were detached except at the non-bonded region identified during the C-SAM inspection. This could be correlated with the air trap while bond wave propagation. Upon the dicing, the diced samples are inspected at cross-section for the bonding quality assessment using the FIB-SEM inspections. Fig. 7 (a) and 7(b) show the interface inspections of the hybrid bonded wafers with a 240nm pad with a pitch of ~460nm with optimal alignment accuracy at the wafer center and with a wafer edge of ~<130nm of misalignment.

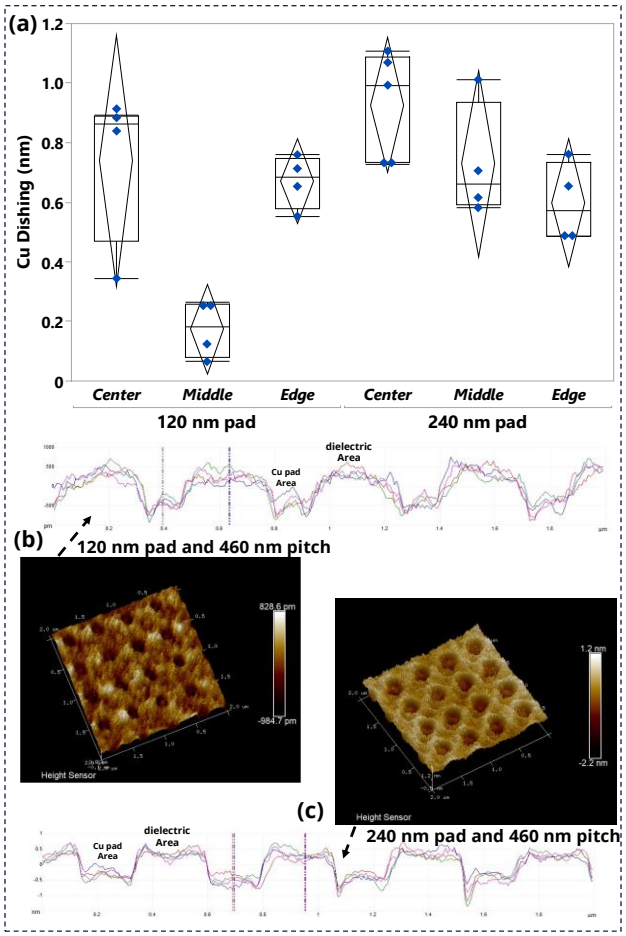

Fig. 5 Surface inspections of the hybrid boding surface using AFM. (a). CD-SEM of 120nm and 240nm CD. (b). DR-SEM inspection of fabricated patterns after etching.

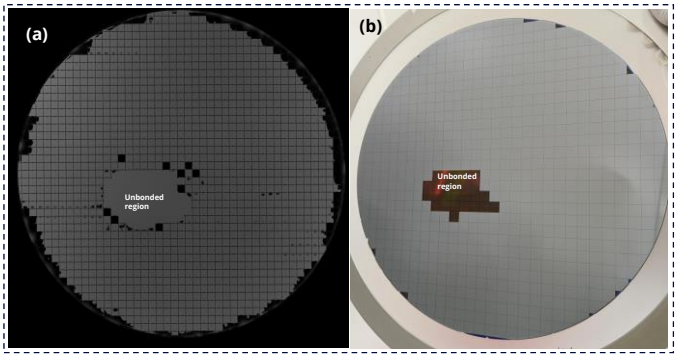

Fig. 6 (a). Annealed post-bond wafer interface inspection using C-SAM. (b). The dicing of the same hybrid bonded wafer of die size of 10mm X 10mm.

IV. Conclusions

This endeavor demonstrates the investigation delved into the influence of novel dielectric materials, with thicknesses limited to a few tens of nanometers, on the strength of wafer bonding and the minimum effective bonding area required to maintain wafer integrity. Our findings revealed that a TEOS-

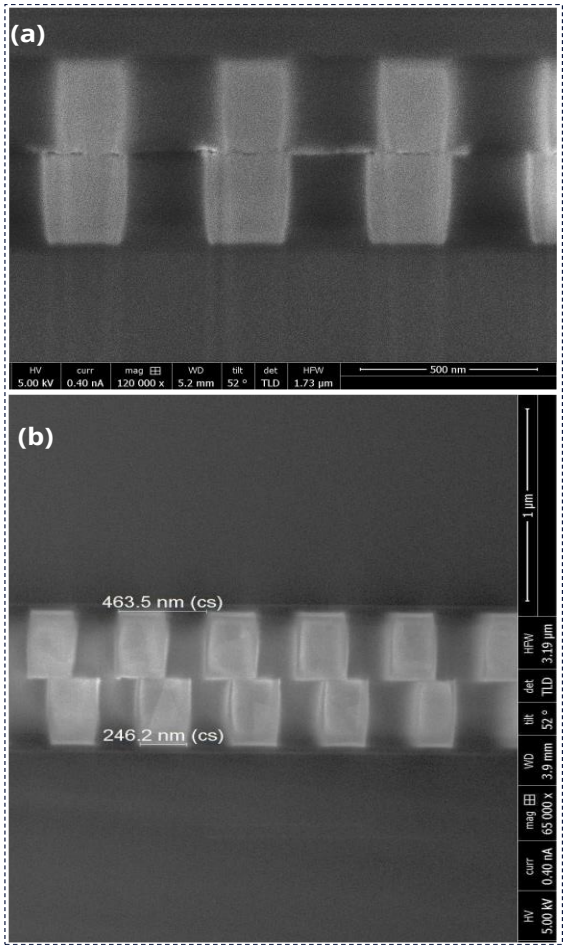

Fig. 7. X-SEM interface inspection of the Cu/dielectric hybrid bonded interface. (a). at the center of the wafer. (b). at the edge of the wafer.

SiCN bonding interface exhibits greater promise in achieving higher bond strength compared to a SiCN-SiCN bonding interface. Moreover, conventional dielectric (TEOS) support bonding with a minimal bonding area of approximately 18% was observed. Furthermore, we successfully demonstrated sub-0.5µm pitch interconnects through meticulous optimization of lithography, electrochemical plating (ECP), chemical mechanical polishing (CMP), and bonding overlay tuning. Utilizing pad sizes of around 120nm and 240nm, with a 460nm pitch design, we achieved remarkable results. However, challenges persist in understanding and optimizing the propagation of bonding waves in fine-pitch high-density hybrid bond structures. These advancements pave the way for future advanced packaging solutions with higher interconnect density, enabling the integration of higher-performance systems. Further research and development efforts are necessary to fully exploit the potential of these innovations.

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