Reliability life assessment and prediction for high density FOWLP package using finite element analysis and statistical approach

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***Abstract*—A Finite Element Analysis (FEA) modelling study on solder joint fatigue life assessment under thermal cycling conditions for two High Density (HD) Fan Out Wafer Level Packaging (FOWLP) packages is presented in this paper. Package designs and material properties of FOWLP packaging materials such as photo-dielectric and epoxy molding compound are studied. Unlike the conventional numerical parametric study, this study adopts both Ansys Mechanical and the statistical analysis tool Minitab to analyze the modelling results. Facilitated by the statistical tool, the solder joint Thermal Cycling on Board (TCoB) fatigue life prediction formulas have been derived. For any parameters within the data ranges prescribed in Design-of-Experiment (DOE) table, solder joint fatigue life can be quickly calculated by using the derived prediction equations. Furthermore, critical factors that significantly affect solder joint fatigue life are identified by the statistical tool. Hence, the novel numerical methodology presented in this paper, which integrates the FEA modelling tool and the statistical tool, is able to enhance the efficiency of the Design Technology Co-Optimization (DTCO) process for solder joint TCoB fatigue life assessment.**

Keywords—HD FOWLP, DTCO, FEA modelling, solder joint fatigue life, TCoB, statistical analysis

I. INTRODUCTION

As a promising emerging advanced packaging technology, Fan Out Wafer Level Packaging (FOWLP) made its debut to the market targeted for mobile devices business a decade ago. However, the early application of FOWLP is often limited to single die package applications. Owing to the continuous development and investments in FOWLP made by big market players, FOWLP market has been extended to cover high-end High-Density (HD) FO applications. It is no double that FOWLP is nowadays a popular option for Antenna-in-Package (AiP) for fifth-Generation (5G) wireless communication, HD packages for High Performance Computing (HPC), and Systems-in-Package (SiP) for Automotive and Artificial Intelligence (AI). In Yole's market trend report, the estimated market value for FOWLP will be US$3 billion by end of 2025 [1].

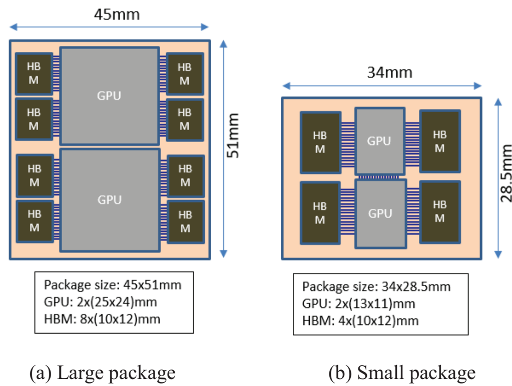
Despite the promising market forecast, the increasing complexity in HD package configurations, the market demand in cost reduction, and high expectation in reliability robustness impose tremendous challenges on the development of HD FOWLP packages. Such realities have made the design and development of a HD FOWLP package the most crucial phase for its success. The concept of Design Technology Co-Optimization (DTCO) is thus proposed to help semiconductor manufacturers reduce cost and time-to-market. This paper is aiming to present a DTCO methodology for HD FOWLP packaging by considering the package designs and material selections for FOWLP process integration simultaneously.

In this study, the Thermal Cycling on Board (TCoB) reliability assessment using Finite Element Analysis (FEA) modelling methodology is carried out to evaluate the solder joint fatigue life under thermal cycling conditions for a HD FOWLP package. The impact on solder joint reliability performance introduced by different package layout designs (e.g. sizes and number of dies) and different FOWLP materials are investigated. For FOWLP materials such as photo-dielectrics (PD) and Epoxy Molding Compound (EMC), modulus and Coefficient of Thermal Expansion (CTE) are the two critical factors to be evaluated. As compared to the conventional parametric studies, the present parametric study employs Minitab, a statistical data analysis tool, to analyze the modelling results. Facilitated by Minitab, the critical parameters among all the variables considered are able to be identified quickly. Impacts on solder joint reliability by each parameter can be clearly visualized and be compared by the main effects plots generated by Minitab. Another major advantage from Minitab is the ease in deriving prediction equations for the solder joint fatigue life. If any design or material change takes place, the prediction equations could thus provide a quick estimation on the solder joint fatigue life, as long as the changes in parameter values are still within the data range defined in the original parametric study Design-of-Experiment (DOE) table. Therefore, the DTCO methodology developed in this study enables the efficient evaluation and optimization process for HD FOWLP package development.

II. TEST VEHICEL AND NUMERICAL METHODOLOGY

A. Test Vehicle

Two high density FOWLP package designs are considered in the current DTCO study. Fig.1 shows the plan-view schematic of two HD FOWLP package layouts where the dimensions are not to scale. The large package (45mm×51mm) in Fig.1a is embedded with two large Graphics Processing Unit (GPU) dies (24mm×25mm) and eight High Bandwidth Memory (HBM) dies (10mm×12mm). The small package (34mm×28.5mm) in Fig.1b is encapsulated with two small GPU dies (11mm×13mm) and four HBM dies (10mm×12mm). All the dies have the same thickness of 700µm. These two HD package designs represent high die area to package ratios, which are 94% and 79% for large and small package designs, respectively.



(a) Large package (b) Small package

Fig. 1. Plan-view schematic of two HD FOWLP package designs.

Fig.2 shows the side-view schematic of the package. The FOWLP package fabricated using RDL-first process is mounted onto the 1.6mm thick PCB via full array Sn–3.8Ag–0.7Cu lead-free solders. The solder joint for both large and small packages is with 400µm diameter and 750µm pitch. This leads to total ~4000 and ~1700 solder joints for large and small package designs, respectively. Underfill is not used in these HD FOWLP package designs.

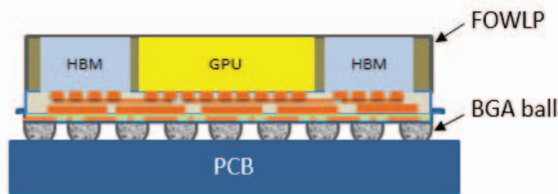


Fig. 2. Side-view schematic of HD FOWLP package design.

B. Finite Element Anaysis and Parametric Studies for Solder Joint Fatigue life Prediction

The current DTCO study focuses on the solder joint reliability performance under Thermal Cycling (TC) condition. Fig.3 shows the thermal cycling profile considered in the analysis for temperature ranging from -40˚C to 125˚C. The total duration of one thermal cycle is 60 minutes which includes a 15-minute ramp-up, a 15-minute cool down and 15-minute dwell time at both -40˚C and 125˚C. FEA software Ansys Mechanical is adopted to generate the modelling results for different design parameters and variations in the material selection.

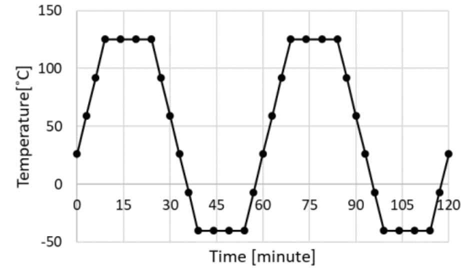


Fig. 3. Thermal cycling temperature profile.

For the sake of simplicity, 3D slice model as shown in Fig.4 is adopted in the FEA simulations. By compromising certain accuracy in the results, the modelling efficiency could be enhanced significantly which makes the subsequent parametric studies more feasible. This simplification is also considered appropriate for this DTCO study as fast turn-around time is preferred in the early package development stage. Hence, the FE models are extracted from the location indicated in Fig.4 for both large and small packages. This location represents the most onerous condition for the solder joint for its compactness in the die arrangement. Due to the half-symmetric package layout, the FE model starts from the package center and cuts through the half package. Each solder joint in the FEA model is half solder due to the symmetry.

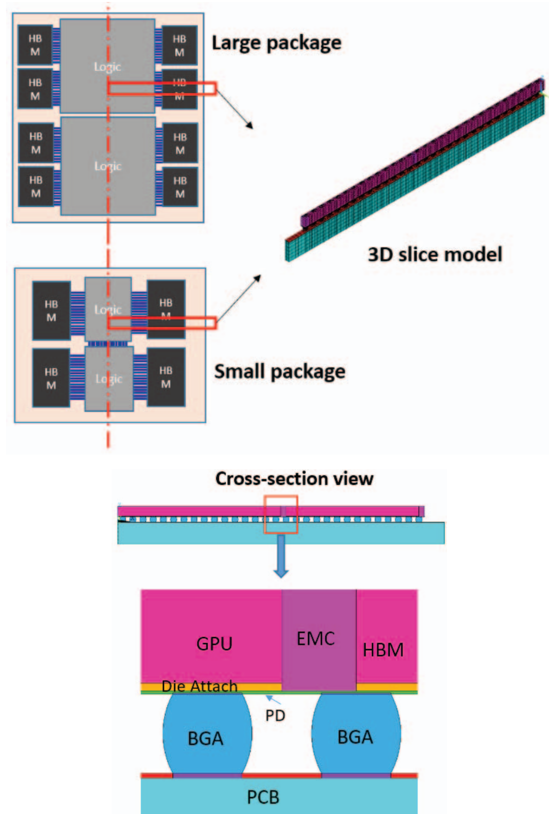


Fig. 4. 3D slice FE models.

In order to examine the impacts on the solder joint reliability performance caused by different package designs and various material candidates, parametric studies are carried out in Ansys Mechanical according to the variables listed in Table I. The parametric study modelling results are subsequently analyzed in the commercial statistical data analysis tool Minitab. By doing so, this DTCO study is able to efficiently identify the critical design parameters'/material properties' impact on the package solder joint reliability performance.

TABLE I. VARIABLES FOR PARAMTRIC STUDIES

Variables	Unit	Lowest value	Highest value
PD CTE	ppm/K	40	100
PD modulus	GPa	1.5	5
PD thickness	μm	10	40
EMC CTE	ppm/K	5	15
EMC modulus	GPa	10	20

C. *Solder Material Constitutive Model and Solder Fatigue Life Prediction Model*

The elastic-plastic-creep constitutive models for Sn-3.8Ag-0.7Cu solder are used in the FEA simulations. Table II lists the solder modulus at different temperatures, Poisson's ratio and CTE [2].

TABLE II. SN-3.8AG-0.7CU SOLDER MATERIAL PROPERTIES

Variables	Unit	Value
CTE	ppm/K	22
Modulus	GPa	54.5@-40˚C, 41.7@25˚C, 36.8@50˚C, 22.2@125˚C
Poisson's ratio	-	0.35

Eq.1 is the hyperbolic-sine creep model for Sn-3.8Ag-0.7Cu solder [3], where $\dot{\varepsilon}$ is the strain rate, σ is the applied stress in MPa, T is the absolute temperature in Kelvin. The four constants for the creep model (Eq.1) for Sn-3.8Ag-0.7Cu solder [3] can be found in Table III.

$$\dot{\varepsilon} = C_1[\sinh(C_2\sigma)]^{C_3} e^{\left(\frac{C_4}{T}\right)} \quad (1)$$

TABLE III. SN-3.8AG-0.7CU SOLDER CREEP MODEL CONSTANTS

Solder	Solder Creep Model Constants			
	C_1	C_2	C_3	C_4
Sn-3.8Ag-0.7Cu	32000	0.037	5.1	6524.7

The energy-based solder fatigue life prediction model developed from FOWLP packages [4] as shown in Eq.2 is adopted for this study.

$$N_f = 137.6 W_{cr}^{-1.112} \quad (2)$$

where N_f is the total number of cycles to failure, W_{cr} is the creep strain energy density accumulated per cycle which is obtained from FEA simulation. To calculate the solder fatigue life at package side and PCB side, the top layer (top interface) and bottom layer (bottom interface) of solder joint FEA elements shown in Fig.5 are used to derive the creep strain energy density for package side and PCB side, respectively.

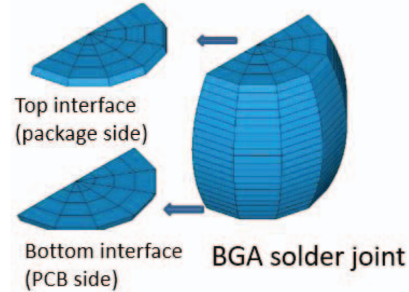


Fig. 5. Solder joint FE model.

III. RESULTS AND DISCUSSIONS

A. *Parametric Study on Effects of FOWLP Materials for Large Package*

The FEA TCoB modelling and the parametric study is first conducted for large package design. In this section, the effects of FOWLP materials, i.e. PD and EMC, on the solder joint reliability life under TC condition are investigated and discussed. Table IV is the DOE table of the design cases for different combinations of PD and EMC material properties and PD thickness. Fractional factorial DOE approach is selected and total 8 cases are generated. It should be noted that by adopting fractional factorial DOE, we assume the higher-order effects of the parameters are negligible. The purpose is to identify main effects and low-order interactions with fewer runs.

TABLE IV. DOE TABLE A FOR EFFECTS OF MATERIAL PROPERTIES

#	Photo-dielectric			EMC	
	CTE	Modulus	Thickness	CTE	Modulus
	ppm/K	GPa	μm	ppm/K	GPa
A1	40	1.5	10	15	20
A2	100	1.5	10	5	10
A3	40	5	10	5	20
A4	100	5	10	15	10
A5	40	1.5	40	15	10
A6	100	1.5	40	5	20
A7	40	5	40	5	10
A8	100	5	40	15	20

The results of solder joint creep strain energy density accumulated over one TC cycle for design case A1 is shown in Fig.6. As expected, creep strain energy density is high at both top and bottom interfaces of the solder joints. Therefore, top and bottom interface layers of the solder joints are used for fatigue

life prediction to identify the potential failure locations. The predicted solder joint fatigue life under TC condition is presented in Fig.7 for Case A1. The results indicate that the critical solder joint locates at package edge, not at large GPU chip edge. Solder joint underneath the region between GPU and HBM dies has the longest life due to top EMC material which has lower stiffness as compared to Si dies. For case A1, most of the solder joints have shorter fatigue life at PCB side interface.

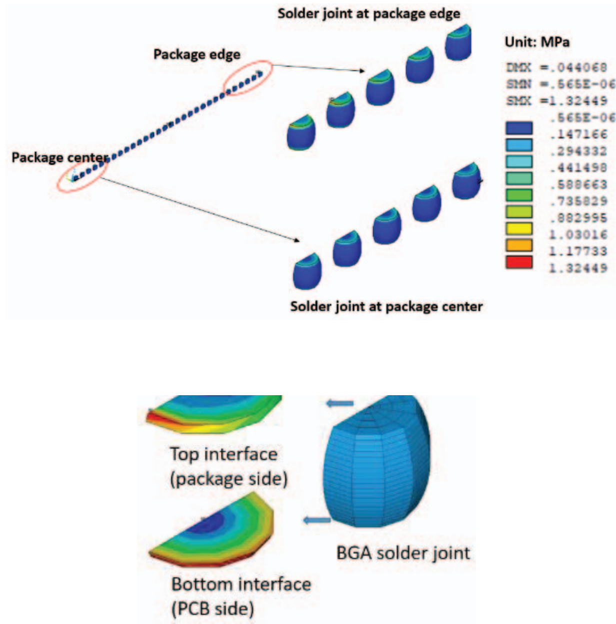


Fig. 6. Solder joint creep strain energy density accumulated over one TC cycle for Case A1.

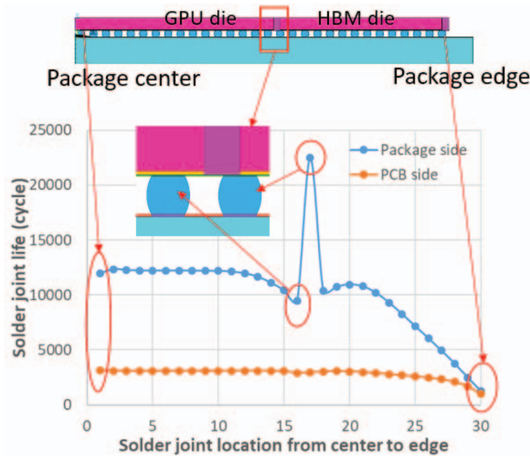
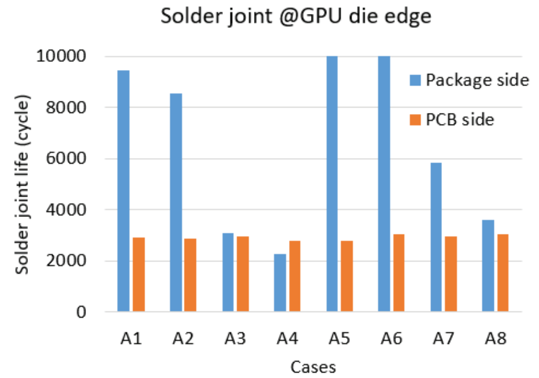


Fig. 7. Solder joint TCoB fatigue life prediction for Case A1.

The comparison of solder joint creep strain energy density accumulated over one TC cycle for all the design cases in DOE Table A (Table IV) is presented in Fig.8. The results for solder joints at two locations, i.e. large GPU die edge and package edge, are reported. Among all the 8 design cases, for most of the cases the solder joint at these two locations have shorter solder fatigue life at PCB side. Only for Case A3 and A4, the solder joints have either similar fatigue life at both sides or shorter fatigue life at package side. The results also indicate that the critical solder joint locates at package edge, not at large GPU die edge. The package reliability life is hence determined by the fatigue life for the solder joints located at package edge.



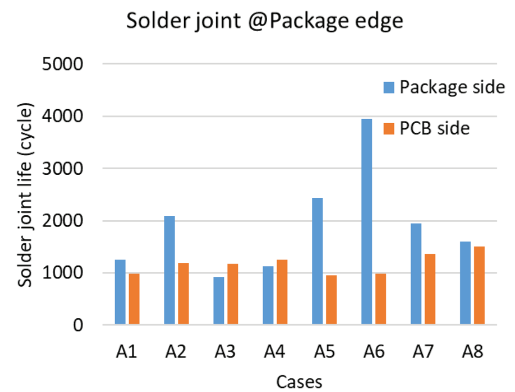


Fig. 8. Solder joint TCoB fatigue life prediction for all the design cases in DOE Table A.

After performing the parametric study simulations in Ansys Mechanical according to the DOE Table A (Table IV), the solder joint fatigue life perdition results for all the 8 design cases are input into Minitab for further statistical analysis. The purpose is to quickly identify the most critical factors that affect the solder joint reliability life for this HD-FOWLP package design. Fig.9 and Fig.10 show the main effect plots derived by Minitab for solder joint life prediction at GPU die edge and package edge, respectively. Each figure consists of individual plots for package side and PCB side.

At GPU die edge, among all 5 factors considered in DOE Table A (Table IV), PD modulus and PD thickness are the two most critical factors affecting the solder joint fatigue life at package side. For GPU die edge solder joint fatigue life at PCB side, EMC modulus and EMC CTE are the two most critical factors. For both package side and PCB side, the GPU die edge joint fatigue life has same trend with regard to all the factors except PD modulus. GPU die edge solder joint fatigue life decreases with increasing PD modulus at package side, while increases with PD modulus at PCB side. Furthermore, at GPU

die edge, PD has more influence than EMC does for package side joint life and vice versa for PCB side joint life.

At package edge, PD modulus and PD thickness are still the two most critical factors affecting the solder joint fatigue life at package side. For package edge solder joint fatigue life at PCB side, the two most critical factors are PD modulus and PD CTE.

For both package side and PCB side, the package edge joint fatigue life has same trend with regard to all the factors except PD modulus and EMC modulus. Package edge solder joint fatigue life decreases with increasing PD and EMC modulus at package side, while increases with PD and EMC modulus at PCB side. In addition, at package edge, PD has more influence than EMC does for both package side and PCB side joint life.

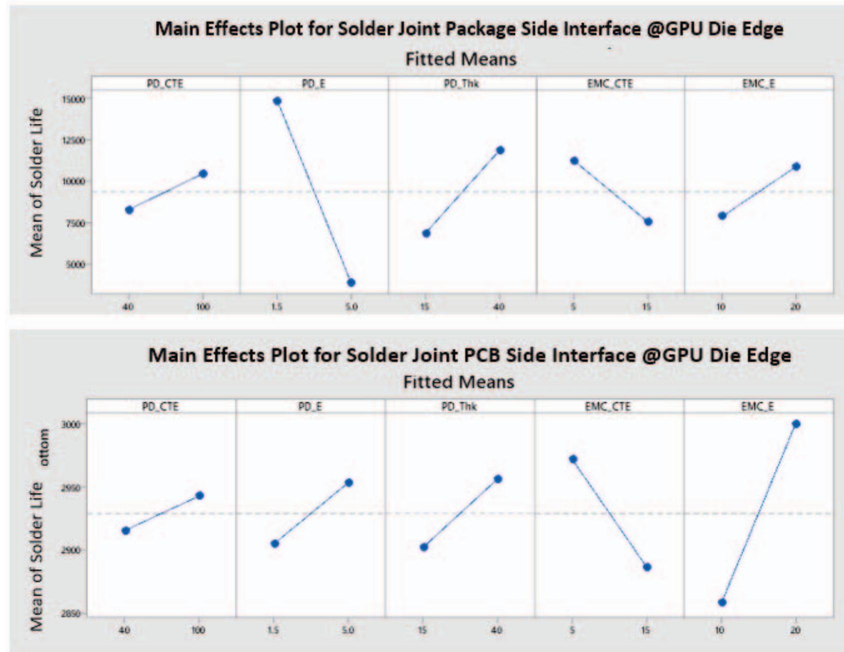


Fig. 9. Main effect plot of solder joint fatigue life at GPU die edge based on DOE Table A results.

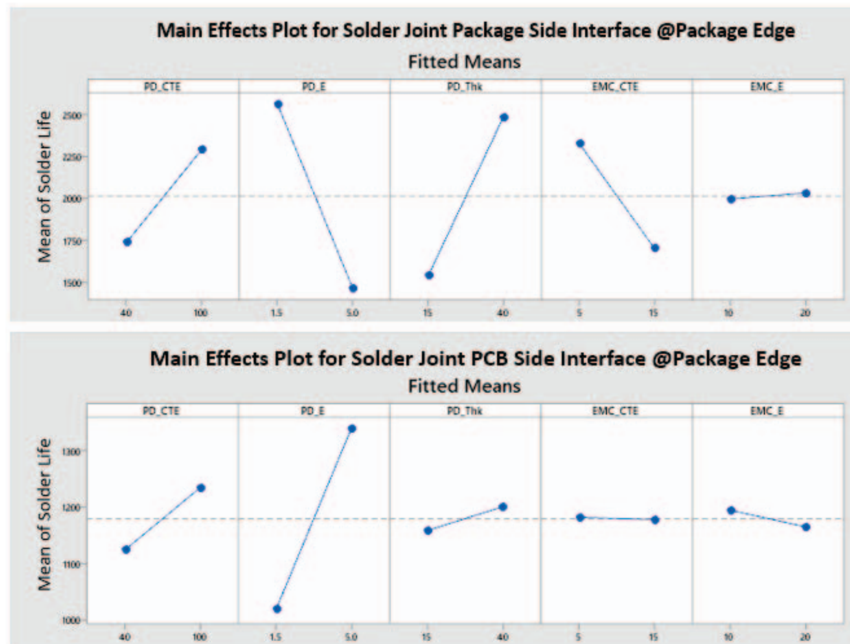


Fig. 10. Main effect plot of solder joint fatigue life at package edge based on DOE Table A results.

As mentioned in the introduction section, one of the major advantages of Minitab is the ease of generating prediction model based on DOE results. Hence, by using the regression algorithm, the solder joint fatigue life prediction equations are generated in Minitab for solder joints at respective locations and at both package side and PCB side. For any values falling within the variable ranges in DOE Table A (Table IV), solder joint fatigue life can be calculated by following equations without the need of running additional simulations.

Package side fatigue life prediction model for solder joint at GPU die edge:

$$N_f = -6505 + 36.02\alpha_{PD} + 2152E_{PD} + 447.5Thk_{PD} - 368.8\alpha_{EMC} + 993.4E_{EMC} - 75.81E_{PD} \cdot Thk_{PD} - 213.3E_{PD} \cdot \alpha_{EMC} \quad (3)$$

PCB side fatigue life prediction model for solder joint at GPU die edge:

$$N_f = 2683 + 0.4537\alpha_{PD} + 8.338E_{PD} - 0.9918Thk_{PD} - 8.505\alpha_{EMC} + 18.79E_{EMC} * 0.97E_{PD} \cdot Thk_{PD} - 1.411E_{PD} \cdot \alpha_{EMC} \quad (4)$$

Package side fatigue life prediction model for solder joint at package edge:

$$N_f = 414.1 + 9.21\alpha_{PD} + 149.6E_{PD} + 61.31Thk_{PD} - 62.49\alpha_{EMC} + 60.66E_{EMC} - 7.235E_{PD} \cdot Thk_{PD} - 17.58E_{PD} \cdot \alpha_{EMC} \quad (5)$$

PCB side fatigue life prediction model for solder joint at package edge:

$$N_f = 1198 + 1.836\alpha_{PD} - 44.89E_{PD} - 8.678Thk_{PD} - 0.3751\alpha_{EMC} - 13.47E_{EMC} + 3.191E_{PD} \cdot Thk_{PD} + 3.245E_{PD} \cdot \alpha_{EMC} \quad (6)$$

where α is the CTE in ppm/K, E is the modulus in GPa, and *Thk* is the thickness in μm.

B. Comparison of Solder Joint Fatigue life between Large Package and Small Package

To compare the effect of package design (size and layout) on the solder joint fatigue life, FEA analysis has been performed using small package design as shown in Fig.4. The most onerous case A3 in DOE Table A (Table IV) is selected as reference case to compare the results of small package with the large package results. Fig.11 shows the solder joint fatigue life for small package predicted by FEA analysis. It is found that the critical solder joint also locates at package edge for small package. Solder joint underneath the region between GPU die and HBM die has the longest life due to EMC material on top of the solder joint at this location. For Case A3, package edge solder joints have similar solder joint fatigue life at package side and PCB side. These findings are similar to those observed for large package design.

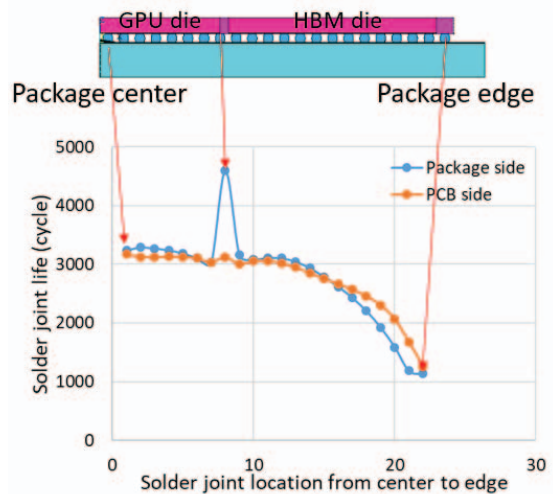


Fig. 11. Solder joint TCoB fatigue life prediction for small package (Case A3).

The results of solder joint fatigue life predicted by FEA analysis are compared between large and small packages in Fig.12, Fig.13 and Fig.14. Fig.12 confirms the previous finding that both small and large package have similar solder joint fatigue life trend, i.e. critical solder joints locate at package edge, not at GPU die edge. According to Fig.13 and Fig.14, solder joint at GPU die edge has similar TCOB fatigue life for both small and large packages. At package edge, the solder joint has longer life for smaller package, however, the difference is not significant.

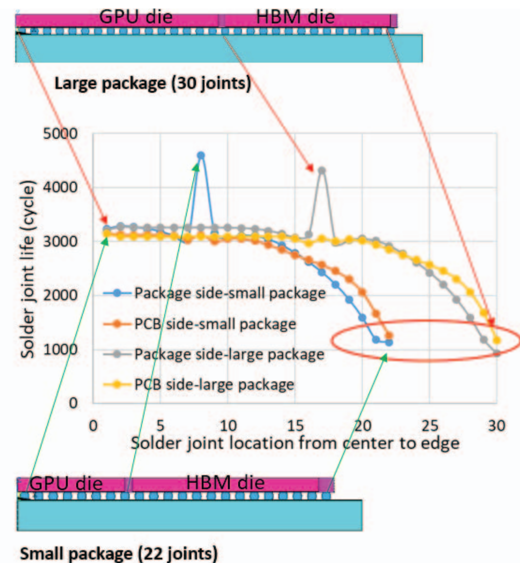


Fig. 12. Comparison of predicted solder joint TCoB fatigue life between large package and small package (Case A3).

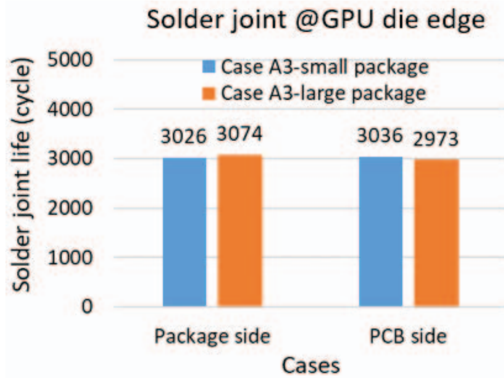


Fig. 13. Comparison of predicted solder joint TCoB fatigue life at GPU die edge between large package and small package (Case A3).

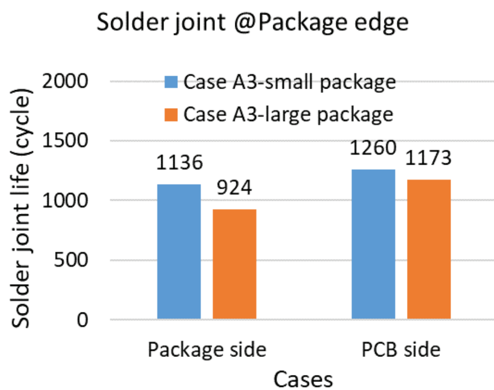


Fig. 14. Comparison of predicted solder joint TCoB fatigue life at package edge between large package and small package (Case A3).

IV. CONCLUSION

A novel DTCO approach incorporating FEA modelling work with statistical tool has been presented in this paper. By adopting this methodology, the critical factors that affect the solder joint TCoB fatigue life for HD-FOWLP package can be efficiently identified. The prediction equations for solder joint TCoB fatigue life for critical solder joints can also be derived. This study demonstrates that the developed DTCO approach helps the design engineer to perform fast and efficient evaluations on the design change and material selections. Case studies on solder joint TCoB fatigue life for two HD-FOWLP package designs are presented. Based on the parametric studies performed, following findings are obtained:

- The results for all the design cases indicate that the critical solder joint locates at package edge, not at large GPU die edge.
- For most of the solder joints, potential failure location is at bottom interface (PCB side), not at top interface (package side).
- Generally, relatively high PD modulus and/or high PD CTE, thick PD layer can help improve overall package TCoB fatigue life.
- Following parameters are identified as the most critical parameters that will significantly impact solder joint reliability performance at various locations:
  - package edge solder joint at top interface (package side): PD modulus and its thickness
  - package edge solder joint at bottom interface (PCB side): PD modulus and CTE
  - GPU die edge solder joint at top interface (package side): PD modulus and its thickness
  - GPU die edge solder joint at bottom interface (PCB side): EMC modulus and CTE.

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