Towards Heterogeneous Integrated Electronic-Photonic Packages for Hyperscale Data Centers

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Abstract

There is an explosion in the volume of data generated, transmitted, processed, and stored across the internet after the wide usage of smartphones, high-performance computing, internet-of-things, and cloud services. To handle such data, high-performance optical transceivers are required. In this paper, a novel electronic-photonic heterogeneous integration solution based on fan-out wafer-level packaging which can be used for high-speed scalable optical engine is discussed. The packaged interconnects are optimized to handle high-speed signals for data center applications and the optical engine package is examined for warpage behavior. The photonic integrated circuit equipped with edge suspended coupler optical I/Os is integrated by employing special processing.

Keywords- Hyperscale Data Centers, Electronic Photonic Package, heterogeneous integration, optical engine, Fan-out wafer-level packaging.

1. Introduction

Data on the internet is handled by data centers. Data center interconnects facilitate hundreds of thousands of servers to communicate with one another, which are the basic building blocks for computing and storage. A hyper-scale data center can contain over 5,000 servers. In order to efficiently handle the volume of data in the coming decades, they need to be able to meet stringent power, performance, form-factor, operating cost requirements [1-2]. Interconnects play a key role to achieve these requirements.

Due to higher data rates, there is an increasing demand to use optical interconnects within and between the data centers [3-4]. Therefore, there is a rapidly growing market for optical links that is expected to grow more than $7B by 2024 [5]. For better energy efficiency and for scalability of data rates into the terabit domain, photonic integrated circuits (PICs) need to be integrated with electronic integrated circuits (EICs) within small form-factor system-in-packages known as optical engines. Electronic photonic heterogeneous integration enables such complex electronic-photonic systems. Moving forward, application-specific integrated circuit (ASIC) switch and optical engines are also to be integrated together for even better performance and energy efficiency [6].

In this study, a fan-out wafer-level packaging (FOWLP) based electronic-photonic heterogeneous integration is employed. The key benefit of this wafer-level packaging is that it can integrate optical engine components from different process nodes and diverse technologies such as complementary metal-oxide-semiconductor (CMOS), silicon germanium (SiGe), silicon on insulator (SOI), etc. They can be optimized independently and integrated into small-form-factor packages to achieve power, performance, form factor, and cost optimization that is not otherwise possible with monolithic integration. Moreover, each optical engine component is pre-tested, and only Known Good Dies (KGDs) are used in the FOWLP package, significantly reducing overall cost.

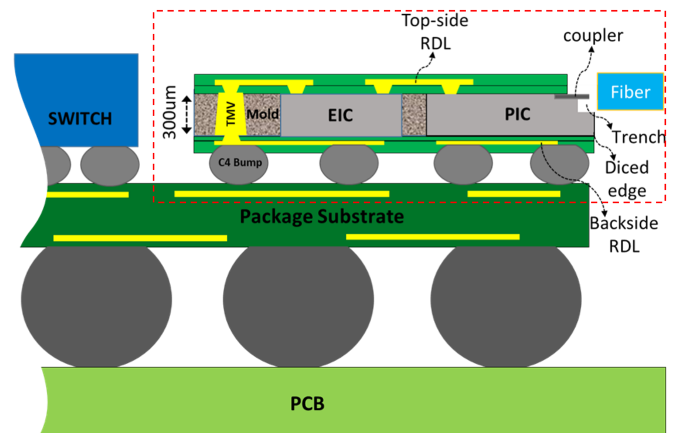

Figure 1. The cross-sectional schematic of the FOWLP optical engine package (inside the dotted outline). The epoxy mold compound embeds the PIC and EIC chips. The extended mold area is used to support the electrical lateral and vertical routing connections using the RDL and TMV.

Other efforts were made to employ advanced packaging for optical engines by using through-Si-via (TSV) technology to achieve electronic-photonic integration at the package level [7]. However, such formats potentially incur high manufacturing costs arising from TSV formation in PIC wafers and providing additional PIC areas for TSV keep-out zones. The impact of TSV fabrication on PIC components also makes the TSV approach complicated from both the design and fabrication perspectives. The FOWLP approach employed here integrating PIC with edge couplers has not been applied to data center. Such integration scheme can achieve the requirements of optical engines at up to 50% cost reduction compared to the TSV approach and also can provide a clear differentiation compared to other formats currently in the industry. The key challenges addressed here include encapsulation of the PIC without impacting PIC critical structures such as the optical couplers, optimization of redistribution layer (RDL) / through-mold via (TMV)

interconnects for high data rate applications, as well as mechanical modeling to study stress and warpage in the optical engine (OE) package.

2. Electronic photonic heterogeneous integration

To address the requirement of integrating photonic and electronic ICs for optical transceivers, packaging of the chiplets based on FOWLP is employed. This has been previously demonstrated for electronic chiplets for Digital and RF applications [8]. The intended application here demands the package to be compatible with high-speed signal. Given that the FOWLP platform has good RF performance, it is therefore appropriate for high-performance OE applications. For demonstration, a package test vehicle is designed with a size of 11mm×11mm where both the PIC and EIC dies are embedded in the mold compound. The package is designed to accommodate PIC with suspended optical couplers to facilitate edge coupling to external fibers. Edge coupling has superior performance comparing with vertical coupling; however, the challenge is to maintain the coupling structures and their facets devoid of any contaminants during the packaging process. Here, a passive PIC with suspended edge couplers on one side with a deep trench of 100μm is employed. A specially designed silicon buffer structure around the trench will protect the couplers during the molding process. A passive EIC chip is employed with daisy chains and the extended mold area around the PIC and EIC will accommodate the TMVs and lateral RDL interconnects. In a functional OE package, EICs used will be Drivers and Trans-Impedance Amplifiers (TIAs) for driving the modulator and amplifying the received signal respectively. Figure 1 and 2 show the cross-sectional schematic and the top view of the FOWLP test vehicle, respectively.

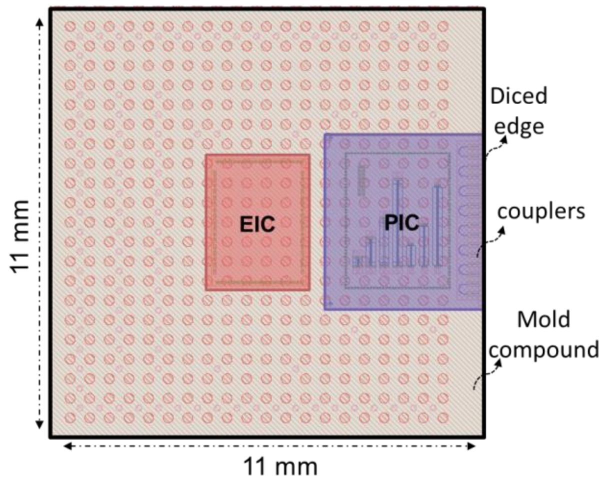

Figure 2. The package test vehicle floor plan layout integrating EIC and PIC. The PIC embedded in mold compound is diced on one side of the package to expose the optical waveguides.

3. Optimization of interconnections

One of the key challenges in creating a package solution for optical transceivers in data center applications is to create an optical engine design that can meet the high-speed data rate handling of the interconnects in the system in package (SiP). To address this challenge, simulations were carried out to optimize the high-speed interconnections that connect the chiplets and then to the external circuit that is based on a differential transmission format.

The structures in GSSG configuration were designed and simulated using a 3D full-wave electromagnetic simulator, high-frequency structure simulator of ANSYS Electronics. The GSSG coplanar waveguide (CPW) with a 100ohm differential impedance has a signal line with a width of 60μm. The space between two signal lines and the space between the signal line and side ground are both set to 30μm. The RDL transmission line has a length of 2mm and the TMV has a top and bottom diameter of 100μm and 150μm respectively with a pitch of 250μm. The transition from CPW transmission line to TMV has a length of 250μm. The controlled collapsed chip connection (C4 bump) connecting the package Cu pad to substrate Cu pad has a center diameter of 100μm and a height of 60μm. The mold compound dielectric constant and the loss tangent are 3.42 and 0.008, respectively. The structures are excited using lumped ports with a 100ohm differential reference impedance.

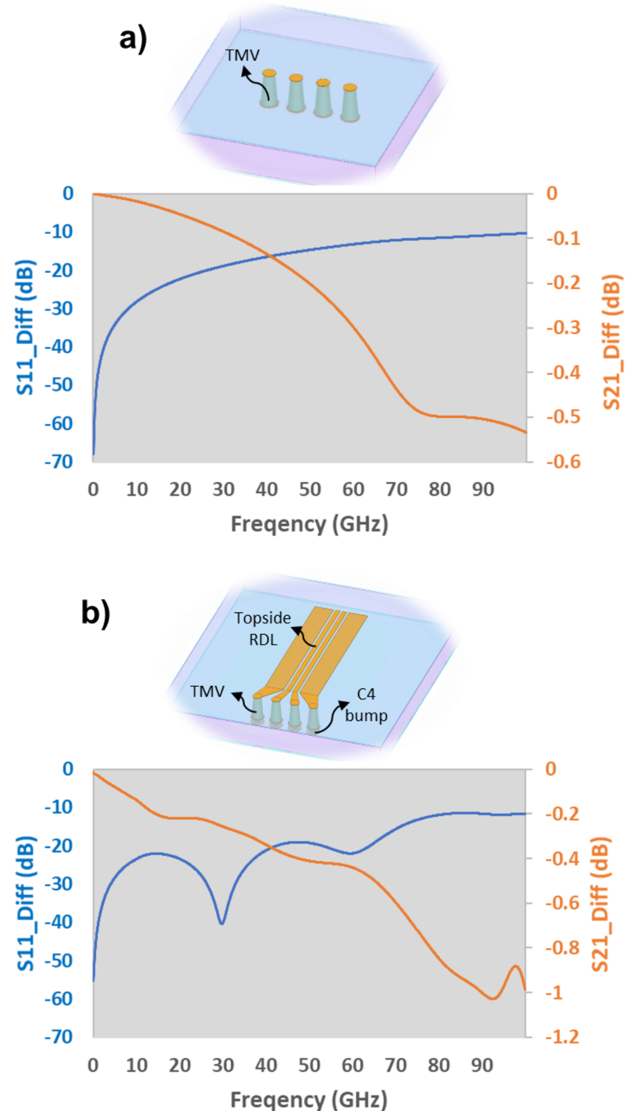

Figure 3. Frequency response of the FOWLP differential transmission line up to 100GHz a) of TMV b) transmission line including C4, TMV, and the RDL.

The results from the model are shown in Fig. 3 for frequencies up to 100GHz. Figure 3a shows the high-speed signal transmission performances of TMV alone and Fig. 3b shows the transmission line including C4, TMV, and the RDL CPW. Figure 3b shows it has a return loss of more than 20dB and an insertion loss of less than 0.5dB at 60 GHz. The simulated results show that the FOWLP interconnect has a wide bandwidth and is capable to support the high-speed digital signals in the OE.

4. Mechanical study

A mechanical study is done to examine the impact of package warpage and other mechanical behavior such as stress in TMV of the OE package. A 3D model, as shown in Fig. 4, is developed for OE FOWLP with TMVs. In the package, there are two silicon dies that are molded within top and bottom dielectric layers of thickness 20µm and mold thickness of 300µm. C4 solder bumps are then attached with the package for interconnecting it with the package substrate. The detailed local model of TMV for stress analysis is shown in Fig. 4c, illustrating the stress developed at critical locations.

The package thermo-mechanical simulation is carried out for a stress-free reference temperature of 175ºC. The room temperature package overall co-planarity is around 15µm (Fig. 4a) and the PIC warpage is 5µm (Fig. 4b). This package warpage doesn't pose any significant challenge for assembly. The local detailed sub-modeling carried out for TMV stress analysis (Fig. 4c) predicted a stress of 125MPa (compressive) which is considered safe for TMV.

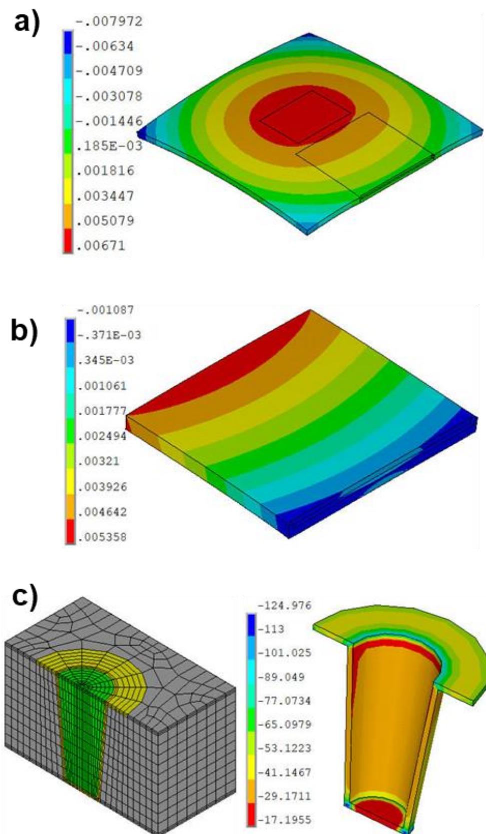

Figure 4. Mechanical modeling of the package a) Package overall warpage. b) PIC warpage. c) cross-sectional mesh view of TMV and its stress plot.

5. FOWLP processing

A mold first approach is employed to fabricate the OE test vehicle. The fabrication is carried out at the Institute of Microelectronics state-of-the-art 300mm FOWLP line. The process steps are described in Fig. 5 where both the EIC and PIC are picked and placed with their face down on the adhesive mold plate and subsequently subjected to molding process to encapsulate the chiplets. After debonding of the reconstituted wafer and back grinding to a thickness of 300µm, the wafer undergoes RDL and TMV interconnect processing. Finally, the solder ball is attached and the package undergoes dicing through its deep trench to expose the optical couplers.

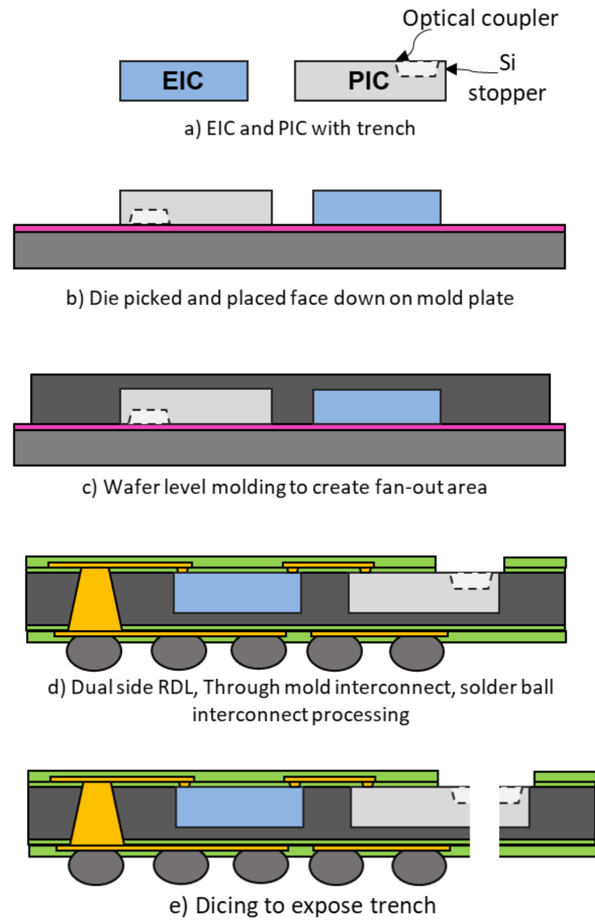

Figure 5. FOWLP process flow of the package where both the EIC and PIC are embedded inside the mold compound.

One of the main challenges in this FOWLP integration is enabling edge coupling to the PIC that is embedded in the mold compound. To make this possible, it is critical to make sure the edge suspended couplers are not contaminated during mold processing. Contamination of the couplers from mold will adversely affect the performance of the PIC as it cannot make good coupling with external fibers. For a contamination-free coupler, a special buffer structure is added to the PIC design that will act like a dam-like stopper structure during the molding process. After the packaging process is completed, the silicon stopper structure is diced away in order to expose the couplers to the external fibers. Figure 6 shows the test vehicle sample where the PIC can be seen embedded in the mold. Figures 6a and 6b show the top view of the sample

before and after dicing respectively and Fig. 6c shows the cross-sectional view of the sample after dicing through the trench. Upon inspection, no cracks or separation were observed along with mold or silicon.

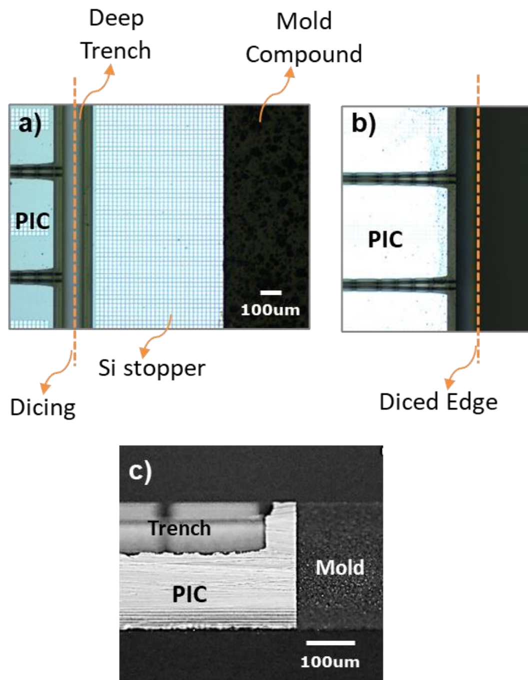

Figure 6. Images showing the PIC embedded inside the mold a) top view after molding, b) top view, diced molded sample to expose the optical couplers and c) cross-sectional view after dicing through the trench.

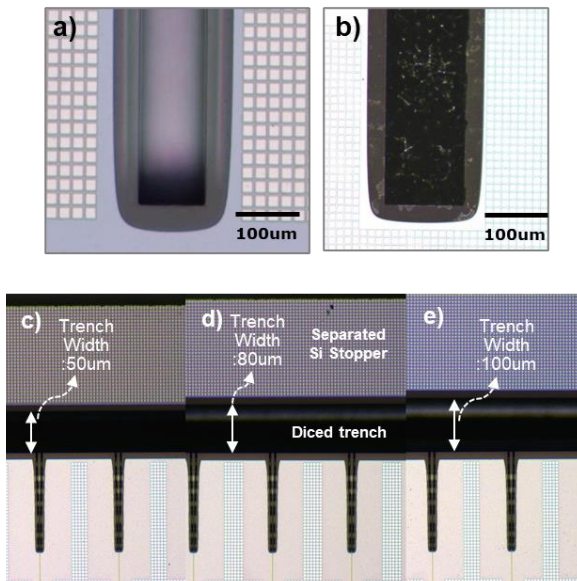

Figure 7. Impact of the silicon buffer structure to stop the mold from seeping into the deep trench a) image showing clean trenches without any contamination from the molding process which was prevented by the silicon buffer structure b) image from a sample without the mold stopper on the north side of the trench where it is evident that the mold compound seeped into the trench. Images from three different samples on dicing frame after dicing through the trench to illustrate the study on trench dicing with trench width c) 50µm, d) 80µm, and e) 100µm.

From Fig. 7a and Fig. 7b, the effect of the silicon buffer structure to stop the mold from seeping into the deep trench can be observed. Figure. 7a shows a top view of a clean trench without any contamination during the molding process as it is prevented by the silicon buffer structure. Another sample (Fig. 7b) is processed without the buffer on the north side of the trench where it is evident that the mold compound seeped into the trench and contaminates the coupling structures. In addition, an experiment was conducted to study the dicing of the PIC through its deep trench with suspended optical couplers. The investigation is to verify that the dicing process to expose the couplers does not cause any damage to the PIC optical couplers. Three variants of PIC were studied with varying trench widths of 50µm (Fig. 7c), 80µm (Fig. 7d), and 100µm (Fig. 7e). The results show that the dicing process was completed without damaging the optical couplers.

Conclusions

In this paper, a new electronic-photonic heterogeneous integration solution based on fan-out wafer-level packaging, which can be used for high-speed scalable optical engine applications, is proposed. Critical areas such as optimization of the interconnect, package warpage, and package processing of PIC with edge optical couplers are discussed. Successful demonstration of FOWLP for hyper-scale data center optical engines will allow FOWLP to be applied to several other applications such as High-performance computing, miniaturized sensors, etc.

Acknowledgments

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