Process Development and Integration on Si Substrate for Ion trap-based Quantum Processors

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Abstract

Si substrates provide flexible platform for quantum application that can integrate photonic components, active devices, and metal electrodes. Photonics integrated surface ion trap can effectively integrate the functionality of photonics integrated circuits and ion traps on the same Si-substrate. The ion trap electrodes are fabricated on a 300mm high resistivity substrate. Both leakage current and capacitance meet the device factional requirements at the wafer scale. The loaded Q-factor of the package at 9.8K is over 20, allowing application of 300V RF at low power at a trap drive frequency of 16 MHz for barium ion.

Introduction

Full stack quantum computers based on different platforms are being scaled up to out-perform classical computers in solving real world problems [1]. This has led to the renewed effort in developing Si-based foundry compatible processes that can be used for component integration and 3D packaging of heterogenous structures as needed in some of the quantum computing platforms like trapped ions and photonic integrated circuits. Of particular interest is barium ion based trapped ion processor which has unique advantage as the detection wavelength matches well with available photonic waveguide material in terms of efficiencies. This system is also well-studied and hence easier to characterize the photonic integrated ion traps. [2,3] where small Noisy Intermediate Scale Quantum (NISQ) algorithms have been demonstrated in this system.

This paper focuses on Si-foundry process development, integration, and packaging for a surface ion trap. The first part will briefly introduce the design of a surface ion trap followed by a detail description of wafer-scale process development and integration. The electrical testing of both the wafer-level and device-level are reported which convincingly tallies with the design parameters. The resonator testing in the cryogenic environment is presented in the concluding section.

Surface Ion Trap Design Specifications

The design of the surface ion trap chip is shown in Fig.1(a). . The most crucial feature of the design are as follows: (a) the central RF ground is split into two so as to tilt the effective trapping axis for laser cooling of all modes, (b) the simulated capacity of the trap is about 70 ions with an equal spacing of about 5-10 microns and lastly, the width of the electrodes are chosen such that for barium ion the location of the trap minimum is about 90 microns above the surface. The detail assignment of electrodes within functional is shown in Fig. 1 (b). The gap between the electrodes are optimized for the fabrication process as well as to make the design uniform across the chip. This allows uniform processing to maintain electric field uniformity along the ion chain.

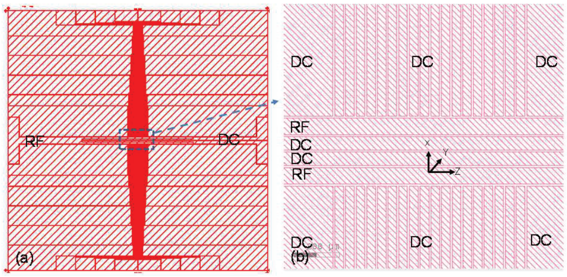

Fig.1 The design of surface ion trap on the Si substrate (a). The enlarged view of the central segments of the trap(b).

Wafer Process Integration and Fabrication

A 300 mm high resistivity Si is used as a substrate for the ion trap fabrication. The Oxide-First-Metal-Last (OFML) approach is developed and applied in this device fabrication process [4]. The surface ion trap chip fabricated by this approach had been used for trapping $^{88}\mathrm{Sr}^+$ ion [5,6,7]. The major process flow of OFML used for $^{138}\mathrm{Ba}^+$ trap fabrication is shown in Fig. 2. Oxide pattern is smaller than the metal pattern preventing the oxide exposer to the trapped ion from the mask design. A 2μm SiO_2 is deposited by PECVD on Si substrate as an isolation layer. (fig. 2a). A positive photoresist (PR) is used within the SiO_2 pattern mask and dry etching (Fig.2 (b)). Subsequently, a Ti/Cu seed layer is sputter deposited on the oxide pattern formed after dry and wet clean process that is shown in Fig. 2 (c). A thick PR is coated for the mask of metal electrodes (see fig.2(d)). Multiple layers of Cu/Au metal electrodes are electroplated after plasma descum (see Fig. 2(e)). A global wet etching (see Fig.2(f)) is used to etch back the Ti barrier and Cu seed layers respectively. This process isolated the metals to form electrodes with low leakage current. The final fabricated device is shown in Fig.3(a) and an enlarged version is shown in Fig.3 (b) and (c). the gap between the metal electrodes are clearly visible on the optical inspection as demonstrated in Fig 3 (c). To further check the metal electrodes isolation and profile, a cross-section Scanning Electron Microscope (SEM) image is taken as shown in Fig. 4. The oxide is fully covered by the top metal electrode in Fig.4 (a) which is even more obvious in the enlarged view of metal electrode (see Fig.4 (b)) clearly showing the oxide layer fully covered by the top Au metal electrode. It is also important to note that the metal electrodes are wider on the top as compared to the bottom oxide space. The ions which are confined 90

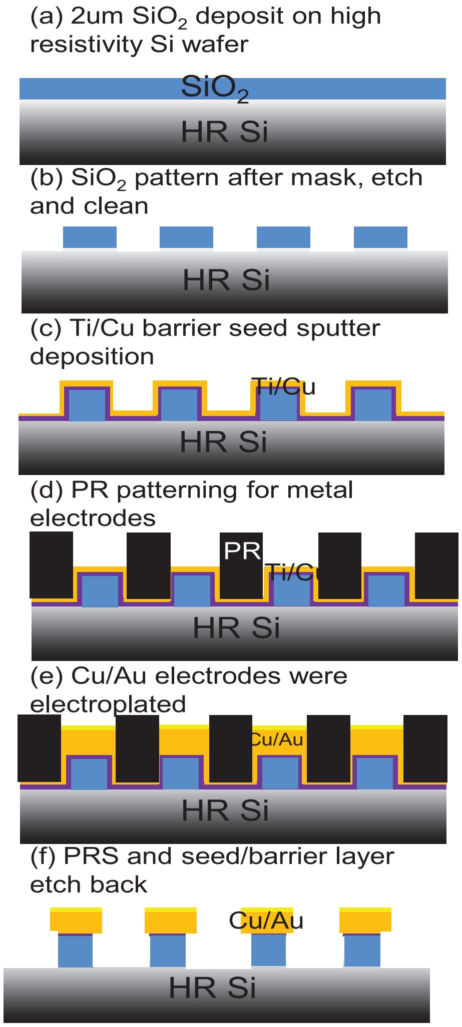

Fig.2.The major fabrication process flow

microns above the trap surface usually have a direct field of view of the oxide. This often leads to unwanted voltage noise seen by the ion, effectively introducing noise to the quantum circuit. Our fabrication method of obstructing the oxide layer and hence charge accumulation screens the noise.

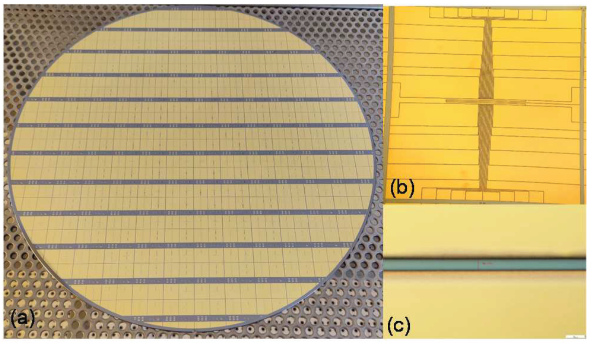

Fig. 3. Fabricated ion trap. (a) full wafer (b) enlarged die image. (c) Enlarged the trench between metal electrodes

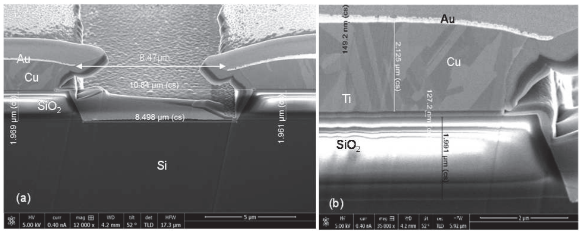

Fig.4. The cross-section of ion trap chip. (a). Trench between metal electrodes. (b). Enlarged view of one metal electrode

Surface Ion Trap Packaging

The fabricated ion trap wafer is diced according to the design size. An adhesive SMT 158N is used as die attach material that had been evaluated at cryogenic temperature to ensure both its compatibility to low temperature and dielectric loss. No delamination is observed for the samples with SMT158N die attach material at 1K. The ceramic pin package array (CPGA) carrier has a cavity which is compensated by a glass spacer added to the chip by SMT158N and aligned within 0.5 degree of angular precision. The chip is wire-bonded using Au wire to the chip-carrier pads and pull-tested before characterization is done. The surface ion trap chip completed packaging and shown in Fig. 5.

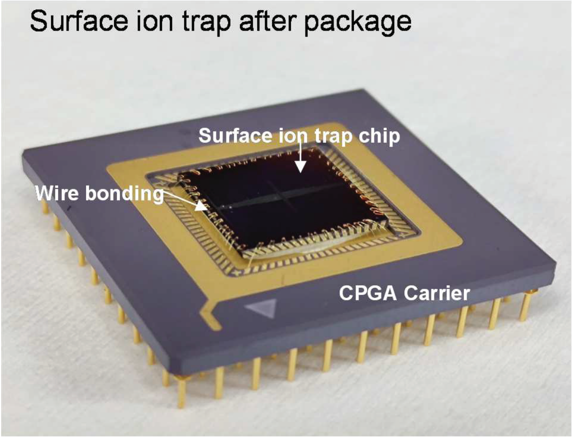

Fig. 5. The surface ion trap chip after package

Results and Discussion

A. DC testing

To characterize the electrical connectivity of the electrodes of the trap, a test structure with 5µm, 7 µm and 10 µm line/space were designed and tape out with ion trap chip that is shown in Fig. 6. A 4-point testing is performed on test structures with varied gaps of 5µm, 7µm and 10 µm metal line in the shape of a comb and meandering structure. The leakage currents obtained from these measurements are important to determine the maximum voltage that can be applied before breakdown as well as possible heating of ion qubits due to high leakage current.

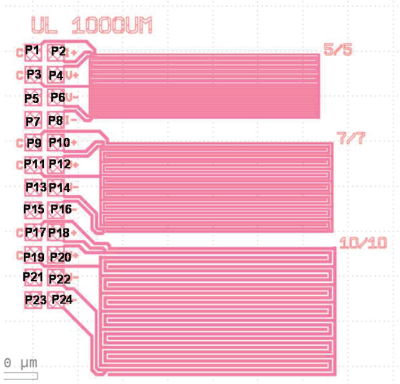

Fig.6. Meander test structures design with 5µm, 7 µm and 10 µm line /space

The resistance and leakage current data for 5µm, 7µm and 10µm gap structures respectively are shown in Fig. 7

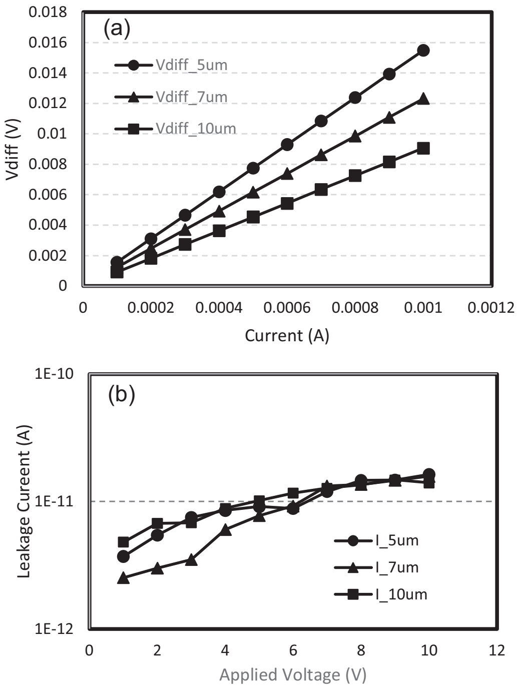

Fig.7.Meander test structures design with 5µm, 7 µm and 10 µm line /space

The voltage different (V_{high}-V_{low}) of resistors with 5µm, 7µm and 10µm gap shows a linear behavior with current, reassuring that connectivity of the lines over a long length even after etching process. The maximum leakage currents for 5µm, 7µm and 10µm gap is less than $2E^{-11}$A at applied voltage at 10V limited by the ammeter sensitivity. No metal short was observed for the test structures.

The fabricated ion trap chip was tested after process monitor test structure characterization. The leakage between the RF and DC pad was characterized and reported in Fig.8 (a). The RF ground and the RF signal electrodes run parallel for 4.6 mm separated by a trench (inset of Fig.8 (b)), which can potentially have undesired barrier metal residue. Ti metal easily oxidized on the oxide surface. The Ti wet etching chemical cannot etch back TiO_2. The measured leakage current between 4.6mm electrodes (DC and RF pads) is however less than $1E^{-5}$A when the swept voltage from 0 to 10V. No DC electrical short was observed between any of the electrodes verifying the success of global wet etching process. The metal electrodes electroplating, and global wet etch back processes of 4.6mm metal line with 7µm space device geometry are challenges. One metal residue or defect within 4.6mm will cause full device higher leakage or short. The process can be further optimized in the subsequence wafer fabrication. The capacitance between RF and DC line is $6E^{-13}$ F at 10 V at 1 MHz frequency, consistent with the expected capacitance of the trap observed in the subsequent device characterization steps.

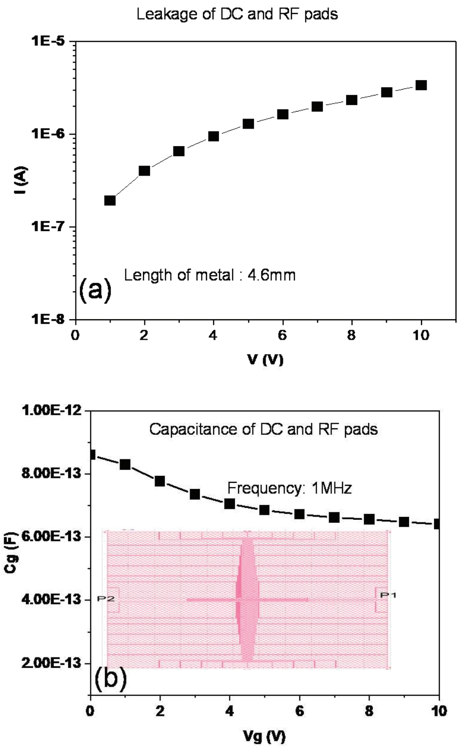

Fig.8. The leakage current and capacitance measurement between DC and RF electrodes in ion trap chip

B Cryogenic Testing of the Ion Trap

The ion trap package placed on the chip-carrier and a calibrated resonator are used to perform the RF electrical characterization. The trap chip package is installed in a close-cycle cryostat from Advance Research Systems (ARS) that is shown in Fig. 9 inset (a). The ion trap package is cooled down from 294K to 9.8K in the cryogenic chamber within 6 hours. We observe the RF as well as other DC electrode electrical properties in an automated data-logging system as the cool down and heating up happens. This allows us to estimate the

RF loss as a function of temperature. For testing the RF properties of the trap chip in the AC path, Agilent Technologies E5061B network analyzer is used. A Keithley 3390 arbitrary waveform generator (AWG) is used as a RF signal generator. The S11 parameter measured in the full quantum computing setup at the base temperature of 9.8K is plotted within the range 10MHz to 70MHz in Fig. 9. The Q factor derived from the S11 plot is 21 at 15.47 MHz at 9.8 K. This Q-factor, as per the design and simulation provides a voltage of 300 V to the RF electrodes. The voltage is equivalent to a trap confinement depth of about 100 meV which is well above the ion energy after Doppler cooling. We have also performed the Q-factor measurement as a function of temperature. As expected, the Q-factor is very low (<1) for temperature above 50K. However, below 20K when impurities in Si as well as in the dielectric freezes out and the dielectric loss in the substrate minimizes and hence the loaded Q-factor of the shoots up. Therefore, the high resistive Si could be used as a substrate for trap operations below 9.8K but cannot be used at room temperature based on the current test results. For room temperature operation, a thick oxide layer will be necessary which is the next version of the trap currently in fabrication.

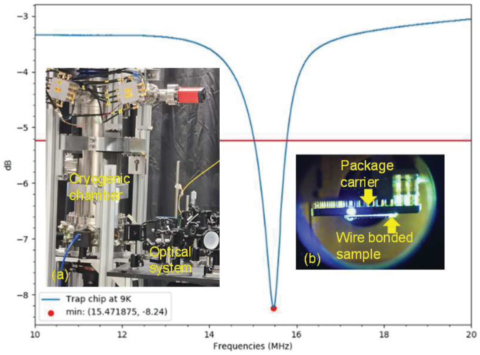

Fig.9. The RF resonance curve measured at 9.8K. The red line indicates the -3 dB line. Inset (a) shown the cryogenic testing chamber and inset (b) shown the ion trap sample was face down installed inside of cryogenic chamber

Conclusions

In summary, a surface ion trap chip was fabricated and integrated on high resistivity Si substrate for trapping and the basic platform for the photonic device integration at visible wavelength.

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