MONOLITHIC INTEGRATION OF SCALN MEMS FILTER ON RFSOI USING ALD AL2O3 AS VHF BARRIER

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ABSTRACT

We present a novel low-temperature process approach that enables the monolithic integration of scandium-doped aluminum nitride (ScAlN)-based radio frequency (RF) micro electromechanical system (MEMS) filters with RF switches. A planarized SiO_2-based ankle and cavities for the MEMS device were established through a three-step process: 1) swimming pool pattern and etch, 2) passivation of the side wall and bottom of the swimming pool with atomic layer deposited Al_2O_3, and 3) swimming pool refill with SiO_2 and planarization. ScAlN film based bulk acoustic resonators (FBAR) filters were then fabricated on the planarized surface, and eventually undercut was formed using vapor hydrofluoric acid (VHF) etch. The highest process temperature is 350 °C in the whole integration flow. The approach enabled successful integration of a ScAlN-based MEMS filter on top of the radio-frequency integrated circuit switch wafer. The integrated FBAR shows a center operation frequency of 2.58 GHz, bandwidth of 117 MHz, and an insertion loss of 3.7 dB. The integrated filter with switch has a footprint of $1mm^2$.

KEYWORDS

Monolithic integration, low temperature, VHF barrier, ScAlN film based bulk acoustic resonator, Filter

INTRODUCTION

With the increasing demand for data-driven applications, electronic megatrends are driving the adoption of MEMS and sensor devices in various areas, such as RFMEMS inertial and micromirrors for 5G and beyond, microphones, micro speakers for voice processing, and pressure and magnetic sensors for electronic cars. Additionally, edge computing for smarter sensors, robots, and health monitoring is gaining popularity. Despite the significant demand for MEMS devices, their integration with traditional chip-level packaging is limited by factors such as high-power consumption, large footprint, and high cost, resulting in the integration of only a limited number of MEMS filters [1]. Vertically integrated monolithic 3D radio-frequency integrated circuit (RFIC) [2], which builds MEMS filters on top of RFIC devices, holds the potential to achieve high density. However, to build MEMS filters monolithically on top of RFIC, various integration problems must be solved. One major issue is the thermal budget of the CMOS backend of the line (BEOL) due to the out diffuse of copper at high temperature, which limits the fabrication process of MEMS devices to below 400°C [3]. This not only restricts the choice of piezoelectric materials for MEMS fabrications but also poses challenges for forming acoustic cavities in MEMS filters. For piezo materials, sputtered AlN is CMOS compatible and has been used in commercialized standalone MEMS devices [4]. Previous research effort has been carried out to integrate ALN based MEMS devices on the BEOL of CMOS [5]. Compared to AlN, Scandium doping into aluminum nitride with similar thermal budget on processing, shows higher piezo electrical coupling constant, higher acoustic velocity, and thermal conductivity. These superior properties make ScAlN more suitable in high power handling, high frequency, and wide band applications areas [6]. Details on producing high quality CMOS compatible ScAlN can be found in our precious work [7]. Apart from piezoelectric materials, formation of the acoustic air cavity is another challenge in the MEMS and COMS integrated system. The well-established deep reactive ion etching [8] or bulk micromachining [9] are not applicable in the monolithic system. Surface micromachining method [10] which involves deposition and patterning sacrificial material, following by a structural layer that forms the walls of the cavity can be used, but improvements are still needed. In traditional surface micromachining, the sacrificial materials are usually SiO_2 and amorphous Si. And in the final step, gas phase etchant was used such as vapor phase HF etching and vapor phase XeF_2 etching to etch away the sacrificial materials. In monolithic integrations, due to the high corrosivity of VHF to SiO_2 which is the dielectrics and structure material in the BEOL, XeF_2 releasing chemistry are mostly used to avoid the CMOS devices from being damaged in release process [11]. The limitations of XeF_2 comes from the corrosivity of the etchant, as such the design and material selection of metal electrodes for the RFMEMS devices. On top of that, the low temperature amorphous Si faces adhesion issue to the MEMS devices. To address this issue, extra layer of nitride is required in between the sacrificial material and the MEMS electrode, which imposes global loading on the MEMS device [12]. Other approaches such as using metallic barriers and with sacrificial material of SiO_2 have also been used for CMOS backend device fabrications, which compromised device performance due to the significant parasitic, especially in high frequency range [13].

In this paper, we report an integration scheme using SiO_2 as sacrificial material for robust integration of ScAlN based MEMS device on the top of CMOS wafers. Since SiO_2 is also the structure materials for CMOS, a layer of Al_2O_3 deposited by atomic layer deposition at 300°C was used as barrier to stop the etch during final sacrificial material removal by VHF. In order to verify the compatibility of the proposed integration scheme, ScAlN based thin film bulk acoustic resonators (FBAR) bandpass filters were utilized as test vehicles and fabricated. RF characterization are performed, and the results are presented, which demonstrated low-temperature barrier for manufacturing MEMS devices at BEOL of CMOS.

INTEGRATION DESIGN AND FABRICATIONS

Figure 1 illustrated the monolithic integration of ScAlN MEMS filter on CMOS which is a RFSOI. A ScAlN thin film based bulk acoustic wave filter was fabricated direct on top on the CMOS wafer. An acoustic cavity was formed in between the CMOS and MEMS device. The surrounding structural material was SiO_2. To prevent the structural SiO_2 from being etched during the process, a barrier layer was deposited to define the cavity etch.

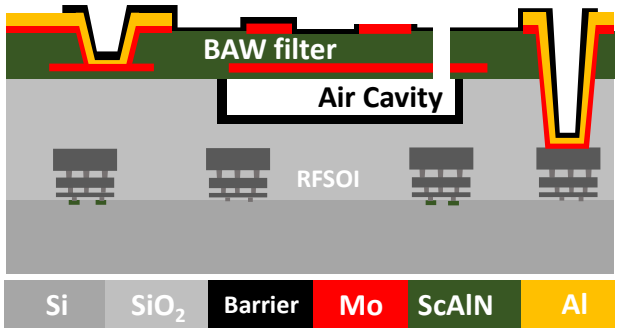

Figure 1. Cross-section schematic of a monolithic integrated ScAlN MEMS filter on RFSOI

For the realization of the structure shown in the illustration, the integration was started with the CMOS finishing wafer. from GlobalFoundries (GF) Singapore. The functionality of the circuit is single pole double throw (SDPT) RF switch. With multi TEOS depositions and CMP, the gaps between final metal lines are properly filled and planarized. Figure 2 (a) shows the starting wafer surface for MEMS device fabrications. After that, a layer of 2-um-thick TEOS oxide was deposited as structural ankles. A swimming pool was then pattern and time etched with thickness control of 1um. To protect the ankle area, a layer of 150 nm thick A_2O_3 was deposited by atomic layer deposition. After that, a sacrificial layer of TEOS with thickness of 1.2um was deposited uniformly on the wafer, filling the swimming pool. A reverse pattern to the swimming pool was printed and etch back. Chemical Mechanical Planarization was further carried out to planarize surface. Ideally the CMP should stop on the surface of the barrier material of Al_2O_3 at ankle area. However due to the pool selectivity of SiO_2 CMP slurry to Al_2O_3, the accurate stop is not possible. The barrier at the ankle area was removed, leaving the vertical barrier shown in Figure 2 (b).

The barrier at the ankle area was removed, leaving the vertical barrier shown in Figure 2 (b). The MEMS device was further fabricated, with layer stacks and thickness of AlN (20 nm) / Mo (150nm) / ScAlN (1um) / Mo (150nm). The 20 nm AlN not only serves as the purpose of seed layer for better growth of the piezoelectric ScAlN, but also enhances the adhesion of the piezoelectric stack on top. During the fabrication of the MEMS stack, a taped side wall profile of bottom Mo is important. In order to achieve a taped side wall, other than changing the gas composition and etch rate, a reflow of resist was also used. After deposition of ScAlN, two sets of Vias with different sizes were formed. The smaller set of Vias were etch stop on bottom Mo to access bottom electrodes of MEMS devices shown in Figure 2 (c). For Via access to bottom Mo, it is important to control the etch to minimize the loss of bottom electrode to get good electric contact.

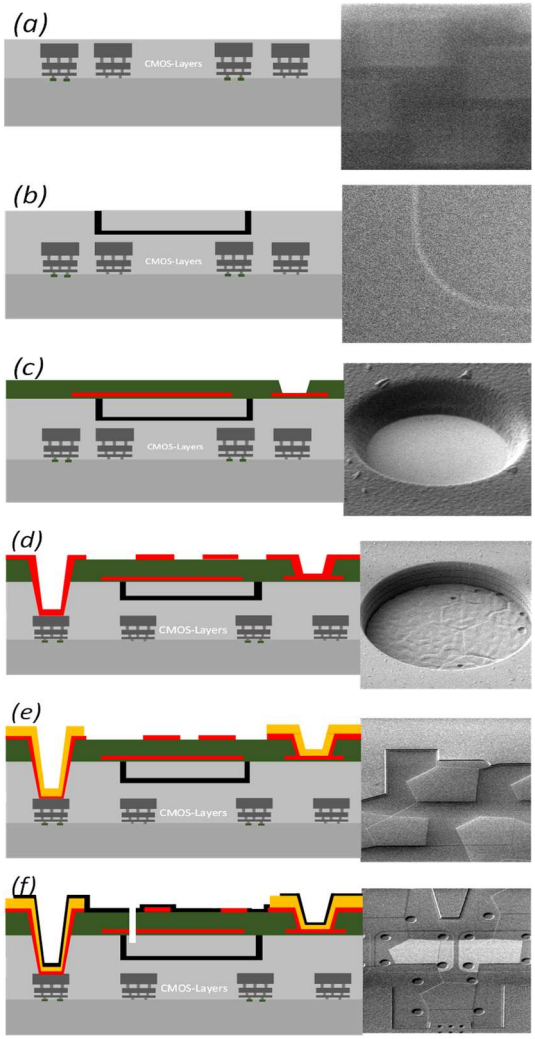

Figure 2. Process flow for monolithic integration of MEMS (a) Planarize CMOS wafer, (b) Cavity formation, barrier and sacrificial filling and planarization, (c) Bottom electrode formation, piezo layer deposition and Via 1, (d)Via 2 etch stop on top metal of CMOS and top electrode formation, (e) Pad formation and Metallization, (f) Mass loading, passivation, and release trench

From the SEM images, it is clearly shown that the Mo suffer limited damage from ScAlN etch. For the Vias with bigger diameter, the top ScAlN was etched together with the smaller Vias. A thick oxide etch was then used to punches through >3-um-thick layers SiO_2 to reach the top metal of RFSOI shown in Figure 2 (d). The different sizes of Vias to access different layers are important for the metallization. Although the etch profile of the large Via is vertical, after a 150 nm top Mo deposition, in line testing shows connection was formed from MEMS device to RFIC, with a resistance at the order of hundreds of ohms. This resistance was decreased to the level of tens of ohms after further passivation layer and metallization layer formation. After the metallization of MEMS filter, a final layer of Al_2O_3 deposited. This layer of Al_2O_3 not only serves purpose of mass loading tunning but also passivate

the whole wafer. The VHF gas sent through the release holes shown in Figure 2 (f) the release the resonators in a controlled manner.

Shown in Figure 3 (a) is the cross-sectional image of the integrated FBAR device on top of the RFIC switch before release. The grey color trapezium is the top metal of the RFIC. On top of the top metal, a swimming pool can be observed with a thin layer of slight brighter contrast covering the bottom and side wall of the swimming pool, which is the barrier layer deposited by ALD. A slight deep can be observed due to the CMP etching. Figure 3 (b) shows a microscopic image of a FBAR device after release. From the different contrast of the top/dummy metal of RFIC inside and outside the barrier, it can be told that the sacrificial TEOS oxide underneath the FBAR devices are full etched. And the barrier effectively confined the etchant within the swimming pool without attacking the ankle and structural TEOS oxide.

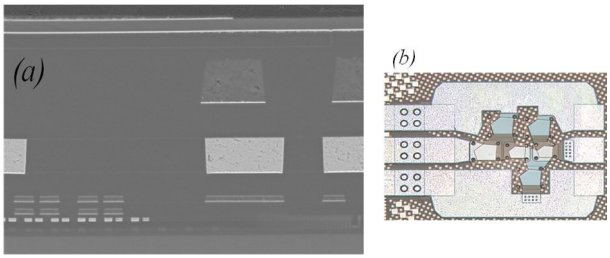

Figure 3. (a) Cross section view of monolithic integrated MEMS filter before release (b) Microscopic image of monolithic integrated MEMS filter after release

Shown in Figure 4 is an illustration of RF SOI switch integrated with a FBAR filter, built using seven resonators in a ladder configuration.

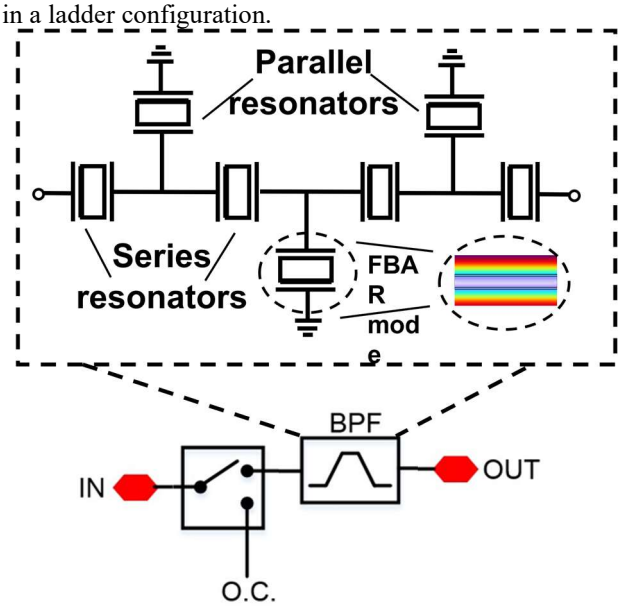

Figure 4. Illustration of MEMS filter with RFIC

The characterization of the integrated switched FBAR filter was carried out with a frequency range of 2.0 GHz to 3.2 GHz and an input power of -17 dBm. The output was captured by Keysight N5244B PNA. The results of the testing are shown in Figure 5. An insertion loss of 3.57 dB and a bandwidth of 128 MHz at center frequency of 2.57 GHz was obtained. The filter demonstrated excellent isolation with a difference of up to 30 dB between the RF switch being on and off.

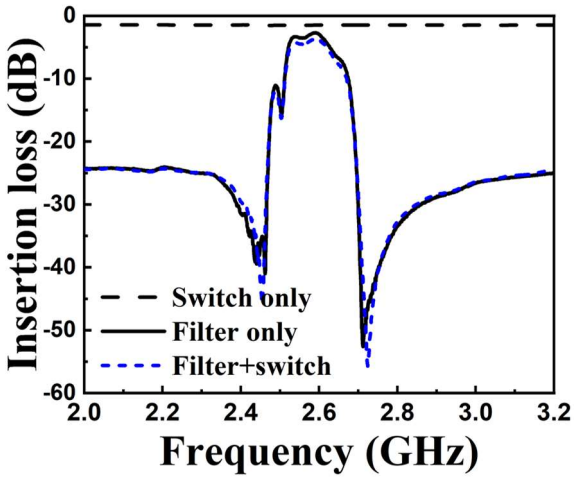

Figure 5. Insertion loss of MEMS filters only and with RF switch

CONCLUSION

A ScAlN-based BAW filter was monolithically integrated on the BEOL of RFIC with TEOS as a sacrificial layer. A thin layer of ALD-deposited Al_2O_3 was successfully used to isolate the structural TEOS from being attacked during sacrificial layer etching using VHF. This integration scheme offers three major advantages compared to other integration schemes. First, the acoustic cavity embedded in a dielectric minimizes unwanted RF coupling or RF loss due to the anchor and barrier materials being dielectrics. Second, the acoustic cavity and dielectric anchor were formed on top of planarized isolation dielectric, minimizing stress in the barrier material due to topography from the CMOS end surface. This results in higher reliability compared to literature work that uses metal of CMOS as an anchor for MEMS devices. Additionally, this work has no limitations on MEMS device design and material selection for MEMS devices, thanks to the fully encapsulated cavity by barrier material. Lastly, the process temperature of the whole flow is way below 400°C, making the material fully compatible with CMOS, ensuring a monolithic compatible process. The integrated switched BAW filter shown an insertion loss of 3.57 dB and a bandwidth of 128 MHz at 2.57 GHz was obtained. The filter demonstrated excellent isolation with a difference of up to 30 dB between the RF switch being on and off.

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