# Systematic Signal Integrity Analysis on Fine Pitch Probe Card for HBM Interposer Testing

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## Abstract

High bandwidth memory (HBM) has overcome the limitations of conventional DRAMs. It can support terabyte/s data transmission between GPU and HBMs with 2.5D packaging technology. To ensure the high-speed data transmission between the HBM and GPU, the signal integrity (SI) of the HBM interposer with many I/O interconnects needs to be tested with the customized fine-pitch probe card. However, SI problem is found on the probe card when the full-wafer SI test is performed on the HBM interposer. This paper demonstrates that the SI of the probe card for HBM interposer testing needs to be considered. Moreover, this paper introduces a comprehensive methodology to discover and localize the SI problem in the HBM interposer testing through the systematic SI analysis.

## Introduction

The testing on HBM interposer is very challenging due to the probe card cost, contact reliability, high probe force, micro-bump damage and SI [1-4]. Especially, [5, 6] have emphasized the significance of maintaining the SI of a probe card from an early design stage for wafer-level high-speed test. However, the probe card manufacturers have to make tradeoff between the SI and space, which means routing more probe channels can lead to poor SI. On the other hand, probe card users normally do not participate the probe card design in details. If the probe card's SI is not guaranteed, the high-speed performance of the HBM interposer cannot be revealed since the high insertion loss and crosstalk of the probe card will dominate the test results. Thus, it is important and practical for the probe card end user to learn about the probe card's SI performance when testing the HBM interposer.

Fig. 1 shows the HBM interposer with 24 interconnects and the illustration of the fine pitch probe card side view. On the each side of the HBM interposer, there are 24 signal and 24 ground micro-bumps for the contact to the input/output and ground ports of the fine pitch probe card. The 24 interconnects have the similar length of 3320 um and they form as the microstrip lines with the ground plane underneath. Each interconnect has width and thickness of 2 um. The spacing between the HBM interconnects ranges from 4.7 to 40 um. The probe card consists of PCB and Multilayer Organic (MLO) layers. The MLO layer is a transition layer to accommodate the probe card interconnects with narrower spacing and finer cross-section in between the probe pins and the PCB layer.

Fig. 2 shows the detailed testing connection from the probe card input ports (P1 to P24) to output ports. When testing a HBM line with the high-speed digital signal, the signal has to go through a PCB line, a MLO line, the HBM line, another MLO line and another PCB line. The high-speed digital signal is the pseudo random binary sequence (PRBS). The PRBS data rate is 1 Gbps and the voltage swing is from -250 to 250 mV. The PRBS rise time is 40% to 50% of the unit interval (UI).

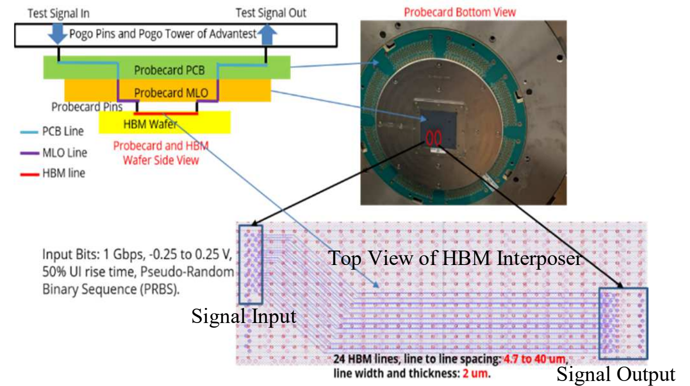



Fig. 1. Illustration of HBM interposer and probe card

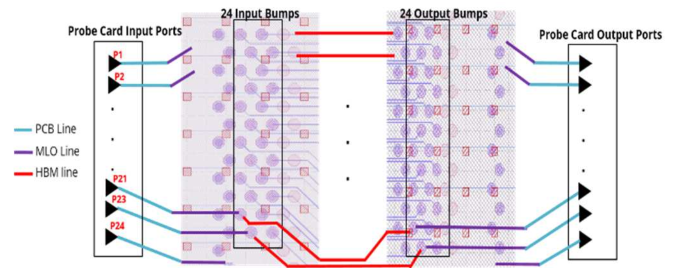



Fig. 2. Interconnect of probe card PCB, MLO and HBM lines

With aforementioned measurement setup, the full-wafer high-speed testing is conducted on a wafer full of HBM interposer dies. The testing results are the eye diagrams, which are also known as shmoo plots in automated test equipment (ATE) testing. For the testing on a HBM interposer die with 24 interconnects in Fig. 1, there will be 24 eye diagrams generated from each testing on a HBM interposer.

This paper describes how the SI problem of the probe card is identified by analyzing the tested eye diagrams and SI simulations for the interconnects of the HBM interposer and the probe card.

## Eye Diagram Measurement of HBM Interposer

The eye diagrams of the whole wafer are measured and the eye diagrams of 2 HBM interposer dies (Die 1 and Die 2) are taken as examples for analysis and discussion. Among the 24 eye diagrams tested from each die, 2 eye diagrams are found to be unusually small compared to the other 22 eye diagrams. Table 1 and Table 2 show the eye diagrams info of 4 different interconnects from Die 1 and Die 2, respectively. In Tables 1 and 2, EA means eye amplitude. Fig. 3 shows the measured eye

diagrams of 4 different interconnects from Die 1 and Die 2. The comparisons in tables and Fig. 3 show that tested channels P21 and P23 (channel numbering refers to Fig. 2) have much smaller eye opening compared with the eye diagrams of P5 and P9, which represent the normal eye diagrams of the other 22 interconnects (P22, P24 and P1 to P20).

Table 1. Eye height and eye width comparison of 4 interconnects in Die 1

| Channel # (Die 1) | Eye Width (ps) | Eye Height (mV) |
|---|---|---|
| P5 | 787 (78.7% UI) | 225 (45% EA) |
| P9 | 840 (84% UI) | 225 (45% EA) |
| P21 | 761 (76.1% UI) | 137 (27.4% EA) |
| P23 | 709 (70.9% UI) | 112 (22.4% EA) |

Table 2. Eye height and eye width comparison of 4 interconnects in Die 2

| Channel # (Die 2) | Eye Width (ps) | Eye Height (mV) |
|---|---|---|
| P5 | 777 (77.7% UI) | 230 (46% EA) |
| P9 | 840 (84% UI) | 230 (46% EA) |
| P21 | 735 (73.5% UI) | 130 (26% EA) |
| P23 | 714 (71.4% UI) | 100 (20% EA) |

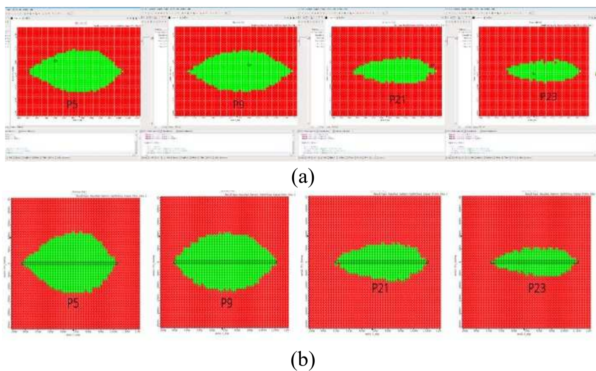


Fig. 3. Eye diagrams of tested channels P5, P9, P21 and P23 on (a) Die 1 (b) Die 2

## SI Analysis on HBM Interposer and Probe Card

The comparison shown in Fig. 3 confirms that 2 HBM interconnects and the corresponding probe card interconnects on P21 and P23 has SI problems. However, it cannot identify whether it is the SI problem of the probe card interconnects or the HBM interconnects. Normally, the HBM interconnects routed in the middle suffer the most severe SI problem, such as the P12 and P13 channels. However, the tested eye diagrams show that the problematic channels are P21 and P23, where the corresponding HBM interconnects are routed at the side area of the HBM interposer in Fig. 2. Thus, the HBM interconnects are unlikely to be the root cause to the unusually small eyes in Fig. 3. To further investigate and localize the SI problem, a series of simulations for the probe card interconnects (PCB and MLO interconnects) and HBM interposer interconnects are done in both time and frequency (from 0.1 to 30 GHz) domains.

Firstly, the S-parameter simulation is done to analyze the insertion loss (IL) and far-end crosstalk (FEXT) of the interconnects in HBM interposer, PCB and MLO layers. The S-parameter simulation model of each type of interconnect covers 7 lines and the simulations are done in Ansys Q3D. Fig. 4 shows 7-line model of the HBM interconnects in Ansys Q3D. The S-parameter results shown in subsequent figures refer to S-parameter of the center line (line 4 in Fig. 4) of the 7-line model. Table 3 shows the cross-sectional info and length of three types of interconnects. The line length in Table 3 refers to the length of a single interconnect. For the length of PCB or MLO interconnect, it refers to the total length of the left and right sections of the probe card in Fig. 1. The minimum line spacing of the HBM interconnects (4.7 um) is selected for the HBM model simulation. However, the probe card vender cannot provide the minimum line spacing of the MLO and PCB interconnects. To complete the simulation models of the MLO and PCB interconnects, the line spacing is assumed to be one line width.

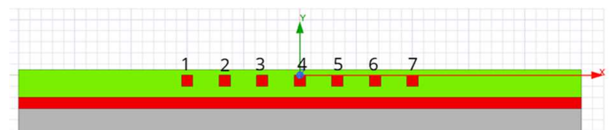
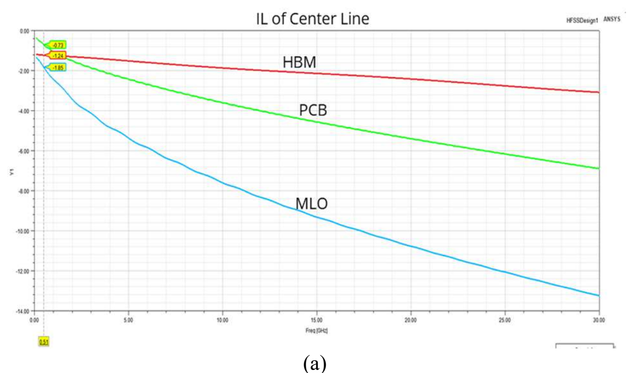



Fig. 4. 7-line model of the HBM interconnects

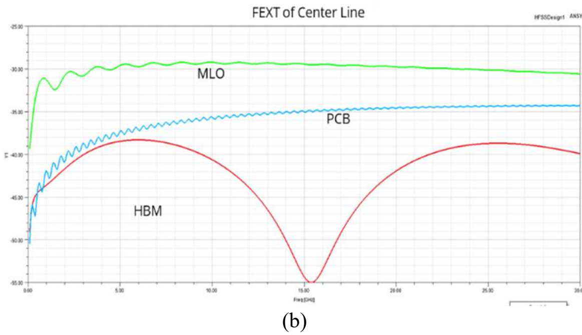
Table 3. Cross-sectional info and length of HBM, PCB and MLO interconnects

| Line Type | Line Width (um) | Line Thickness (um) | Line Length (cm) | Line Spacing (um) |
|---|---|---|---|---|
| HBM | 2 | 2 | 0.332 | 4.7 (minimum) |
| MLO | 10 | 6.5 | 5.44 | 10 (assumed) |
| PCB | 130 | 13 | 19.81 | 130 (assumed) |

The simulated IL and FEXT of the HBM, PCB and MLO interconnects are shown in Fig. 5.




(a)

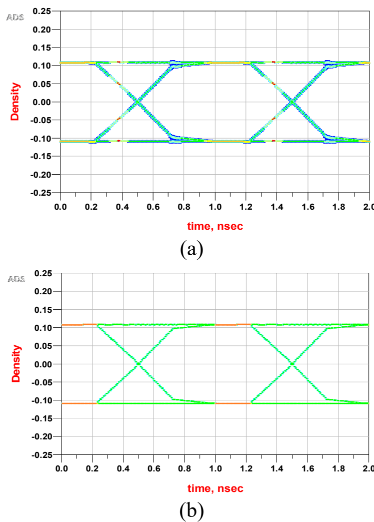



(b)

Fig. 5. Simulated (a) IL (b) FEXT

Fig. 5 shows that the MLO interconnects have the highest IL and FEXT, which means the MLO interconnects have the worst performance among the three types of interconnects. The HBM interconnects have the smallest IL and FEXT. The IL and FEXT difference between the MLO and HBM interconnects explains that the MLO interconnects have the most significant impact on the eye height and eye width of the eye diagram. Thus, the high-speed performance of the HBM interconnects will be masked by the high-speed performance of the MLO interconnects. In other words, the tested eye diagrams in Fig. 3 is mainly demonstrating the high-speed performance of the testing equipment (probe card) instead of the device under test (HBM interposer).

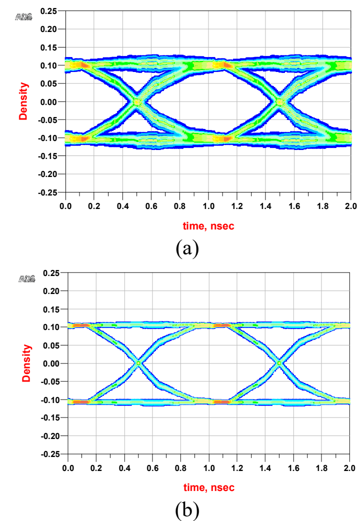
The frequency domain simulations confirm that the probe card's MLO interconnects cause the small eye opening of channels P21 and P23. To localize the root cause of the small eye opening, the time domain (eye diagram) simulations with different line spacing are done in ADS and the simulated eye diagrams of the center interconnect of different models are shown in subsequent figures. Since the line spacing of the HBM interconnects range from 4.7 to 40 um, the eye diagrams of the smallest and largest line spacing can be simulated and shown in Fig. 6.




(b)

Fig. 6. Eye diagrams of HBM interconnects (a) 4.7 um spacing (eye height: 208 mV, eye width: 971 ps) (b) 40 um spacing (eye height: 211 mV, eye width: 984 ps)

Fig. 6 shows that the eye height and eye width only increases by 1.4% when HBM line spacing increased from 4.7 um to 40 um. It means that the line spacing variation of the HBM interconnects has insignificant impact on SI. Hence, the small eye opening of P21 and P23 is not caused by the difference of the HBM line spacing. Since the PCB interconnects have the largest interconnect cross-section area and largest line spacing among the three types of interconnects, there is no need to do the eye diagram simulation for PCB interconnects with line spacing variation. For the eye diagram simulations of the MLO interconnects, the maximum and minimum line spacing is assumed to be 10 and 5 um, respectively. The simulated eye diagrams of MLO interconnects with line spacing of 5 and 10 um are shown in Fig. 7.




(b)

Fig. 7. Eye diagrams of MLO interconnects (a) 5 um spacing (eye height: 155 mV, eye width: 870 ps) (b) 10 um spacing (eye height: 191 mV, eye width: 950 ps)

Fig. 7 shows that the eye height and eye width only increases by 23% and 9% when MLO line spacing increased from 5 um to 10 um. Thus, the small eye opening in P21 and P23 can be caused by the variation of the MLO line spacing.

To further demonstrate the impact of the MLO line spacing, eye diagram simulations combining the PCB, MLO (spacing of 5 and 10 um) and HBM models are done. Fig. 8 shows the eye diagram simulation setup in ADS. Fig. 9 shows the simulated eye diagrams of the combined interconnects with different MLO line spacing (5 and 10 um).

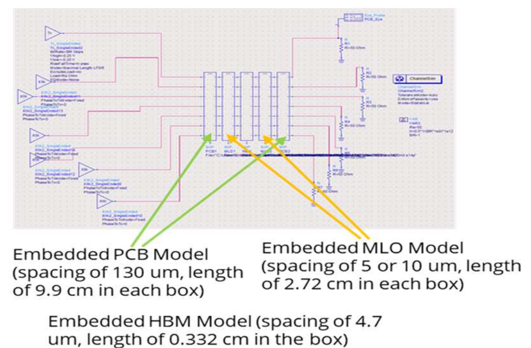



Fig. 8. Eye diagram simulation setup in ADS for combined interconnects

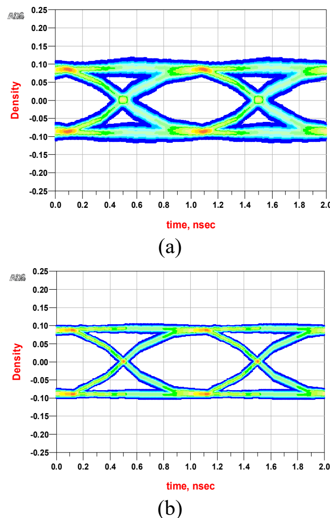



Fig. 9. Eye diagrams of combined interconnects (a) 5 um spacing of MLO interconnects (eye height: 122 mV, eye width: 828 ps) (b) 10 um spacing of MLO interconnects (eye height: 145 mV, eye width: 925 ps)

Fig. 9 shows that the MLO line spacing will still dominate the eye diagram pattern even PCB and HBM interconnects are taken into consideration.

To prove the aforementioned deductions from the simulations, the high-speed testing setup of the ATE is changed. If P21 and P23 of the probe card are problematic, the same HBM interconnects originally in contact with P21 and P23 will show larger eye opening when using other probe card pins to contact the HBM interconnects. Fig. 10 shows two different setup for the HBM interposer testing. B21 and B23 refer to the micro-bumps originally in contact with P21 and P23 of the probe card. Setup 1 is the original setup which shows P21 and P23 with small eye opening. Setup 2 is the new setup which avoids the problematic probe card channels (P21 and P23) to contact the HBM interconnects. In Setup 2, the HBM interposer wafer is moved along the arrow direction by 96 um so that P21 and P23 are not in contact with the HBM interconnects. Table 4 shows the tested eye height and eye width of setups 1 and 2.

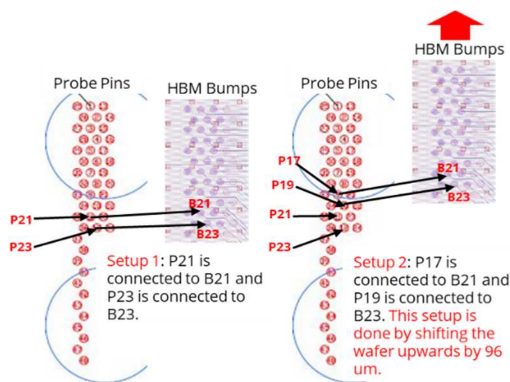



Fig. 10. Two different setup for HBM interposer testing

Table 4. Tested eye height and eye width of setups 1 and 2

| Setup # | Eye Height (mV) | Eye Width (ps) |
|---|---|---|
| 1 | B21: 137 | B21: 761 |
| | B23: 112 | B23: 709 |
| 2 | B21: 225 (increased by 64%) | B21: 840 (increased by 10%) |
| | B23: 163 (increased by 46%) | B23: 788 (increased by 11%) |

Table 4 shows that significant eye height and eye width increase is demonstrated by changing the probe card channel connection on the HBM interconnects. It is further confirmed that the narrow MLO line spacing of P21 and P23 interconnects causes the small eye opening. The root cause of the eye diagram difference is discovered and localized through systematic simulations and measurements.

## Conclusion

With the systematic SI analysis on the probe card and HBM interconnects, the problematic probe card channels causing the SI problem on the testing results are found. When the SI problem of the testing equipment is identified, the engineers doing the full-wafer high-speed test will not be misled by the tested eye diagrams and think it is the wafer's problem. The fine pitch probe card must have SI problem on some testing channels, foundries as the end users of the fine pitch probe card cannot mitigate the SI problem because the probe card's physical configuration cannot be changed. However, it is very significant and helpful to learn about the SI nature of the probe card before the massive high-speed wafer testing starts. Once the worst testing channels are found, testing engineers can change the ATE setup accordingly like Fig. 10 to avoid using the problematic channels.

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