GaN-on-Si HEMT Technology for mm-Wave Mobile T/R Modules Demonstrating Concurrent High Efficiency (>60 %) and Low Noise (<1.2 dB)

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***Abstract*—This Letter reports a GaN-on-Si HEMT technology with 60 to 150 nm T-gate achieving simultaneous high efficiency and low noise at low voltage (3−6 V) RF operation, suitable for monolithic integrated FR2 mobile Transmit/Receive (T/R) modules. At 30 GHz and V_{DS} = 5 V, in continuous wave operation, the fabricated L_g = 100 nm device delivered a saturated output power of 1.2 W/mm with a record-high peak power-added efficiency (*PAE*) of 62% while maintaining a state-of-the-art minimum noise figure (NF_{min}) of 1.1 dB. Enabled by the optimized epitaxial structure and fabrication process, the proposed technology, even with moderate scaling, offers a cost-effective solution for FR2 T/R modules.**

***Index Terms*—InAlN/GaN, HEMTs, low voltage application, FR2.**

I. Introduction

The mm-wave range is highly attractive for future high data rate wireless communication, yet existing technologies such as SiGe HBT and GaAs pHEMT struggle to meet the stringent requirements. GaN-on-Si HEMT technology, with its low-cost and large-scale, has emerged as a strong candidate, particularly for mobile applications where a high-volume market exists. GaN-on-Si HEMTs have demonstrated high saturated power (P_{sat}) and power-added efficiency for V_{DS} ≤6 V (handset) [1], [2], [3], [4], [5], [6], [7], [8], [9], while noise performance with minimum noise figures (NF_{min}) below 1.5 dB has also been reported separately [2], [10], [11], [12], [13]. However, monolithic integration of both power amplifier (PA) and low-noise amplifier (LNA) would offer superior performance over discrete power-bar and wire-bonding. This requires a single technology that meets both demands, an area where only a few studies have been reported [2], [10], [14].

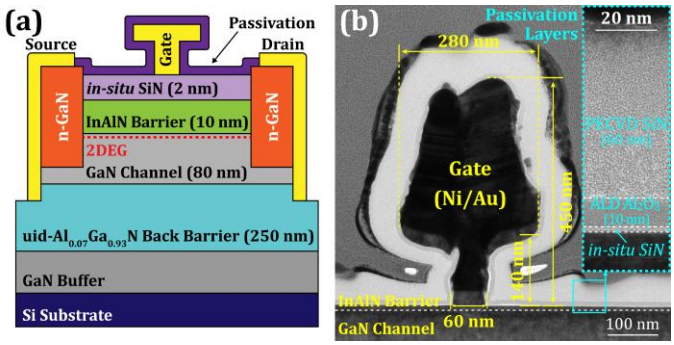

Fig. 1. GaN-on-Si HEMT technology proposed in this work. (a) Device structure. (b) Transmission electron microscopy (TEM) image of the T-gate and bilayer passivation.

Most previously reported HEMTs rely on aggressive lateral scaling, with gate length (L_g) below 100 nm and source-drain distance (L_{SD}) below 1 µm [2], [3], [4], [5], to achieve low on-resistance (R_{on}) and high frequency performance. It is noted that scaling down brings challenges in mass manufacturability on top of the limitations of the short channel effect and reliability. Key characteristics for low-voltage operation, such as contact resistance, electron confinement, and trapping effects, can also be significantly improved through optimization of the epitaxial structure and fabrication process [5], [8], [15].

This work presents a GaN-on-Si HEMT technology based on an InAlN/GaN/AlGaN epitaxial structure suitable for monolithic integration of FR2 mobile T/R modules, which demand high efficiency and low noise. Thanks to its low sheet resistance, vertical scaling, enhanced electron confinement via the ultra-thin channel and back barrier (BB), together with regrown ohmic contacts and bilayer passivation stack, the devices demonstrate efficiency exceeding 60% and NF_{min} below 1.2 dB, while maintaining moderate lateral scaling compatible with cost-effective production.

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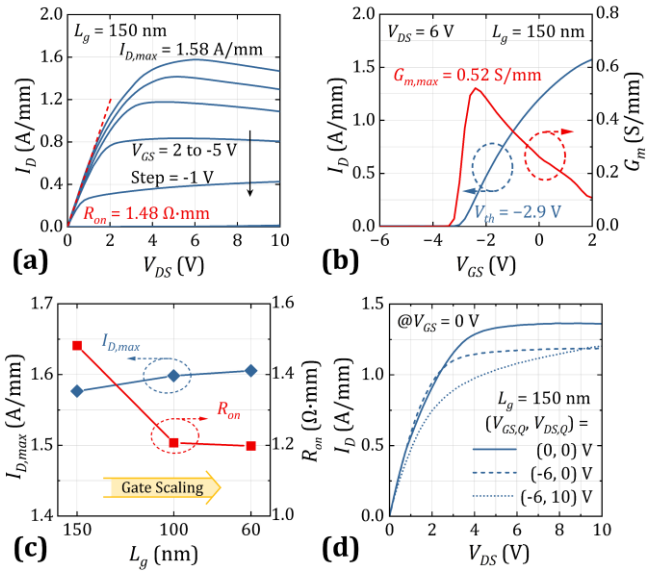

Fig. 2. DC and pulsed characteristics of the proposed HEMTs. (a) Output and (b) transfer curves of the L_g = 150 nm device. (c) Variation of $I_{D,max}$ and R_{on} with L_g scaling. (d) Pulsed IV characteristics.

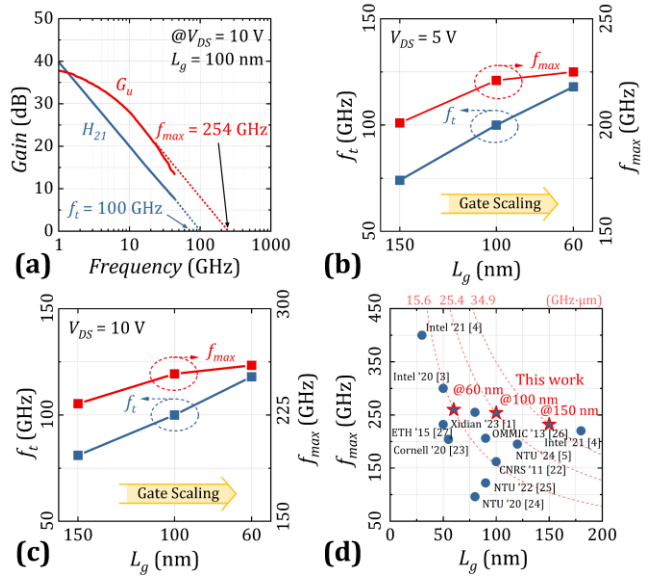

Fig. 3. Small-signal characteristics of (a) the L_g = 100 nm device with its ft/f_{max} = 100/254 GHz after de-embedding. Extracted f_t/f_{max} with L_g scaling at (b) V_{DS} = 5 V and (c) V_{DS} = 10 V. (d) Benchmark of f_{max} vs. L_g with the product indicated as dashed line.

II. Device Technology

The GaN epitaxy used in this work is grown on a 6-inch high-resistivity Si (>5 kΩ·cm) by metal-organic chemical vapor deposition (MOCVD). From top to bottom, the structure comprises a 2 nm SiN cap, a 10 nm InAlN barrier, an ultra-thin (80 nm) GaN channel, and a 250 nm unintentionally doped AlGaN BB (5% Al), followed by a C-doped GaN buffer optimized for RF performance. The InAlN barrier provides strong polarization and a low gate-to-channel distance, enabling improved two-dimensional electron gas (2DEG) control. Additionally, the configuration of the ultra-thin GaN channel and the AlGaN BB further enhances electron confinement, effectively suppressing short-channel effects and lowering channel noise [15]. Non-contact Hall measurements show a carrier sheet density (N_s) of 2.3×10^{13} cm^{-2}, electron mobility (μ) of 1440 cm^2/V·s, and sheet resistance (R_{sh}) of 190 Ω/□.

The fabrication began with mesa isolation using Cl_2-based plasma etching. A hard mask consists of 200 nm SiO_2 and 80 nm SiN by PECVD was deposited for the regrown ohmic contacts, followed by lithography and 50 nm Cl_2-based etch (etch rate of ~1.5 nm/s). Subsequently, an 80 nm Si-doped regrown n-GaN layer was deposited by molecular beam epitaxy (MBE) at 725 °C, followed by buffered oxide etch (BOE) lift-off. By TLM measurements, a total contact resistance of 0.12 Ω·mm was obtained, of which 0.04 Ω·mm was attributed to the n-GaN/2DEG interface.

Metal-insulator-semiconductor (MIS) gate stack was then formed by T-gate (Ni/Au, 30/330nm), while preserving the thin (2 nm) *in-situ* SiN. At the end, a bilayer passivation stack consisting of 10 nm thermal ALD Al_2O_3 at 250 °C and 60 nm PECVD SiN at 300 °C was applied to suppress surface trapping and leakage [16]. Devices with L_{SD} of 2 μm, gate width (W_g) of 2×25 μm, and different L_g of 60, 100, and 150 nm were fabricated and characterized. Fig. 1(b) presents the cross-sectional view of the fabricated device.

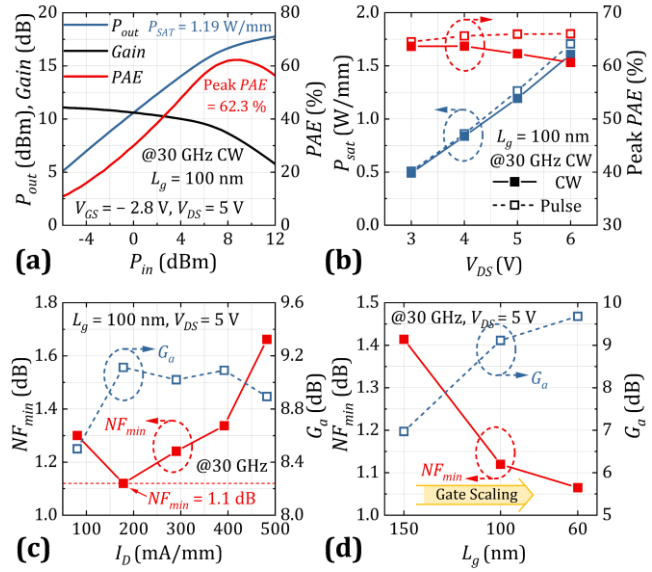

Fig. 4. Power and noise performance of the L_g = 100 nm device at 30 GHz. (a) Power performance at V_{DS} = 5 V. (b) Summary of P_{sat} and peak *PAE vs.* V_{DS} in both CW and Pulsed modes. Excellent efficiency (> 60%) is achieved. (c) NF_{min} and G_a vs. I_D, achieving NF_{min} of 1.1 dB. (d) Improvement of noise performance by the L_g scaling.

III. DC and Small-Signal Characteristics

The L_g = 150 nm device achieves a maximum drain current ($I_{D,max}$) of 1.58 A/mm, R_{on} of 1.48 Ω·mm, threshold voltage (V_{th}) of −2.9 V, and peak transconductance ($g_{m,max}$) of 0.52 S/mm at V_{DS} = 6 V (Fig. 2(a) and 2(b)). Their DC characteristics follows the typical scaling trend as shown in Fig. 2(c). The effectiveness of the bilayer passivation is confirmed by pulsed IV measurements, showing gate lag of 10% and current collapse of 24% (extracted at (V_{GS}, V_{DS}) = (0, 4) V), compared to >80% before the passivation (Fig. 2(d)).

The small signal characteristics were measured on passivated devices with various L_g. Fig. 3(a) shows the measured small-signal characteristics for the L_g = 100 nm device after de-

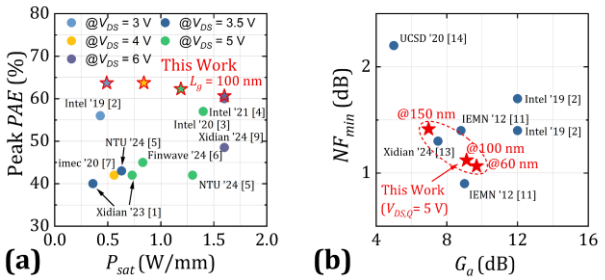

Fig. 5. Benchmark of the power and noise performance of the characterized devices with reported GaN-on-Si HEMTs at 26 − 30 GHz. (a) Peak *PAE* vs. P_{sat} at low voltage (≤6 V). Record high efficiency (>60 %) is achieved in this work. (b) NF_{min} vs. G_a. State-of-the-art noise performance (1.1 dB) is achieved by this at L_g = 100 nm (without extreme lateral scaling).

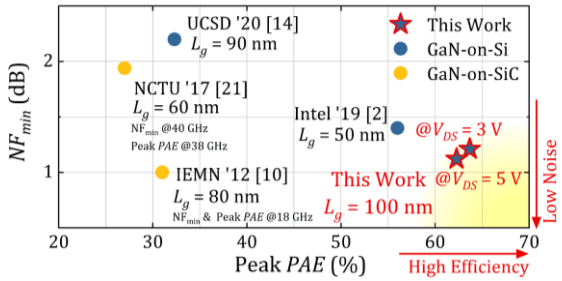

Fig. 6. Benchmark of NF_{min} vs. Peak *PAE* of the GaN HEMTs at ~30 GHz, unless otherwise stated. Reports of simultaneous power and noise are included.

embedding. Owing to the reduced parasitic resistance, high transconductance, and well-designed gate structures, the devices exhibit f_{max} > 200 GHz at V_{DS} = 5 and 10 V. As L_g scales, f_t continually increases, while f_{max} improves until saturates at 60 nm (Fig. 3(c)–(d)). A similar trend is evident in f_{max} vs. L_g benchmark (Fig. 3(d)). Although a larger L_{SD} is adopted, the L_g = 150 nm device still achieves an excellent $f_{max} \times L_g$ of 34.9 GHz·μm which is comparable to the highest reported values obtained from extremely scaled GaN-on-Si HEMTs.

IV. Power and Noise Performance

Large-signal power performance was characterized on the L_g = 100 nm device under both continuous-wave (CW) and pulsed conditions at 30 GHz. The device is biased at V_{GS} = −2.8 V, corresponding to the peak f_{max}, and V_{DS} = 3-6 V to evaluate its performance in low voltage. Despite the larger L_{SD} (2 μm *vs.* <0.8 μm) and the consequently higher R_{on} (1.2 Ω·mm *vs.* <0.5 Ω·mm) compared to some aggressively scaled reported devices, this work demonstrates decent power performance under low voltage operation. Under CW mode, the device delivers a P_{sat} of 1.19 W/mm, linear gain of 11.1 dB, and peak *PAE* of 62.3% (Fig. 4(a)). Fig. 4(b) summarizes the power performance measured under both CW and pulsed modes, showing peak *PAE* >60% across the low-voltage range. The maximum *PAE* of 63.7% is achieved at V_{DS} = 3 and 4 V. Thanks to the effectiveness of the proposed bilayer passivation in suppressing surface trapping effects, no significant difference in performance is observed between CW and pulsed modes. The L_g scaling improves the linear gain from 10.8 dB on L_g = 150 nm device to 14.7 dB on L_g = 60 nm device, while maintaining the high peak *PAE* and P_{sat}. The high efficiency in low-voltage operation proves its potential for mobile applications.

Low-noise performance was characterized by using a cold-source noise measurement system. At V_{DS} = 5 V, the transistors achieve an optimal balance between low noise and high associated gain (G_a). The excellent electron confinement, high gain, and low parasitic resistance, enabled by the ultra-thin channel, AlGaN BB, and regrown ohmic contacts, result in outstanding low-noise characteristics (NF_{min} < 1.4 dB) across FR3 to FR2 bands from 10 to 40 GHz, even without aggressive lateral scaling. The NF_{min} of 1.1 dB (0.8 dB), corresponding to G_a of 8.3 dB (14.1 dB), is achieved at 30 GHz (13 GHz) (Fig. 4(c)). The scaling of the L_g is proven favorable to improve noise performance, with the NF_{min} decreasing from 1.4 dB to 1.1 dB and G_a increasing from 6.9 dB to 9.7 dB at 30 GHz (Fig. 4(d)).

The low-voltage power and noise performance at 30 GHz are benchmarked separately in Fig. 5. To the best of the authors' knowledge, the L_g = 100 nm device, while achieving competitive P_{sat}, demonstrates the record high peak *PAE* across all benchmarked V_{DS}, with larger L_{SD} and L_g. The InAlN barrier provides high electron density and mobility, and the regrown ohmic contact further reduces contact resistance, enabling low R_{on} and high saturation current without extreme device scaling. This combined optimization on epitaxial structure and process yields competitive output power under low-voltage operation. The thin barrier, ultra-thin channel, and BB configuration offer excellent intrinsic confinement of the 2DEG. Together with the optimized T-gate structure, these features provide high linear gain at 30 GHz. Furthermore, the bi-layer passivation greatly suppresses the trapping effect (reduced by ~60%), contributing to high PAE >60%.

It is known that the intrinsic f_t, extrinsic source resistance (R_s), and gate resistance (R_g) dominate the NF_{min} of GaN HEMTs [17], [18]. In this work, the regrown ohmic contacts reduces the R_s, while the optimized gate design with a favorable gate head to gate foot ratio lowers the R_g [19]. Additionally, the well confinement of the 2DEG formed by the thin barrier, ultra-thin channel, and BB further reduces thermal and shot noise. These combined effects result in the excellent noise performance at 30 GHz for GaN-on-Si HEMTs.

Even with only moderate scaling (L_g= 100 nm), the combination of a well-confined, high-mobility, high-density channel and minimized parasitic resistance enables RF performance comparable to that of highly scaled devices. It is worth noting that the proposed technology demonstrates high efficiency and low noise simultaneously among both GaN-on-Si and GaN-on-SiC technologies (Fig. (6)).

V. Conclusion

This work demonstrates a GaN-on-Si MIS-HEMT technology on InAlN/GaN/AlGaN epitaxial structure for FR2 mobile T/R module applications. The characterized device achieves record high peak *PAE* >60% across the low-voltage range and state-of-the-art NF_{min} of 1.1 dB at 30 GHz simultaneously. These results suggest that moderate scaling could deliver competitive GaN-on-Si HEMT technology, when combined with optimized epitaxial structure and process. This work highlights the potential of GaN-on-Si HEMTs as a promising technology for future monolithically integrated FR2 mobile front-end applications.

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