Drop Impact Reliability Test and Failure Analysis for Large Size High Density FOWLP Package on Package

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Abstract—**Drop test reliability of the 20 *mm* × 20 *mm* RDL-first FOWLP on bottom and 8 mm × 8 *mm* WLCSP on top for Package on Package (PoP) test vehicle was validated by the experimental testing in this paper. The results show that the built up PoP test vehicle can pass 30 times of drop impact test and some samples can pass 200 times drop impact test with the loading of 1500 *G*/0.5 *ms*. The failure mechanisms of Cu pad peeling off, cracking of dielectrics and Cu trace on the bottom RDL-first FOWLP and crack on package corner solder joints of top WLCSP were identified by cross section observation. The peeling stress level on the solder joint and dielectrics layer were investigated by the dynamic explicit nonlinear drop impact simulation.**

Keywords-RDL-fist FOWLP, Package on Package (PoP), Drop Impact Test, Failure Analysis, FEA

I. INTRODUCTION

Multi-functions and miniaturization packaging with high reliability is the requirement of microelectronic packaging industry. Fan out wafer level package (FOWLP) with multi-chips embedded can provide one of the potential solutions. Different chips with functions of logic, memory and sensor can be integrated through multi-chips FOWLP technology [1, 2].

Currently, tow technique process flows were developed for the FOWLP. One method is mold-first FOWLP and the other method is redistribution layer first (RDL-first) FOWLP. For mold-first process flow, the chips will be molded firstly to reconstruct the mold wafer. After that the RDL is fabricated on the molder wafer. For RDL-first FOWLP method, the RDL will be fabricated on the supporting glass wafer firstly. And then the chips are mounted on the RDL layer using micro-bumps by flip chip bond. Molding process is done finally. The advantage of the RDL-first FOWLP process flow is that it can avoid the die shift issue during the molding process and reduce wafer level warpage during the fabrication process.

The drop impact reliability for the RDL-first FOWLP, especially for large package size, is the concern for mobile applications. With the highly acceleration loading conditions, crack and delamination failures may happen to the solder joints and dielectrics layers.

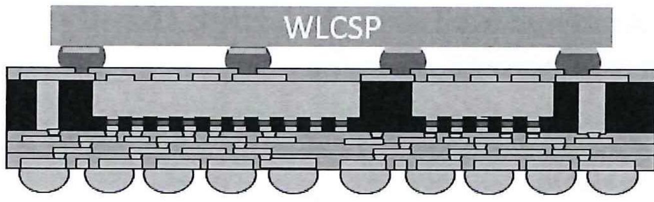
In this paper, the drop impact reliability of the package on package (PoP) test vehicle with the wafer level chip scale package (WLCSP) on top and the RDL-fist FOWLP on bottom was tested. The dimension of bottom RDL-first FOWLP package is 20 *mm* × 20 *mm* × 0.2 *mm*. The dimension of top WLCSP is 8 *mm* × 8 *mm* × 0.2 *mm*.

The drop impact reliability tests for the RDL-first FOWLP PoP were conducted with the loading of 1500 *G*/0.5 *ms* according to the JEDEC standard JESD22-B111. Daisy chains were designed on the critical interconnections in order to monitor the resistance during drop impact testing. The failure mechanisms were identified by cross section observation. The stress on the solder joints and RDL layer were investigated by the nonlinear dynamic explicit drop impact simulation.

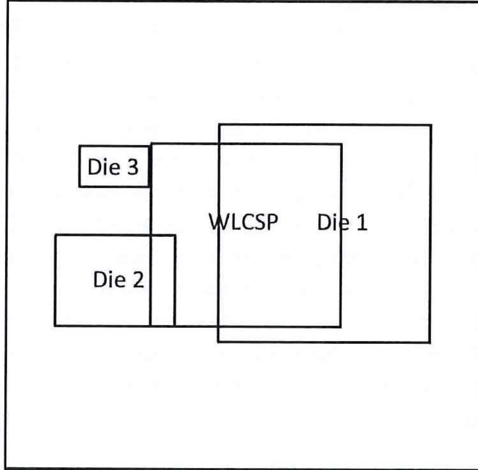
II. RDL-FIRST FOWLP POP TEST VEHICLE

The schematic of the developed RDL-first FOWLP PoP is shown in Figure 1. Three dies was embedded in the bottom RDL-first FOWLP which sizes are 9 *mm* × 8 *mm*, 5 *mm* × 4 *mm* and 3 *mm* × 2 *mm*, *respectively*, as shown in Table I. The locations of three embedded dies in the bottom package and WLCSP are shown as Figure 1 (b). The front side RDL of RDL-first FOWLP was fabricated on the supporting glass wafer firstly. Three different pitches 125 μm, 80 μm and 60 μm Cu pillar/solder micro-bump were used for the interconnections between the three chips and front side RDL of the bottom RDL-first FOWLP. The height of micro-bumps is 50 μm including Cu pillar and solder bump. 2 *mil* diameter vertical Cu wires embedded in the bottom package were used for the interconnections between the front side and back side RDLs. Compression molding process was used to fabricate the molded wafer after flip chip bonding. And back side grinding and polishing process was used to achieve 200 μm thickness of bottom package. The thicknesses of front side RDL and back side RDL are 24 μm and 12 μm, respectively. The I/O numbers of bottom RDL-first FOWLP package and top WLCSP are 2400 and 361, respectively. Solder balls (SAC305) with 400 μm pitch and 250 μm diameter were used for bottom and top packages.

The RDL-first FOWLP PoP test vehicle after fabrication is shown in Figure 2. Figure 2 (a) shows the bottom RDL-fist FOWLP after solder ball drop. Figure 2 (b) shows the top WLCSP package after solder ball drop. Figure 2 (c) shows the PoP test vehicle after stacking WLCSP on the RDL-first FOWLP and PCB with thermal compression bonding.

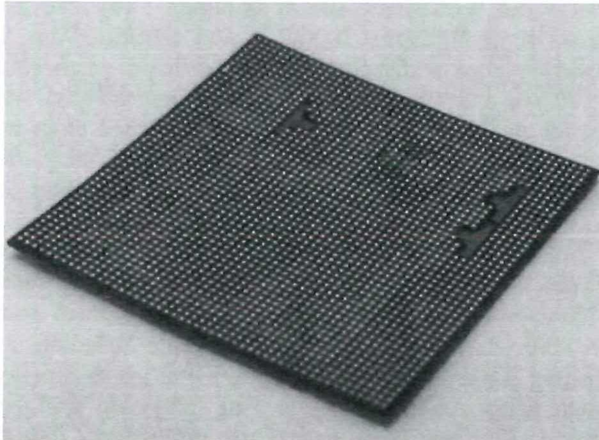


(a) Cross section view of RDL-first FOWLP PoP.

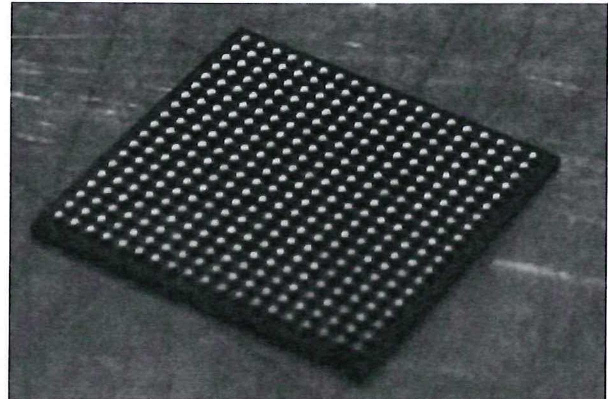


(b) Location of embedded dies in bottom RDL-first FOWLP and WLCSP.

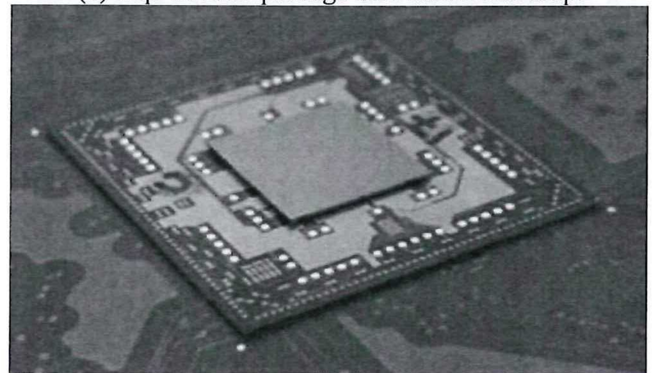
Figure 1. Schematic of RDL-first FOWLP PoP: (a) Cross section view of RDL-first FOWLP PoP; (b) Location of embedded dies in bottom DL-first FOWLP and WLCSP.



(a) Bottom RDL-fist FOWLP after solder ball drop.



(b) Top WLCSP package after solder ball drop.



(c) PoP test vehicle after stacking WLCSP on the RDL-first FOWLP and PCB with thermal compression bonding.

Figure 2. RDL-first FOWLP PoP test vehicle after fabrication: (a) Bottom RDL-fist FOWLP after solder ball drop; (b) Top WLCSP package after solder ball drop; (c) PoP test vehicle after stacking WLCSP on the RDL-first FOWLP and PCB with thermal compression bonding.

TABLE I. DIMENSIONS OF RDL-FIRST FOWLP POP.

	Dimensions (*mm*)
Bottom RDL-first FOWLP	20 *mm*×20 *mm*×0.4 *mm*
Top WLCSP	8 *mm*×8 *mm*×0.2 *mm*
Die 1 embedded in bottom RDL first FOWLP	8 *mm*×9 *mm*
Die 2 embedded in bottom RDL first FOWLP	4 *mm*×5 *mm*
Die 3 embedded in bottom RDL first FOWLP	2 *mm*×3 *mm*
Solder ball pitch	0.4 *mm*
Solder ball diameter	0.25 *mm*

III. Drop Impact Simulation and Analysis

Dynamic drop impact simulation was conducted to investigate the peeling stress level on critical solder joints and dielectrics layers. One quarter simulation model for RDL-first FOWLP PoP on the PCB was established, as shown in Figure 3. The RDL-first FOWLP PoP at the center location of PCB which is defined as U3 was considered. Global and local technique was used in order to simplify the simulation model. Detail structure with fine element meshes was only considered for the critical solder joints. Solder joints on the other location were considered with simplified block structure with coarse element meshes. 9×9 solder joints array at package corner of bottom RDL-first FOWLP and 3×3 solder joints array at package corner of top WLCSP was built up with local model as shown in Figure 3. The interaction constrains were applied between the global and local models.

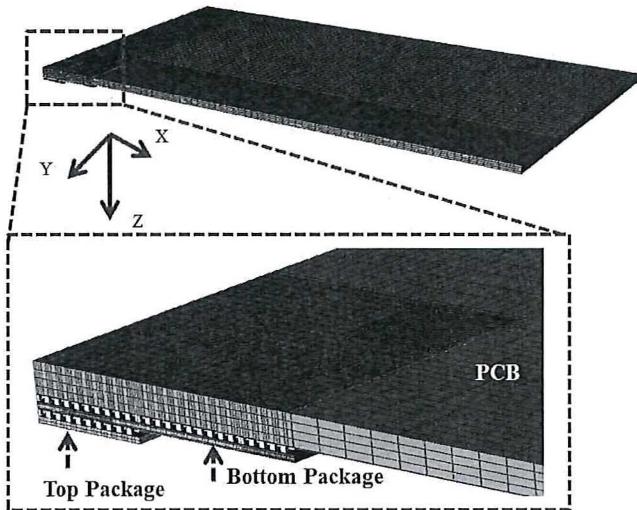


Figure 3. One quarter simulation model for the drop impact test of the RDL-first FOWLP PoP with global/local technique.

The input-G method was used to simulate dynamic response of drop impact test [2-8]. For the input-G simulation, the acceleration loading of 1500 *g*/0.5 *ms* was directly applied on the four bolt holes on corner of PCB. And the initial velocity in Z direction of -4.77 *m/s* was applied on whole model. Abaqus was used for the drop test simulation with dynamic explicit method. The element type is selected as C3D8.

Material properties for drop test simulation are listed in Table II. The anisotropic material properties were considered for PCB. The rate dependent stress-strain behavior of solder SAC 305 was considered [9]. Cu material was assumed to be with elastic-plastic behavior with yield strength of 120 *MPa*. The other materials were assumed to have the linear elastic properties.

TABLE II. Material properties used for dynamic drop test simulation.

Materials	Density Kg/m^3	Elastic Modulus (*GPa*)	Poisson's Ratio	Yield Stress (*MPa*)
Si	2329	131	0.28	-
Cu	8950	117	0.35	120
Dielectrics	2200	2.2	0.35	-
PCB	2200	25/x, y 11/z	0.11/x, y 0.39/z	-
Solder Mask	1300	2.4	0.32	-
SnAgCu(305)	7390	41.7	0.35	Rate dependent [9]
EMC	2000	18	0.35	-

Figure 4 indicates deformation of RDL-first FOWLP PoP at PCB center under the drop impact loading. From the side view of the deformation, it can be predicted that the critical solder will be located on the package corner of bottom RDL-first FOWLP and the package corner of the top WLCSP due to the bending effects.

The peeling stress σ_{33} of 9×9 solder joints array at package corner of bottom RDL-first FOWLP under drop impact loading is shown in Figure 5. Due to the bending effects, the solder joint at package corner suffered higher peeling stress. The maximum peeling stress σ_{33} on the package corner solder joint of the bottom RDL-first FOWLP is 229 *MPa*. The peeling stress at PCB side is higher than the package side.

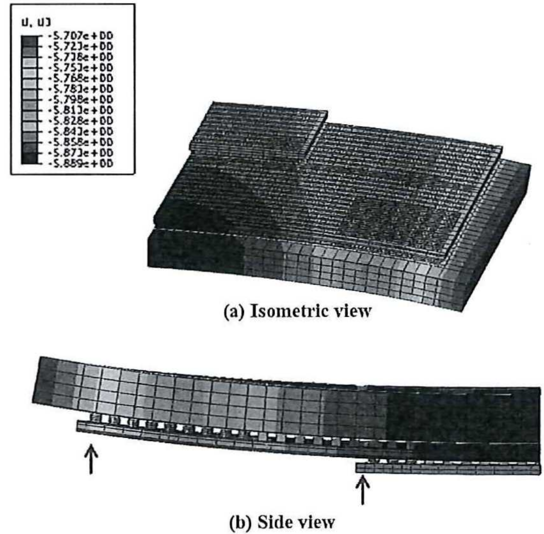


Figure 4. Deformation of at RDL-first FOWLP PoP on the U3 location of PCB due to bending effects.

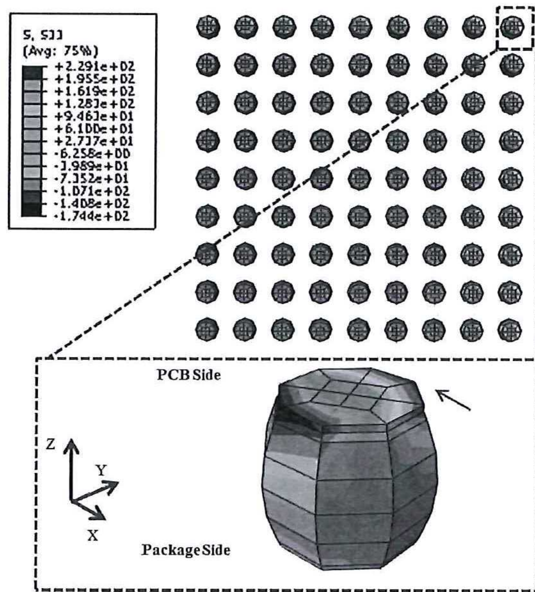


Figure 5. Peeling stress σ_{33} of 9×9 solder joints array at package corner of bottom RDL-first FOWLP.

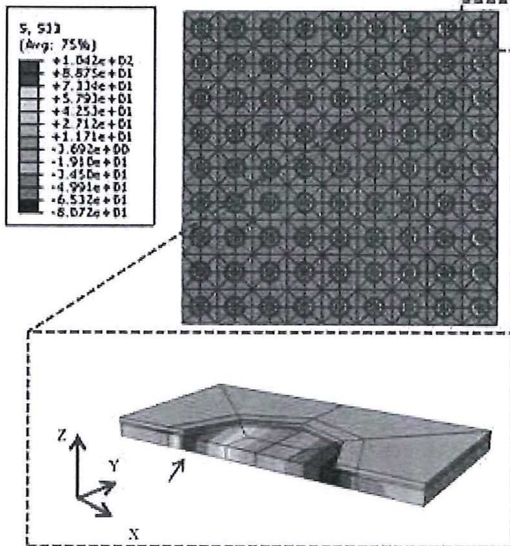


Figure 6. Peeling stress σ_{33} on the dielectrics at package corner of bottom RDL-first FOWLP.

Figure 6 shows peeling stress σ_{33} on the dielectrics at package corner of bottom RDL-first FOWLP under drop impact loading. The peeling stress σ_{33} about 104 *MPa* was induced to the dielectrics under the Cu pad on the location of package corner.

Figure 7 shows the peeling stress σ33 of 3×3 solder joints array at package corner of top WLCSP under drop impact loading. Due to the bending effects of bottom package and PCB as shown in Figure 4, the solder joint at package edge of WLCSP suffered the higher peeling stress. The maximum peeling stress σ_{33} on the package edge solder joint is about 253 *MPa*. The critical location on the solder joint is RDL side.

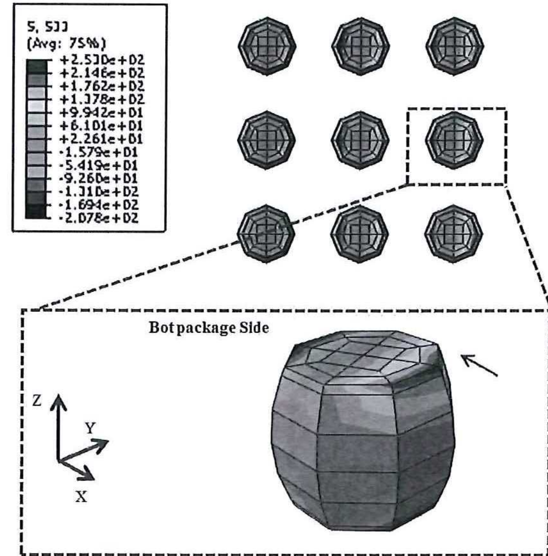


Figure 7. Peeling stress σ_{33} of 3×3 solder joints array at package corner of top WLCSP.

IV. Drop Impact Test and Failure Analysis

The RDL-first FOWLP PoP mounted on the PCB is shown in Figure 8. The size of drop impact test board is same as JESD22-B111, which is 131 *mm*×77 *mm*×1 *mm*. Only five RDL-first FOWLP PoP packages can be mounted on the PCB due to the large size of 20 *mm*×20 *mm*. Locations of the packages on the PCB are defined as U1, U2, U3, U4 and U5 as shown in Figure 8. No underfill was used for the RDL-first FOWLP PoP.

The PCB was installed on the table of drop impact tester with four support bolts. When doing the drop impact tests, the loading of a half sine shock pulse of 1500 *g*/0.5 *ms* was applied. During the drop impact testing, the resistance of the critical daisy chains was monitored.

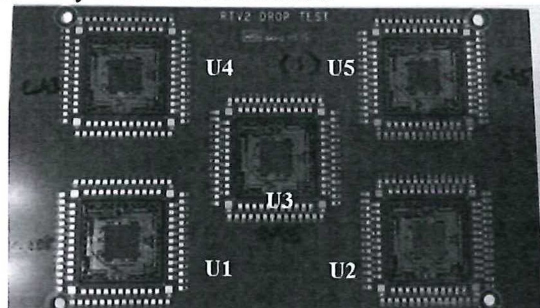


Figure 8. RDL-first FOWLP PoP mounted on the PCB with thermal compression bonding.

Table III shows the drop impact testing results of RDL-first FOWLP PoP on three PCB for 200 drops test. The testing results shows that the sample can pass 30 drops test

which was required by the standard for mobile applications. Some package can pass 200 times of drop test. Through the drop impact test, the drop test reliability of RDL-first FOWLP PoP test vehicel was validated.

TABLE III. DROP TEST RESULTS OF RDL-FIRST FOWLP POP FOR 200 DROPS.

Location	Sample 1	Sample 2	Sample 3
U1	200 drops 1st fail	pass	170 drops 1st fail
U2	200 drops 1st fail	200 drops 1st fail	pass
U3	50 drops 1st fail	pass	50 drops 1st fail
U4	110 drops 1st fail	50 drops 1st fail	pass
U5	170 drops 1st fail	pass	pass

Some early failures were found to RDL-first FOWLP PoP under drop impact loading. Cross section was done by mechanical grinding and polishing to show the mechanisms of the failed daisy chains as shown in Figures 8, 9 and 10.

The cross section along the package corner of bottom RDL-first FOWLP was done by the mechanical grinding and polishing. The SEM picture of the failed critical solder joints at the package corner of bottom RDL-first FOWLP is shown in Figure 8. It is can be found that delamination happened to the interface between Cu pad and dielectrics layer. The Cu pad and trace was peeled off. Crack happened to Cu traces. The delamination at the interface between Cu pad and dielectrics was caused by the peeling stress under drop impact loading and poor adhesion. From the picture, it can be seen that the vertical Cu wire structure is good under drop impact loading.

The cross section along the package edge of bottom RDL-first FOWLP was done by the mechanical grinding and polishing. The SEM picture of the failed critical solder joints is shown in Figure 9. It is can be observed that Cu pad was peeled off from the dielectrics layer. Crack happened to dielectrics layer at edge of Cu pad. Large deformation happened to the Cu pad. The delamination at the interface between Cu pad and dielectrics was caused by the peeling stress under drop impact loading, as shown in Figure 6.

The adhesion of the Cu pad to dielectrics layer need to be enhanced to withstand the peeling stress under drop impact loading. The delamination may happen to the interface between Cu pad and dielectrics and also the interface between dielectrics and EMC causing the critical issues to the drop impact reliability of FOWLP.

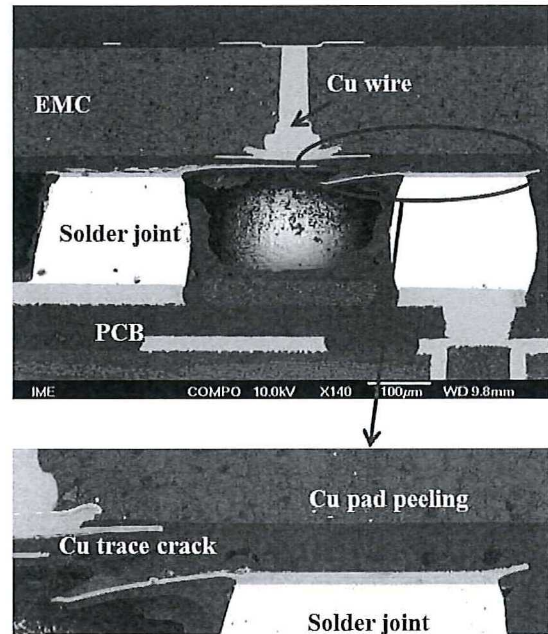


Figure 9. Failure mechanisms of the crictical solder joint at the package corner of bottom RDL-first FOWLP with details of Cu pad peeling and Cu trace crack failures.

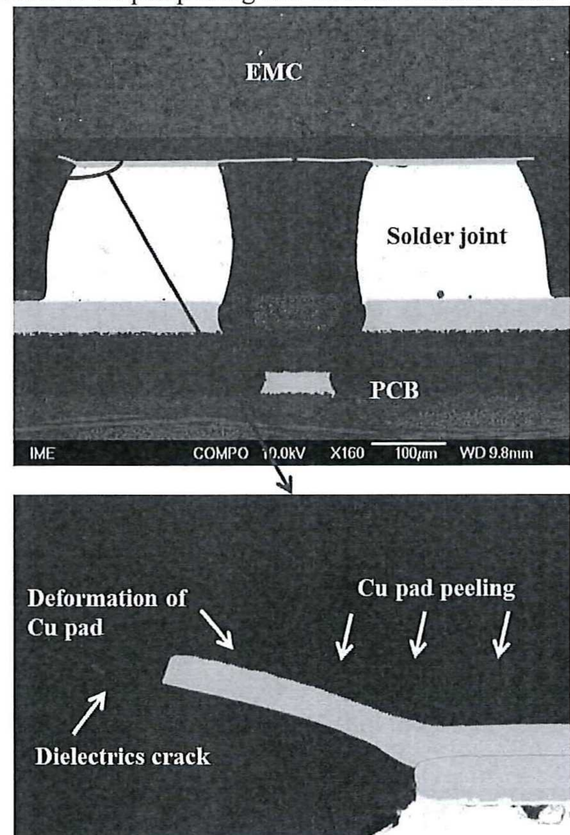


Figure 10. Failure mechanisms of the solder joint at the package edge of bottom RDL-first FOWLP with details of Cu pad peeling and dielectrics crack failures.

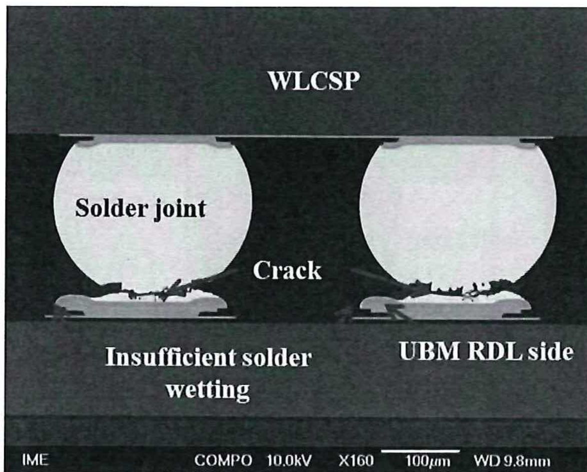


Figure 11. Failure mechanisms of the package edge solder joint of top WLCSP with details of crack on solder joint at RDL side.

Figure 11 shows failure mechanisms of the solder joint at the package edge of top WLCSP. It can be found that with crack happened on solder joint at back RDL side under the drop impact loading. It can be also seen that the insuffient solder weting hanppend to the solder to the UBM at back RDL side. The crack can happpen to the solder joint more easily with the insuffcent wetting under the highly peeling stress as shown in Figure 7.

V. CONCLUSIONS

In this paper, drop impact test reliability of the 20 *mm* × 20 *mm* RDL-first FOWLP on bottom and 8 mm × 8 *mm* WLCSP on top for PoP test vehicle was validated by the experimental test. The failure mechanisms were identified by cross section observation. Some important conclusions are summarized as following:

(1) Drop impact reliability of large size (20 *mm* × 20 *mm*) RDL-first FOWLP PoP test vehicle was validated by 1500 *G*/0.5 *ms* drop impact testing. The samples can pass 30 times of drop test and some package can pass 200 times of drop test.

(2) The failure mechanisms of the early failed samples were identified to be Cu pad peeling off, cracking of dielectrics and Cu trace on the bottom RDL-first FOWLP and crack on the package edge solder joint of top WLCSP.

(3) The delamination on the interface between Cu pad and dielectrics were caused by the peeling stress due to bending effects of drop testing board. The adhesion of the Cu pad to dielectrics layer need to be enhanced.

(4) Highly peeling stress was induced to the solder joint of top WLCSP due to the bending effects which caused the solder joint cracking.

ACKNOWLEDGMENT

This work is the result of a project initiated by High Density Fan-Out Wafer Level Packaging (HD-FOWLP) Consortium. The authors greatly appreciate the members' participation in discussions and encouragement throughout the course of the project which makes this research possible.

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