1V, 1.13μm pixel pitch Liquid Crystal Driver with Charge-Balancing Scheme for SLM Applications

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***Abstract*——This work proposes a compact 9T SRAM-based pixel design for low-voltage and high-speed modulator for spatially varying modulation of light (i.e. SLM). To reduce the supply voltage to the CMOS pixel backplane, the operating point is shifted towards the linear window by dynamically pulsing both the top & bottom electrodes in each pixel. A test chip in a standard 40nm CMOS technology was implemented, supporting upto 90 frames/second VGA display. Our testing results demonstrated that the proposed HCS switching scheme is efficient in achieving optical modulation up to 8-bit resolution, making it a viable candidate for state of the art SLMs applications with high frame rate and low power requirements.**

***Index Terms*—Spatial Light Modulators, Liquid Crystal Displays, Low voltage displays, Digital driving scheme, VGA.**

I. Introduction

Liquid Crystal on Silicon Spatial Light Modulators (LCoS-SLM) are advanced technology used to modulate amplitude, phase or polarization of light waves [1]. Thanks to their high frame rate & flexibility in generating arbitrary light pattern [1], LCoS-SLM are found in many advanced optics/photonics applications such as holographic, augmented reality (AR) and virtual reality (VR) (Fig. 1(a) [2], [3]. Essentially, an LCoS-SLM has three main components: a CMOS backplane, a liquid crystal (LC) layer & an ITO-coated cover glass, as illustrated in Fig. 1(b). The CMOS backplane is an integrated chip that allows high speed and accurate phase and intensity control of the light that pass through each LC pixel. In 2D SLM arrays, the bottom electrodes are individually addressed by the CMOS chip to provide the pixel voltage, V_P, whereas the top ITO voltage, V_{ITO} is shared as a common biasing [1]. The LC molecules' orientation is determined by the voltage applied across each pixel $|V_{LC}| = |V_{ITO} - V_P|$, as shown in Fig. 1(c).

Although CMOS technology offers excellent control speed and scalability, there are challenges in implementing the pixel driving circuits in CMOS technology, especially in advanced nodes. First, standard CMOS devices usually operate at low voltage (e.g. 1V in 40nm) while the LC requires high voltage to switch its orientation (3V to 5V, as shown in Fig. 2(a)). Second, conventional analog driving scheme is facing limited scalability and gray-scale resolution while consuming large

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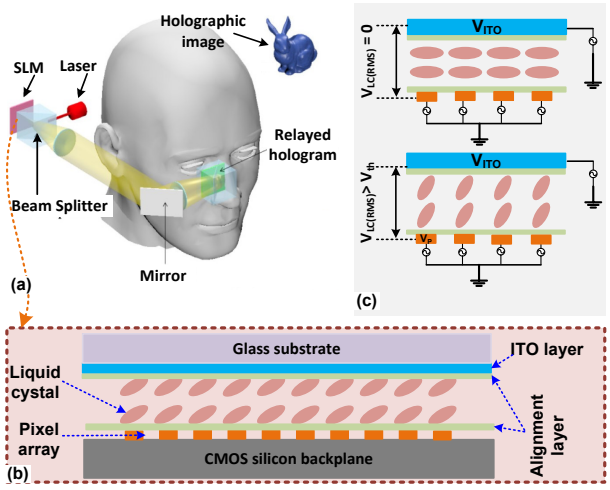

Fig. 1: (a) LCOS-SLM technogloy & applications in near-eye hologram [4], (b) Structure of typical LCoS cell, (c) Typical switching operation

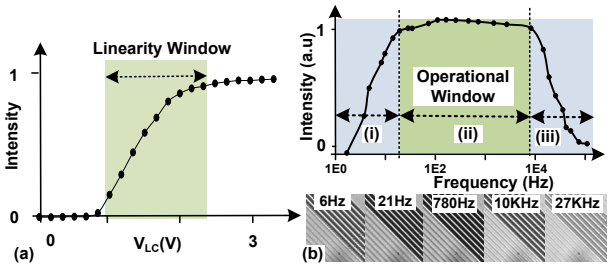

Fig. 2: (a) Typical voltage response curve of a reflective SLM, (b) LC Response vs different V_{ITO} modulation frequency

silicon area and power due to the column-based driving circuits [1]. Third, although thick gate CMOS devices can be use to elevate to voltage headroom of the pixel, it results in high power consumption [5], [6]. Thick gate devices also lead to large pixel pitch [5], [6] that limits the viewing angle of the true 3D holographic display [1]. Finally, the control chip also needs to provide field inversion at proper interval to ensure charge balancing across the LC to avoid both ion-migration (low frequency, region (I) in Fig.2b), and slow LC response time (high frequency, region (III) in Fig.2b) region of operation, failing which will result in poor modulation of light [1]. As presented in Fig. 2(b), our measurement data on an in-house LC device confirmed that reflected light intensity indeed attenuated when the ITO switching frequency is either

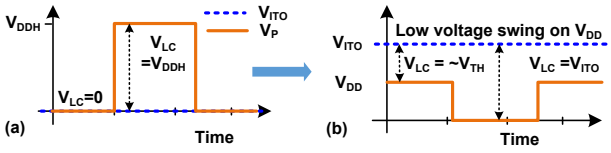

Fig. 3: (a) Conventional driving scheme, (b) Proposed driving scheme

too fast (i.e. above 10 KHz) or too slow (i.e. below 50 Hz). Thus we must keep the field inversion switching frequency within a certain range, depending on the characteristic of the LC.

In this work, to mitigate the need for large LC voltage swing, we propose a Hybrid Control Scheme (HCS) to shift the LC operating point to a narrower but linear range, enabling a compact pixel and low-voltage control scheme using purely thin oxide devices with only 1V supply. Coupling with a digital pulse-code modulation (PCM) scheme [1], this is the first work to demonstrate the feasibility to realize high frame rate, 8-bit SLM gray scale with high linearity response using 1V backplane control.

II. PROPOSED LOW VOLTAGE & DRIVING SCHEME AND PIXEL DESIGN

A. Low voltage driving scheme

Fig. 2(a) shows a typical intensity response of a LC pixel against the voltage across its bottom and the top electrodes, V_{LC}. It can be seen that the LC requires a substantial voltage (i.e. $V_{LC} > 3V$) to exhibit the full intensity response. As a result, in the conventional design, a high voltage swing is applied across the LC with V_P swinging between 0V and V_{DDH} (e.g. 3.3V) while V_{ITO} is kept at 0V, as shown Fig. 3(a). 3.3V being the typical IO voltage in a standard CMOS chip.

Although the LC requires $> 3V$ to switch completely, we noticed that majority of response happens within a narrow and linear window (1V to 2.4V). Thus, in our proposed HCS we shift the V_{ITO} to an intermediate voltage, while V_P is only switched between 0V and V_{DD} (e.g. 1V), as illustrated in Fig. 3b. In this scheme, V_{ITO} is chosen so that when $V_P = V_{DD}$, V_{LC} (i.e. $V_{ITO} - V_{DD}$) is at minimum and close to V_{TH} (switching threshold of LC). When $V_P = 0V$, V_{LC} is at maximum and equal to V_{ITO}. By doing so, we set the LC to the operating point where light intensity is the most responsive to the V_{LC} changes (i.e. the green shaded area in Fig. 2(a) and thus requires the least possible pixel voltage swing for the required intensity. To maintain DC balancing, both the top and bottom electrode are inverted at the given interval, while maintaining the same average $|V_{LC}|$ across the frame. This can be digitally done by repeating the sub-frame with inverted pixel data (i.e. $0 \leftrightarrow 1$) while changing the ITO voltage from V_{ITO} to $-(V_{ITO} - V_{DD})$. We have comprehensively verified this scheme on our in-house LC to ensure endurance and long-term operation of the display.

B. 9T cell for near-$1\mu m^2$ pixel

Our LC is digitally driven by an array of SRAM based cells using PCM scheme. Schematic of the proposed cell is shown

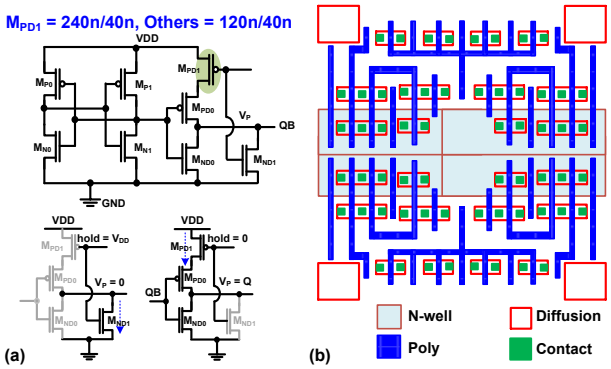

Fig. 4: (a) Schematic of the proposed 9T cell with the power transistor M_{PD1} shared among 4 adjacent cells, (b) 4-cell layout with shared M_{PD1} & well taps added at 4-cell cluster level to ensure layout uniformity

in Fig. 4a consisting of a 6T-SRAM structure for storing the pixel value and four additional transistors $M_{PD0/1}, M_{ND0/1}$ for driving the bottom electrode of the LC (i.e. V_P) (access transistors are not shown for clarity). During data loading, SRAM cell is written similar to conventional memory. "Hold" signal is pulled to V_{DD} to drive V_P to GND via M_{ND0}. After loading, "Hold" signal is pulled low to turn on (off) $M_{PD0}(M_{ND0})$. Thus, $V_P \rightarrow V_{DD}(GND)$ if $Q_B = \backslash 1"(\backslash 0")$ to modulate the LC. As the "Hold" signal is common to the whole array, M_{PD1} can be shared among multiple cells (4 in this work, as shown in the layout of 4-cell group in Fig. 4(b)) to save area. This cell layout also includes well taps to maintain the homogeneity of display array. By using logical layout rules, we achieved 80% electrode fill factor, $900F^2/cell$, which is 33% more compact than [6].

Due to constrained pixel size and pitch, we opted to use minimum size transistors of the process for the SRAM design, in order to ensure the stability of the unit cell is simulated for pessimistic noise margin(i.e. Static Noise Margin(SNM)). We ran Monte-Carlo simulation for 1000 sampling points. As shown in Fig. 5a and Fig. 5b the SRAM unit cell has large enough write margin (WSNM) of $350mV$ to ensure no write error at 1V supply. As the read operation is of least significant in display operation and only used for debugging purposes the low read static noise margin (RSNM) of $20mV$ can be safely nullified. The final cell layout occupies in effective area of 1.2 $\mu m \times$ 1.13 μm. It can be projected that with a simple scaling, it is possible to realize a more compact cell (i.e. $\leq 1\mu m$ pitch) and thus higher display density and 3D display angle if using the proposed cell structure and riding on the technology scaling with advanced CMOS node (e.g. 28 nm and below).

C. Array implementation

Schematic of the proposed design is shown in Fig. 6, supporting VGA display of 480 rows × 640 columns. Conventional memory structure is used to access the bottom electrodes in order to support 100MHz for 8-bit gray scale at 90fps with 32 bit I/O. 20-to-1 column multiplexing along the column direction is deployed to reduce number of IO pads. Pixel cells are addressed sequentially by using an internal

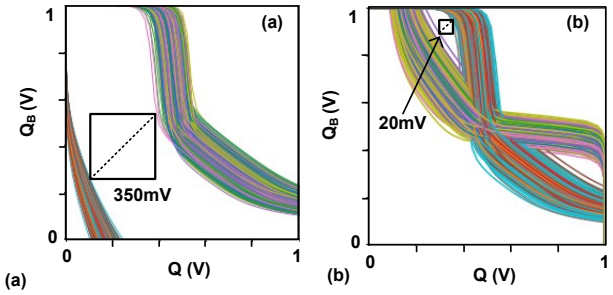

Fig. 5: Monte-Carlo simulation of the proposed SRAM-based pixel data storage (a) Write static noise margin (WSNM) (b) Read static noise margin (RSNM)

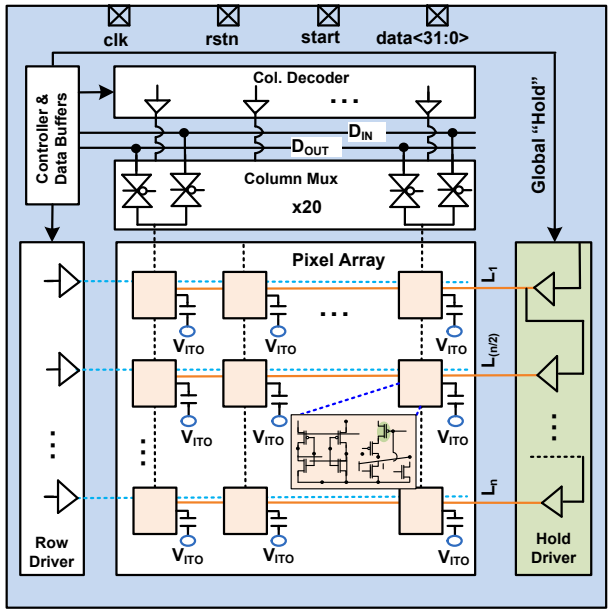

Fig. 6: Array implementation of the proposed design with conventional row/column drivers and a daisy-chain hold driver to mitigate its peak current at the rising and falling edge of the display mode enable

address generator with 9600 clock cycles for each write or read operation to cut down address IO pins. The global "Hold" signal is triggered and kept high immediately right after the data loading, thus transferring the content of the whole memory array to the corresponding bottom electrodes of the LC panel. Since the "Hold" signal drives all the pixels at the same instance, it draws a huge peak current of 300mA from V_{DD} at the beginning of each display cycle. To mitigate this, we daisy-chained the "Hold" buffer along the row direction, spreading the hold triggering over a period of 50ns, successfully reducing the peak current by 98% (Fig. 7(a)). Note that the total display time is in tens of microseconds thus the difference of 50ns between the first and the last row is insignificant in terms of light response. During continuous operation (i.e. loading data and display), the proposed design reduces about 90% of power consumption compared to prior art with high voltage pixels, thanks to the usage of core devices across the whole array which removes the need for level-shifter and high voltage row/column drivers (Fig. 7(b)).

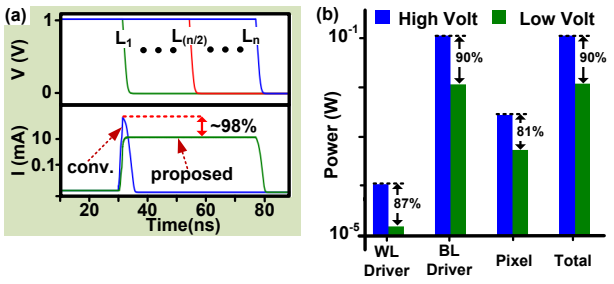

Fig. 7: Simulation results of the proposed design (a) 98% peak current reduction thanks to the daisy-chain hold buffers (b) Overall 90% total power saving between high voltage and proposed Low voltage cell

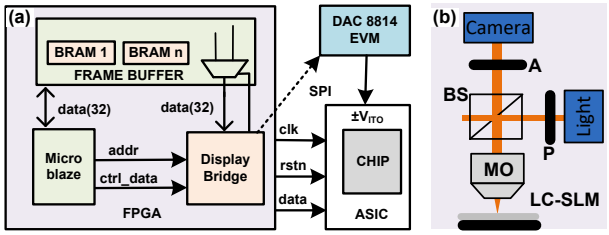

Fig. 8: Test setup using FPGA-based control (a) Block diagram of functional control including a MicroBlaze controller, a customized bridge to interface with the chip & BRAMs for frame buffer (b) Optical set-up in reflective mode

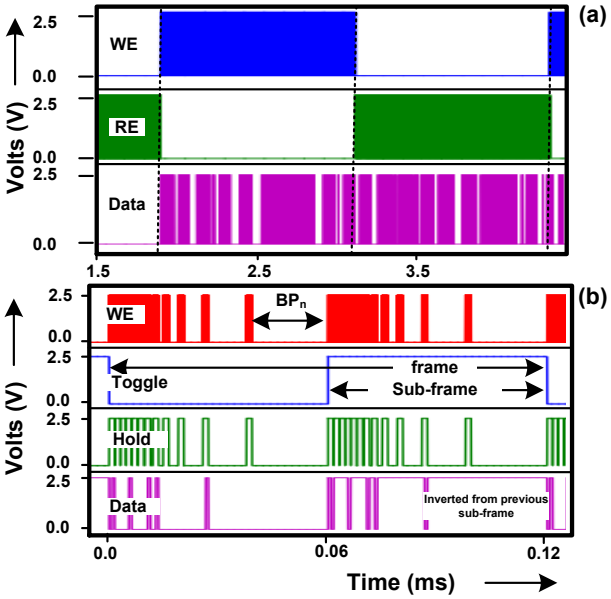

Fig. 9: Electrical function verification in (a) SRAM content read-out mode, (b) Continuous display mode

III. TEST CHIP MEASUREMENT RESULTS

A prototype of our SLM driver has been fabricated in 40nm CMOS technology, occupying a total die area of 16 mm^2 with core circuits requires only 0.48 mm^2. A FPGA-based test system was deployed with on-FPGA data frame buffers & off-the-shelf DAC for V_{ITO} biasing (Fig. 8a). For optical measurements the sample is placed under a crossed polarizer-analyzer configuration with the FPGA driving the input data patterns. A camera captures the response of the LC panel for real-time display, calibration & data post possessing (Fig. 8b). Fig. 9(a) and Fig. 9(b) show the measured waveform of the chip in SRAM read/write & display modes respectively.

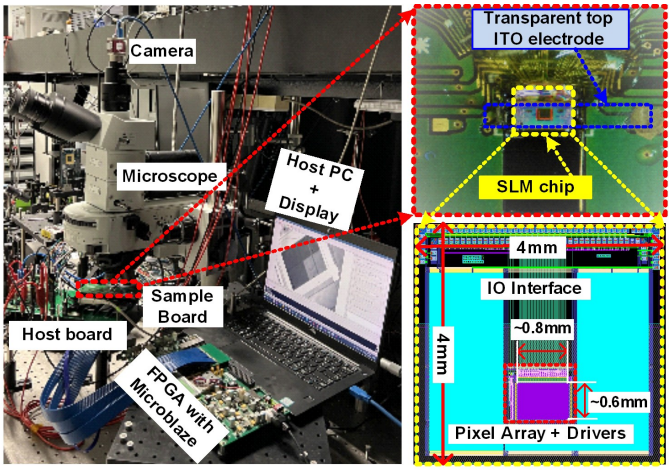

Fig. 10: Setup with host PC, microscope, FPGA & camera (Light source/DC supply are not visible), (**Insert 1**: top, right) Sample PCB with LC, ITO & glob top encapsulation, (**Insert 2**: bottom, right) Layout of the chip. The pixel array only occupies 0.8mm × 0.6mm (i.e. the purple rectangle) while majority of the chip is filled will dummy metal due to the required distance between the pixel array to the chip edge for post-processing purposes

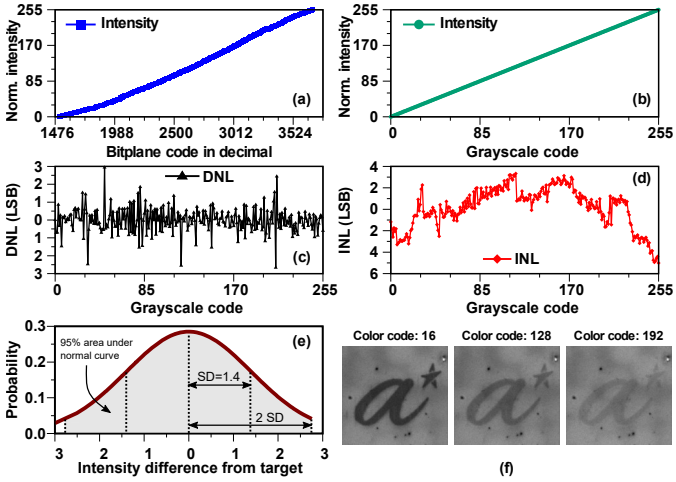

Fig. 11: (a)-(b) 8-bit gray code to intensity response using square & LUT based approach resp., (c)-(d) DNL & INL of intensity gray code mapping, (e) Measured temporal intensity variations of pixel patch, (f) Displaying logo image on chip

During the read mode, we were able to achieve 0% bit error rate (BER) at 50MHz, 1V. In the display mode, toggling of pixel data and DAC voltage between sub-frame is used to realize the digital DC balancing as explained earlier in II-A. The detailed test setup used in optical measurement is shown in Fig. 10 along with the PCB and chip layout. Fig. 11(a) shows the raw LC's intensity response when the 12-bit pulse-code values were swept from 1024 to 4096. The data below 1024 are not shown as the total display duration is too short to create any differentiation in light intensity. It is apparent that digital code (& thus the total pulse width) to intensity response is not linear due to the (1) response time of the LC (2) fixed data loading time for each bitplane, which contributes as a DC offset & (3) root-mean-square relationship between effective pulse width & intensity. To calibrate this, a look-up table (LUT) based on the measured data in Fig. 11(a)

TABLE I: Comparison of the proposed design against the state-of-the-art

	JDT'12 [5]	TCAS I'20 [6]	IEDM'21 [7]	This work
Tech. Node	180nm	130nm	VST	40nm
LC voltage (V)	4	3.3	10	1V
Pixel topology	6T	8T	-	9T
LC driving	Digital	Digital	Digital	HCS
Resolution	8-bit	8-bit	8-bit	8-bit
DNL/INL	3.8/24.33	-	-	3/6
No.of Bitplane	34	-	-	12
Pixel pitch* (μm)	2.5x2.5	1.6x1.6	-	1.13x1.13
Freq. (MHz)	75	100	-	100
Voltage (V)	1.8/3.3	1.5/3.3	-	1
Frame rate (Hz)	360	360	24	90

∗ Normalized with technology node.

was developed to map the closest pulse-code value to each desirable intensity response, as validated in Fig. 11(b). Using this LUT, the SLM driver's response was measured again to verify the mapping & linearity. Fig. 11(c) and Fig. 11(d) show the measured differential non-linearity (DNL) and integral non-linearity (INL) of the chip. The chip achieved about 3 LSB DNL & 6 LSB INL which is 21% and 75% better than earlier reported values, respectively [5]. Fig. 11(e) shows a typical temporal variation of the design for 100 measurement cycles. The LC deviates from the expected intensity by only 2.8 LSB for 95% of the time, which includes quantization noise from the camera. This confirms that the LC responds accurately to the proposed switching scheme, as illustrated in example images in Fig. 11(f).

Table I compares our work with the state-of-the-arts. Our design offers the lowest voltage operation while maintaining a competitive INL/DNL with the smallest pixel using low-cost standard CMOS technology.

IV. Conclusion

We have demonstrated a low-voltage, low-power control scheme to for multi-bit gray-scale SLM display. Comprehensive test results on commercial 40nm CMOS process prototype chip with in-house LC device demonstrates 8-bit linearity with core supply voltage of 1V. This leads to 90% power reduction compared to conventional driving high voltage pixel and switching schemes with un-compromised display quality.

References

[1] G. Lazarev *et al.*, "Beyond the display: phase-only liquid crystal on silicon devices and their applications in photonics [invited]," *Opt. Express*, vol. 27, pp. 16206–16249, May 2019.

[2] J. H. Choi *et al.*, "The new route for realization of 1-μm-pixel-pitch high-resolution displays," *Journal of the Society for Information Display*, vol. 27, no. 8, 2019.

[3] H.-M. P. Chen *et al.*, "Pursuing high quality phase-only liquid crystal on silicon (LCoS) devices," *Applied Sciences*, vol. 8, no. 11, 2018.

[4] J.-S. Chen *et al.*, "Improved layer-based method for rapid hologram generation and real-time interactive holographic display applications," *Opt. Express*, vol. 23, pp. 18143–18155, Jul 2015.

[5] J.-S. Kang *et al.*, "Digital driving method for low frame frequency and 256 gray scales in liquid crystal on silicon panels," *Journal of Display Technology*, vol. 8, no. 12, pp. 723–729, 2012.

[6] J.-K. Cho *et al.*, "A low-voltage-driven high-voltage SRAM pixel circuit for power reduction in a digital micro-display panel," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 5, pp. 1640–1652, 2020.

[7] J. H. Choi *et al.*, "World-first 1 μm-pixelated 72k large area active matrix spatial light modulator on glass for digital holographic display," in *2021 IEEE International Electron Devices Meeting*, pp. 9.3.1–9.3.4, 2021.