Two-Phase Liquid Cooling for High-Power Microelectronics via Embedded Micro-Pin Fin Heat Sink

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***Abstract*—Two-phase liquid cooling can achieve significantly high heat flux and is therefore a key method for heat dissipation of high-power microelectronics. In this study, we develop an embedded two-phase liquid cooling solution with micro-pin fins embedded in a thermal test vehicle. We conduct experimental tests under various coolant (deionized water) flowrates and heat fluxes. Heat fluxes up to 181 W/cm^2 (heat power 181 W) are achieved at small coolant flowrates. Chip temperature and pressure in the two-phase regime are fluctuated. By degassing the coolant prior to experimental testing, the chip temperature fluctuation span can be reduced to as low as 7.6°C. The pressure fluctuation is also greatly reduced. These results are beneficial for the practical application of two-phase liquid cooling in microelectronics, where chip temperature fluctuations may damage chips due to temporary overheating. In addition, the temperature and temperature gradient of chip linearly increase with increasing heat flux. They both can be reduced by increasing coolant flowrate. As coolant flowrate increases, the heat flux at which two-phase cooling occurs also increases. The present results demonstrate the effectiveness of embedded two-phase liquid cooling, which can facilitate our next step to develop embedded two-phase liquid cooling for true 3D ICs (i.e., two-layer stacked chips).**

***Index Terms*—Embedded micro-pin fins, high-power microelectronics, two-phase liquid cooling.**

I. Introduction

MOORE'S Law of ICs comes towards an end due to the limitations in physics, material, and electronics. However, thanks to the advanced packaging technology, microelectronics continues developing towards higher integrations [1]–[5]. More powerful and further miniaturized microelectronic devices are fabricated to fulfill the demands of industries, including power plants, electric vehicles, avionics, supercomputers, and data centers [6]–[11]. Along with the higher integration, the power density of microelectronics has also been greatly increased. Heat dissipation becomes a bottleneck to the development of high-performance microelectronics via advanced packaging techniques [12]–[16]. Conventional air cooling fails to dissipate high heat fluxes. Hence, new high-efficient cooling techniques are demanded.

Researchers developed various liquid cooling methods towards the practical applications in different fields, such as data center [17]–[19], power module [20]–[23], lithium-ion battery [24], RF device [25], and high bandwidth memory [26]. Among these methods, two-phase liquid cooling is attracting increasing attention as it can handle higher heat fluxes by utilizing latent heat of coolant [27], [28]. Researchers developed various types of two-phase liquid cooling techniques for high-power microelectronics, ranging from immersion cooling [29], [30], spray cooling [31]–[33], microchannel cooler [34]–[37], jet impingement [38]–[40], to micro-pin fin cooler [41]–[43]. Much higher heat fluxes have been achieved compared to single-phase liquid cooling. However, the complex nature of two-phase liquid boiling is prone to violent fluctuations in chip temperature and system pressure. The fluctuations can lead to unstable cooling and possibly damage the chip due to temporary overheating.

Many studies have been conducted to achieve a stable two-phase liquid cooling [44]. Micro-pin fin cooler is effective to reduce the fluctuations in two-phase liquid cooling [34], [41]–[43]. In addition, compared with other methods, it also has the advantages of small flow resistance and easy integration. Therefore, we adopted micro-pin fins to develop embedded two-phase liquid cooling for high-power 3D ICs. As the first step, we designed and developed a single-layer thermal test vehicle (TTV) with an embedded micro-pin fin heat sink (MPFHS). The TTV was tested under various conditions. High heat fluxes and stable chip temperatures were achieved at low coolant flowrates. The present results can facilitate our next step of research on embedded two-phase liquid cooling of true 3D ICs, i.e., two-layer stacked chips.

II. Experimental Methodology

A. Thermal Test Vehicle

The TTV is composed of a silicon cap, a silicon chip, and a PCB. The silicon chip and cap are of footprint 1 cm

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$\times$ 1 cm, and thickness 300 μm. The silicon chip contains a titanium thin-film heater and two resistance temperature detectors (RTDs) on the active side, with micro-pin fins embedded on the back side. The back side was bonded to the silicon cap using our in-house high-temperature non-conductive epoxy adhesive, forming the embedded MPFHS. Unlike the conventional embedded MPFHSs, whose coolant inlet and outlet are designed in the top wall as shown in Fig. 1(a), the present MPFHS was designed with coolant inlet and outlet in the sidewalls as shown in Fig. 1(b). The silicon consumption is greatly reduced due to the removal of coolant feeding and collection parts in present MPFHS. The heater and RTDs, deposited to mimic high-power electronics and monitor the chip temperature, occupy the main area of active surface. The MPFHS was bonded to the PCB via solder balls for electrical connections.

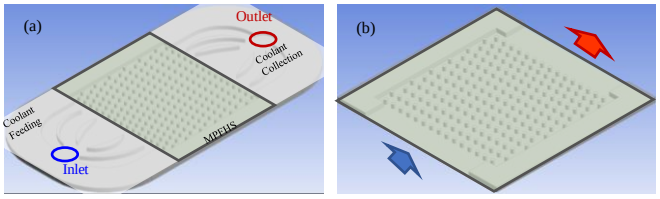

Fig. 1. (a) Conventional design and (b) present design of MPFHSs.

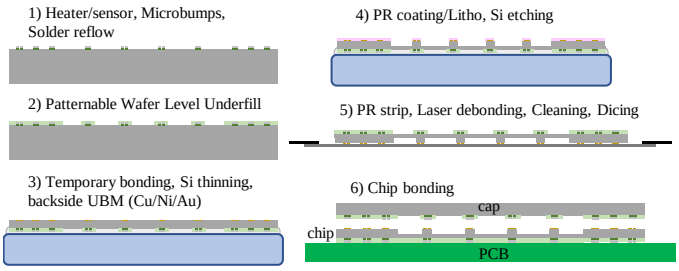

Fig. 2. Process flow of the TTV.

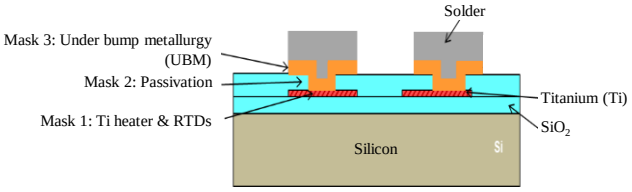

Fig. 3. Three mask layers for the TTV.

A fabrication process using three masks was designed to fabricate the TTV as shown in Figs. 2 and 3. The heater and RTDs were designed as meandering lines of width and spacing 200 μm and 20 μm, respectively, and deposited on the active side of silicon chip. The heater area covers more than 80% of the whole TTV area (Fig. 4). Two RTDs are located at two corners for chip temperature monitoring.

We measured the widths of heater and RTDs of fabricated wafer, which are 199.89 ± 0.76 μm and 19.82 ± 0.55 μm, respectively, as shown in Fig. 5. The differences between different chips are small, showing good consistency across samples.

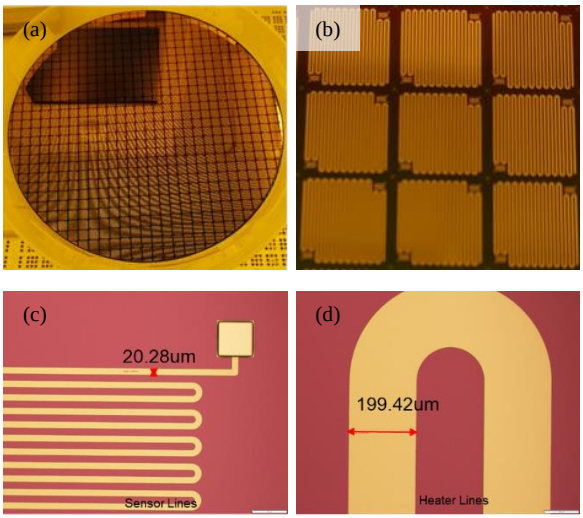

Fig. 4. Photos of titanium (Ti) layer deposition. (a) The whole wafer, (b) the enlarged view of nine chips, (c) the RTD, and (d) the heater.

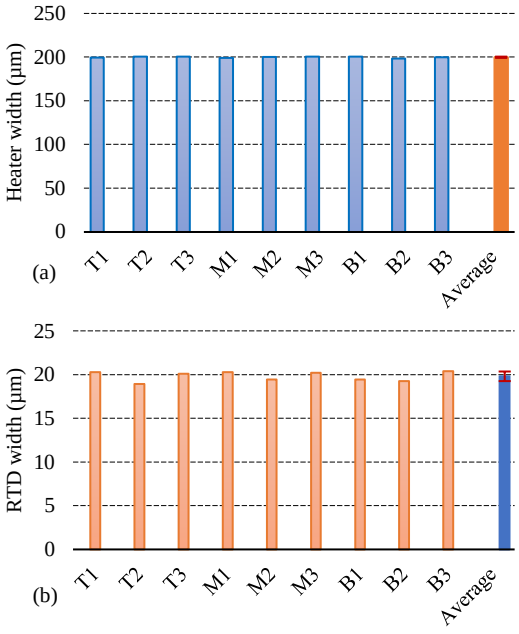

Fig. 5. The widths of (a) heater and (b) RTDs of fabricated wafer, which are 199.89 ± 0.76 μm and 19.82 ± 0.55 μm, respectively. Note: the numbers before and after the plus-minus sign are mean and standard deviation, respectively. This definition applies in the whole paper unless otherwise mentioned.

Besides the heater and RTDs, the active side of chip also contains UBMs as shown by the dots in Fig. 6(a). The UBMs were fabricated for chip-PCB bonding using solder balls. The chip back side was etched for staggered micro-pin fins based on our numerical simulation [45]. The diameter, pitch, and height are 100 μm, pitch 150 μm, and height 220 μm, respectively, as shown in Figs. 6(b,c). The roughness of micro-pin fin side walls due to multi-step etching process can serve as boiling nucleation sites and promote the two-phase cooling.

The chip is bonded to the silicon cap and then soldered to the PCB for electrical connections (Fig. 7). The copper trace CT1, CT2 and CT3 are used for electrical connections of RTD1, RTD2 and heater, respectively.

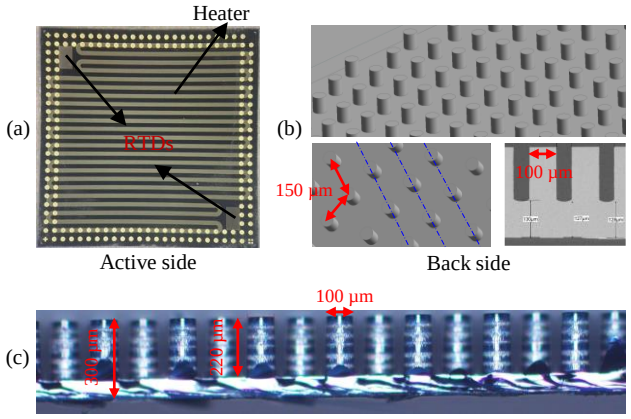

Fig. 6. (a) Chip active side containing a thin-film heater and two RTDs, (b) chip back side is embedded with staggered micro-pin fins of diameter 100 μm, pitch 150 μm, and height 220 μm, and (c) side view of the etched micro-pin fins. Chip footprint is 1 cm $\times$ 1 cm.

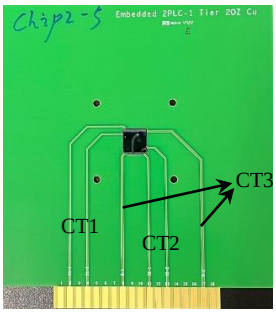

Fig. 7. Photo of the TTV. CT: copper trace. CT1, CT2 and CT3 are used for electrical connections of RTD1, RTD2 and heater, respectively.

The RTDs are calibrated from 25°C to 150°C. Fig. 8 shows the calibration curves. Clearly, the resistance changes linearly as temperature rises. It follows

$$R = R_0 \left[1 + \alpha \left(T - T_0\right)\right], \tag{1}$$

where R_0 and R are the resistances at temperature T_0 and T, respectively, and α is the temperature coefficient of resistance (TCR). $T_0 = 25$°C is the room temperature in present study.

We rearrange (1) and get

$$\left(R - R_0\right)/R_0 = \alpha \left(T - T_0\right). \tag{2}$$

The resistance rise ratio $\left(R - R_0\right)/R_0$ is linear to the temperature rise $\left(T - T_0\right)$. After the mathematical calculation of original data in Fig. 8(a), we plot $\left(R - R_0\right)/R_0$ vs. $\left(T - T_0\right)$ in Fig. 8(b). The curve fitting reveals that α equals to 0.003677/°C, which is used to convert the RTD resistance into the chip temperature in the following tests.

B. Two-Phase Cooling Loop

For proper coolant feeding and collection through the side openings of MPFHS, we designed and fabricated a manifold

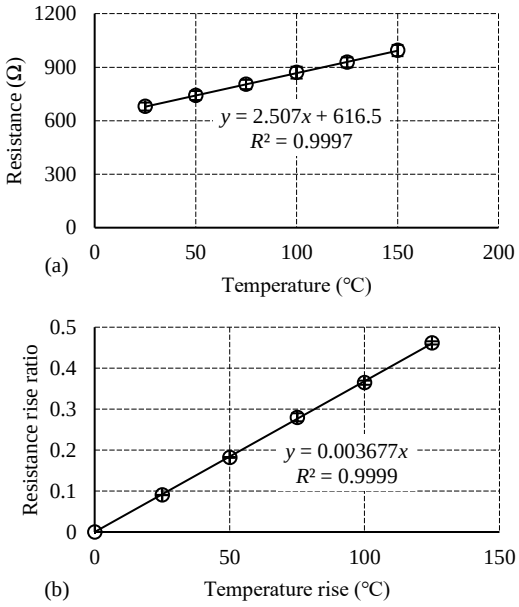

Fig. 8. RTD calibration curves. (a) Resistance vs. temperature, and (b) resistance rise ratio vs. temperature rise. The solid lines are obtained from curve fittings. R^2 is the fitting goodness. Note: the error bars of directly and indirectly measured values are the standard deviations and calculated based on the propagation of uncertainty. This definition applies in the whole paper unless otherwise mentioned.

through 3D printing [46]. The manifold was assembled with TTV via a metal stiffener and screws (Fig. 9). Its bottom surface has a cavity to hold the chip. An O-ring was used for coolant sealing between manifold and TTV. The fabricated manifold and its assembling with TTV are shown in Fig. 10.

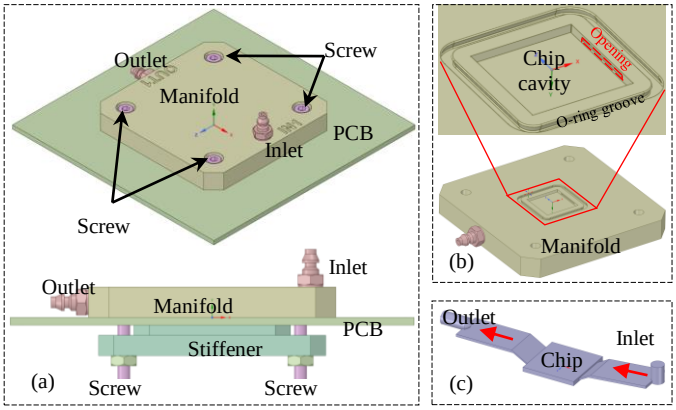

Fig. 9. Manifold design. (a) Assembling with TTV, (b) bottom view of manifold, and (c) coolant flow inside the manifold.

The assembled manifold and TTV were connected into the testing setup for two-phase liquid cooling. The testing setup is composed of a cooling loop and a degassing loop (Fig. 11). In the cooling loop, the coolant (deionized water) is stored in a coolant reservoir (Apache 316SS vessel model 90-1). It goes through a microparticle filter (Swagelok 7.5 μm) before entering a gear pump (Fluid-o-tech gear pump FG204). For safety, a pressure relief valve (Altecnic CA-RS/313430) is installed after the pump. A flowrate sensor (Omega FLR1007)

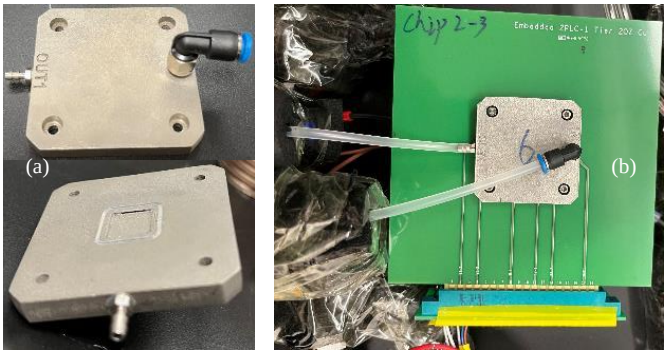

Fig. 10. Photos of (a) 3D printed manifold (EOS M 290, EOS Stainless Steel 316L), and (b) manifold assembled with TTV.

is used to measure the coolant flowrate. A pressure transducer (Omega PX409-015-G10V) and a thermocouple (Omega type-T) are installed to measure the pressure and temperature, respectively, at both inlet and outlet. An air-cooled condenser (EKWB EK-CoolStream PE 360) is used to reject coolant heat to the environment. Bypass 1 is used to regulate coolant flowrate. Bypass 2 is used to run coolant when TTV is not connected in the loop.

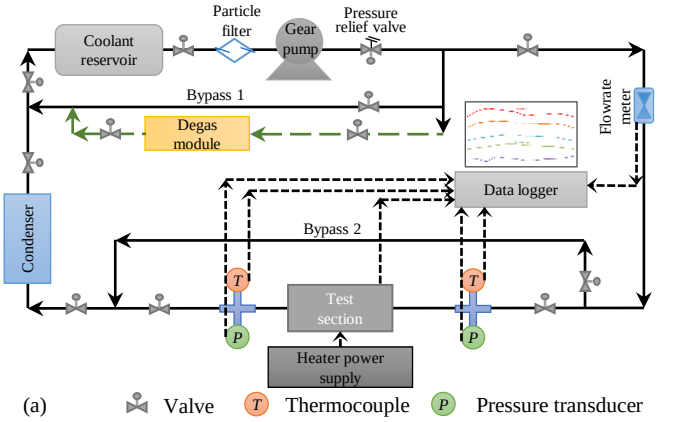

Fig. 11. (a) Schematic illustration and (b) photo of the testing setup. (1) Coolant reservoir, (2) gear pump, (3) flowrate sensor, (4) pressure transducers, (5) thermocouples, (6) TTV, (7) condenser, (8) degas module.

Before the experimental tests, we closed the valves in cooling loop and open these in degassing loop. The deionized (DI) water went through the degas module (GL Sciences

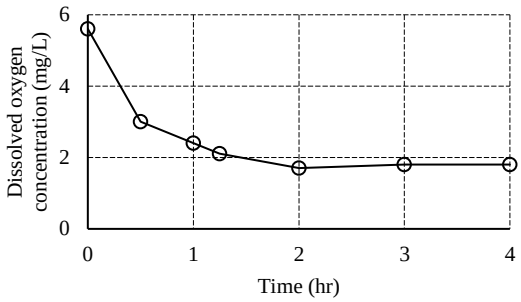

Fig. 12. Variation of dissolved oxygen concentration with time.

Degassing Unit BG-42-10) and got degassed. We measured the concentration of dissolved oxygen in DI water by a dissolved oxygen meter (Fisher Scientific CTL06-662-66) and conducted tests when it reduced a constant value (Fig. 12).

III. Results and Discussion

We carried out cooling experiments at certain coolant flowrates and gradually varied the heat power for each flowrate until the two-phase cooling occurred. The chip footprint is 1 cm $\times$ 1 cm. The coolant inlet temperature is the room temperature 25°C.

Fig. 13 shows the cooling results over time at coolant flowrate 73.2 ± 0.6 mL/min. Within the single-phase regime (time $\leq$ 435 s, heat flux $\leq$ 141 W/cm^2), as the heat flux increases, the coolant outlet temperature and chip temperatures increase, the flowrate slightly increases, and the inlet pressure slightly decreases. The reason is that the viscosity of DI water reduces as temperature increases. Hence, the increasing outlet temperature of DI water leads to a lower flow resistance, and correspondingly a higher flowrate and a lower inlet pressure. When it enters the two-phase regime (time $>$ 435 s in Fig. 13(e)), a part of DI water evaporates and becomes water vapor. Vapor has a much larger volume compared to liquid of the same mass. As a result, the pressure increases (Fig. 13(d)) and the flowrate decreases slightly when entering two-phase cooling.

In addition, the chip temperature fluctuates in the two-phase cooling (Fig. 13(e)). The fluctuation decreases as heat flux decreases (Figs. 13(b,e)). A clearer picture of two-phase cooling can be seen in Fig. 14. As heat flux increases, the pressure drop and pressure fluctuation, chip temperature and temperature fluctuation increase. Strong fluctuations in pressure and temperature are common in two-phase liquid boiling flow [40]–[44], [47], [48]. However, it is not preferable for microelectronics cooling as chip damage may occur due to temporary overheating. Researchers explored various methods to minimize the fluctuations, such as micro- and nano-structures on channel surfaces [34], counter-flow stepped channels [37], and downstream reducing pin fins [42]. In this study, we degassed DI water before experiments to minimize the fluctuation. Numbers in Fig. 14 show means $\pm$ standard deviations as defined in the caption of Fig. 5. The maximum chip temperature fluctuation spans (RTD2 reading) for the three heat fluxes from left to right are 20.7°C, 7.8°C and 12.9°C,

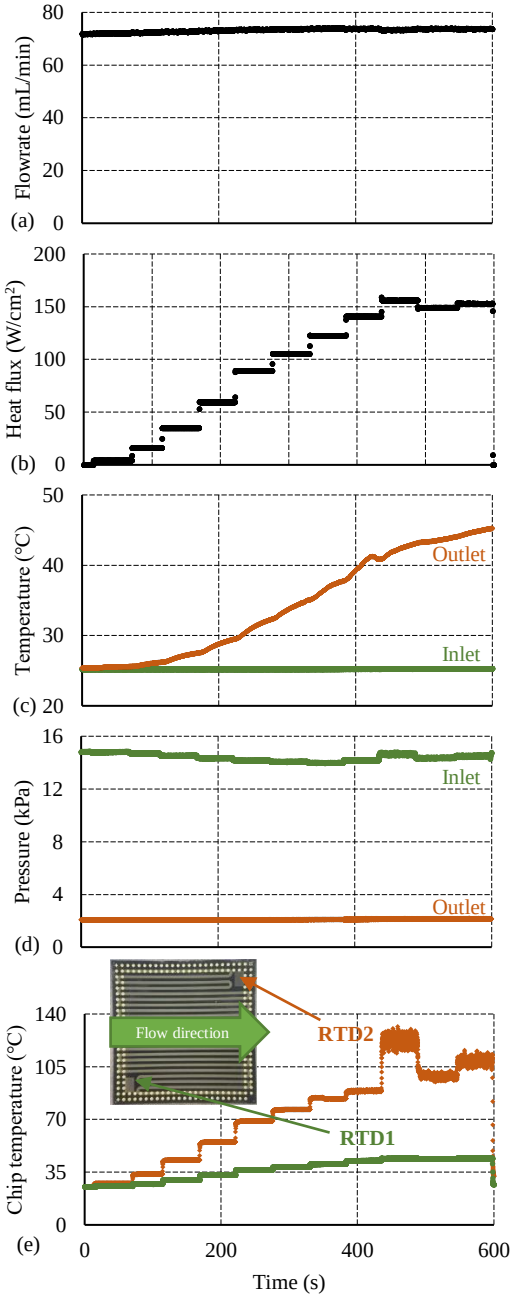

Fig. 13. Cooling results over time at coolant flowrate 73.2 ± 0.6 mL/min. (a) DI water flowrate, (b) heat flux, (c) DI water temperatures at the inlet and outlet, (d) DI water pressures at the inlet and outlet and (e) chip temperatures.

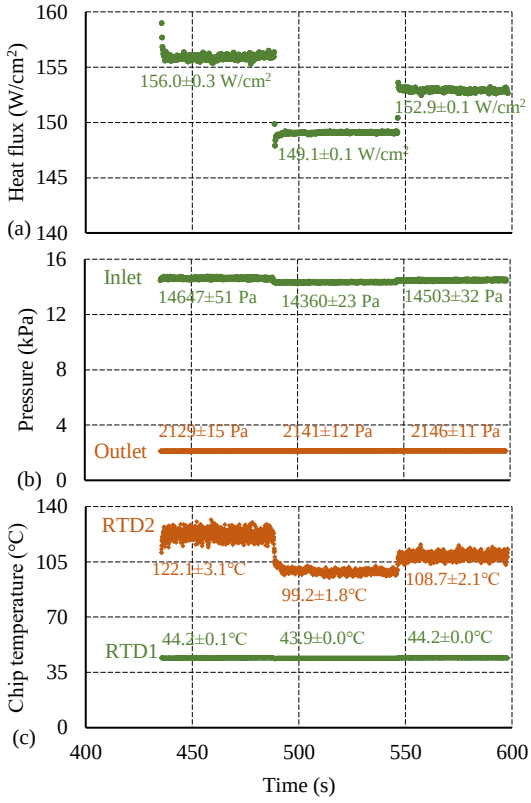

Fig. 14. Variations of (a) heat flux, (b) pressure and (c) chip temperatures with time in the two-phase regime. The maximum chip temperature fluctuation spans (RTD2 reading) in (c) are 20.7°C, 7.8°C and 12.9°C, respectively, for the three heat fluxes from left to right.

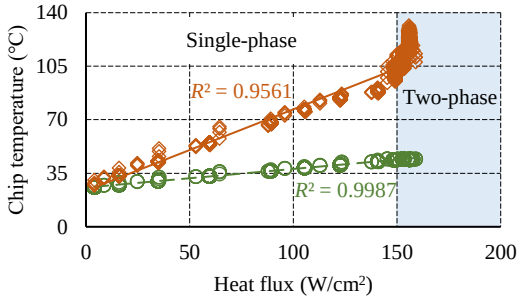

Fig. 15. Variation of chip temperatures with heat flux. The solid and dash lines are obtained from curve fitting. R^2 is the fitting goodness.

respectively (Fig. 14). Clearly, they are significantly smaller compared to the case without degassing [48], demonstrating the effectiveness of current method for chip temperature stabilization.

Fig. 15 clearly presents that, except for the two-phase cooling regime, the chip temperatures roughly linearly increase as heat flux increases. Hence, the chip temperature difference, i.e., the chip temperature gradient, also linearly increases as heat flux increases. The coolant inlet temperature is kept to 25°C. To reduce the chip temperature gradient, we can increase the coolant inlet temperature or the coolant flowrate. As the coolant flowrate increases, the max chip temperature (RTD2 reading) reduces for the same heat flux (Fig. 16). In addition, the maximum heat flux achieved in the two-phase regime also increases with the flowrate.

The maximum chip temperature fluctuation (RTD2 reading) with time in two-phase cooling at different flowrates are shown in Fig. 17. We can see that as heat flux increases, the temperature fluctuation of chip increases. The temperature fluctuations are insignificant under all these different experimental conditions. This demonstrates the effectiveness of degassing for chip temperature fluctuation control in present embedded two-phase liquid cooling.

We compared the two-phase cooling of present study with existing typical literatures on embedded two-phase liquid

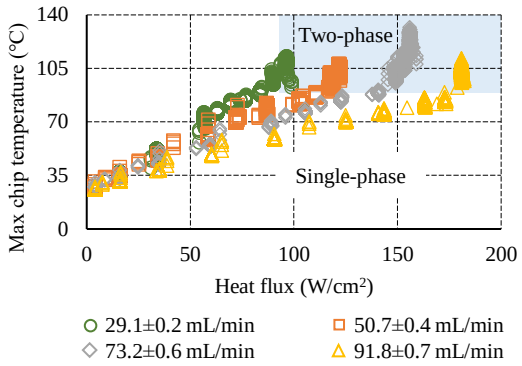

Fig. 16. Variation of maximum chip temperature (RTD2 reading) with heat flux at different coolant flowrates.

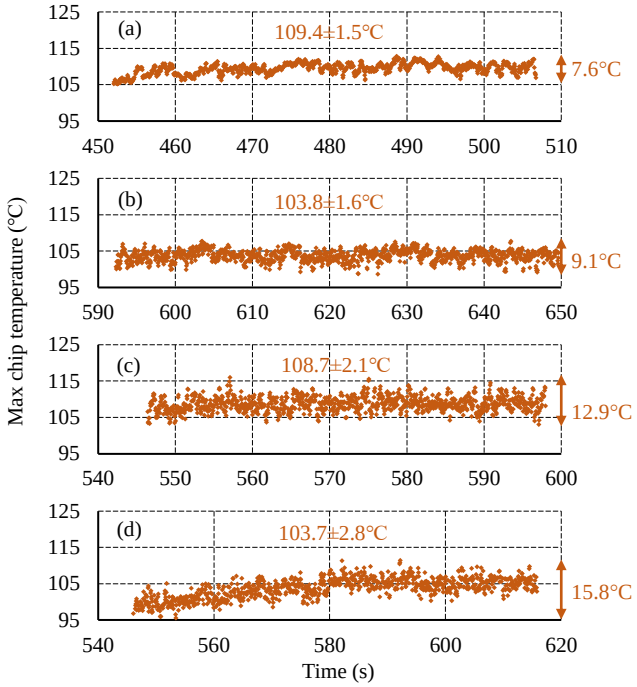

Fig. 17. Max chip temperature fluctuation (RTD2 reading) with time in the two-phase regime under different coolant flowrates and heat fluxes. (a) 29.1 ± 0.2 mL/min and 97 W/cm^2, (b) 50.7±0.4 mL/min and 106 W/cm^2, (c) 73.2± 0.6 mL/min and 153 W/cm^2, and (d) 91.8 ± 0.7 mL/min and 181 W/cm^2. The double-arrowed line on the right vertical axis indicates the temperature fluctuation span.

cooling using DI water as coolant in Fig. 18 and Table I. The heat power, heat flux, chip size ratio (active area over chip footprint) and temperature fluctuation of the chip in two-phase regime are compared and analyzed. Table I shows that our TTV is large in both active area (covered by heater and RTDs) and chip size ratio (active area over chip footprint).

The heat flux in [34] is high, but the heat power is low and the chip size ratio is very small (Figs. 18(a,b)). The chip footprint is 60 times larger than the active area as shown in Table I. The temperature fluctuation of the chip is small (Fig. 18(c)) thanks to the structures of sidewall and the hydrophilic treatment of bottom wall of the microchannel. The structures act as nucleation sites to facilitate liquid boiling, while the hydrophilic treatment helps keep bottom wall from drying out. These two factors work together to make two-phase liquid cooling easier and more stable.

TABLE I
COOLER INFORMATION OF THE LITERATURES COMPARED IN FIG. 18.

Refs.	Cooler	Active area (mm^2)	Chip footprint (mm^2)
[34]	structured microchannel	0.5 × 10	10 × 30
[47]	micro-pin fins	10 × 10	28 × 13.5
[48]	micro-pin fins	10 × 10	10 × 10
[49]	expanding microchannel	1.27 × 1.27	1.27 × 1.27
Ours	micro-pin fins	10 × 10	10 × 10

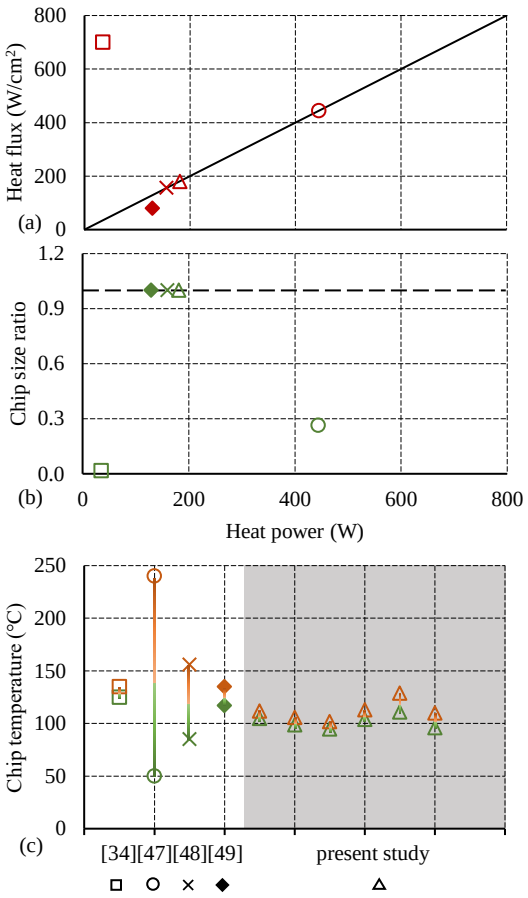

Fig. 18. Comparison with some typical embedded two-phase DI water cooling studies. (a) Heat flux and (b) chip size ratio (active area over chip footprint) vs. heat power, and (c) chip temperature fluctuation span, in the two-phase regime of different studies. The squares, circles, crosses, black diamonds, and triangles indicate data from [34], [47], [48], [49] and present study, respectively. For the present study in (c), the experimental conditions are shown in Table II, listed accordingly from left to right.

TABLE II
EXPERIMENTAL CONDITIONS OF THE PRESENT STUDY IN FIG. 18(C).

Flowrate (mL/min)	29.1	50.7	73.2			91.8
Heat flux (W/cm^2)	97	106	149	153	156	181

Both heat flux and heat power are high in [47], but the chip size ratio is small. The chip footprint is 3.78 times larger than the active area (Table I). More importantly, the chip temperature fluctuates significantly in two-phase regime, ranging from 50°C to 240°C (Fig. 18(c)). The temperature fluctuation of the chip in our preliminary study [48] is smaller compared to [47], but still much larger than other studies.

The chip size ratio in [49] is the same as that of our preliminary study [48] and present study, but the chip size is much smaller (Table I). Besides, the heat flux and heat power are also smaller. By expanding the microchannel along the flow direction, the temperature fluctuation of the chip in [49] is reduced. The reason is that the expanding microchannel facilitates the escape of vapor, thereby reducing the flow instability and temperature fluctuation if the chip.

The triangles in Fig. 18 show the two-phase cooling cases of present study listed in Table II. The active area is of the same size of chip footprint in present study (Table I and Fig. 18(b)). The heat power and heat flux in present study are both relatively large. Although heat power and heat flux in [47] are larger than that in present study, the chip size ratio is small. Furthermore, the temperature fluctuations of the chip are small in all the experimental cases of present study as shown in Fig. 18(c). The fluctuation spans are comparable to that of [34]. The embedded cooler of present study utilizes micro-pin fins, hence, the fabrication process is simpler. The comparison with our previous study without degassing in [48] clearly shows the effectiveness of degassing in reducing chip temperature fluctuations.

IV. Conclusion

In this paper, we developed an embedded two-phase liquid cooling solution for high-power microelectronics. We designed and fabricated a TTV containing a thin-film heater and two RTDs on the active side, with micro-pin fins embedded on the back side. The TTV was tested in a two-phase liquid cooling loop under various coolant flowrates and heat fluxes. The results showed that the chip temperature and temperature gradient linearly increase as heat flux increases. They can both be reduced by increasing coolant flowrate. As coolant flowrate increases, the heat flux occurring two-phase cooling also increases. The chip temperature and system pressure fluctuated in the two-phase regime. By degassing DI water before experimental tests, the fluctuations were greatly reduced under various experimental conditions. This study can facilitate the development of embedded two-phase liquid cooling for true 3D ICs in our next step.

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