Development of Chip to Wafer Assembly with CuSnAg Microbump on Solder on Pad Interposer using Thermocompression and Solder Reflow

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Abstract

Chip to wafer (C2W) bonding to form interconnect is not new to the industry. However, if the bottom wafer has thick (i,e ≥ 10um) Cu RDL layers, the CTE difference between Cu RDL and silicon material of the bottom wafer creates tremendous warpage during any heating or solder reflow process. Post flip chip bonding, this warpage causes cold joints and lead to device electrical failure. We had demonstrated good solder joint connection using thermocompression process with 50um top chip to 775um bottom wafer. The bottom wafer has 3 layers of Cu RDL (each layer is 4um in thickness) and tin silver solder on pads. A detail comparison using thermo- compression and solder reflow process to perform C2W will be explored.

Introduction

Modern electronic requires high performance and high chip density integration packed in a small form factor. One of the approaches is to use 2.5D heterogeneously integrated packaging methodology [1,2] is by combining multiple complex devices together onto an active Si interposer module using ultra fine pitch interconnects. However, 2.5D packaging integration is a big challenge because the dense RDL layers on the active interposer can cause high interposer warpage and prevents ultra-fine pitch bumps of devices from properly forming interconnects with the interposer [3,4]. This result in high assembly yield losses, reliability failure and packaging process challenges.

In a chip to wafer (C2W) process, one way to overcome the warpage induced packaging challenges is to form interconnect to bottom interposer wafer using thermocompression with 50um thin die instead of conventional mass reflow. Thermocompression is done with heated bottom wafer to help reduce module warpage during bonding and prevent stress accumulation and stress induced interconnect failure. Using thermocompression bonding (TCB) in C2W packaging integration, firstly, allows proper mitigation of thermomechanical stress between top die and bottom wafer. During TCB, the top die is heated above SnAg solder liquidus temperature while the bottom substrate wafer stays at a cooler temperature. Because the top chip and bottom wafer have different effective CTE, this temperature difference between top and bottom silicon help mitigate solder joint stress and prevent solder joint crack. In addition, the top die is thin down to 50um, this reduces die elastic modulus and further decreases the package thermo-mechanical stress during assembly heating cycles. Secondly, there are solder on pad (SOP) on the bottom interposer wafer, if thermocompression is not perform properly, the solder from the top die will not melt and merge properly with interposer SOP and causes a different mode of cold joints failure. Lastly, a comparison will be made between TCB and solder reflow process to show how thermocompression is able to prevent cold joint cause by excessive warpage of the thick Cu RDL bottom wafer during package assembly.

Methodology Approaches

Figure 1 shows the schematic diagram of the test vehicle. 2 different dies 6x4x0.05mm and 2x1.8x0.07mm needs to be bonded on the wafer with thick RDL. Tin Silver (SnAg) solder on pad (SOP) is present on the interposer wafer. The SOP is form via electroplating and solder reflow. Figure 2 shows process flow for both thermocompression and normal solder reflow. As shown in the diagram, during a solder reflow process, the entire package is subjected to the same temperature profile, and it is not possible to set a different temperature for the top die and a bottom interposer wafer to mitigate thermal expansion coefficient (CTE) difference between them. This type of uncontrolled heating is suitable for big interconnect pitch that can absorb significant warpage and coplanarity difference between the bonding surfaces but not ideal for smaller pitch devices. In addition, it is a common misconception to regard chip to wafer as a bonding process with mere minute CTE mismatch between top chip and bottom wafer. The mechanical structure and dimensions of both the top and bottom die should be properly reviewed prior to process development. Thus it is important to first understand and characterize the warpage behavior versus temperature of both bonding surfaces before deciding on the right bonding process approach. In this work, the thick RDL layer on the bottom interposer wafer is predicted to cause undesirable warpage during reflow process during assembly hence will have detrimental effect on interconnect integrity. Furthermore, the presence of SOP on the interposer wafer also complicate process development and must be properly investigated.

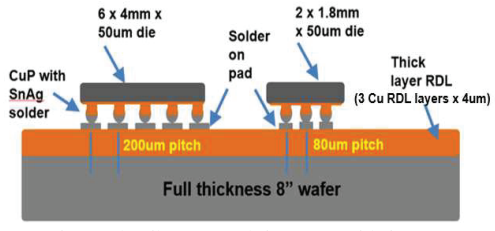


Figure 1. Schematic diagram of the test vehicle

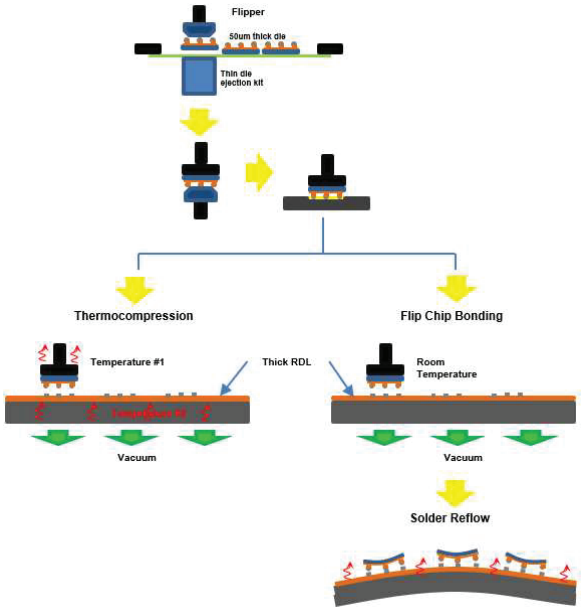
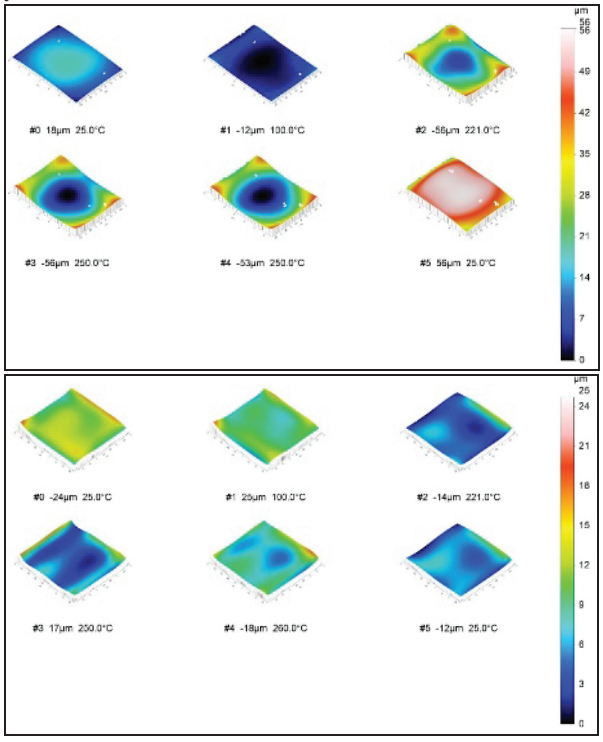


Figure 2: Thermocompression vs Normal solder Reflow Process Flow

To understand why thermocompression is required for a robust C2W process, Warpage behavior of interposer wafer at room temperature and top dies under solder reflow condition is first investigated. Figure 3 shows the warpage profile of the 2 top dies (die back facing up) with respect to temperature using shadow moire. For the bottom wafer, the warpage was measured with IR camera after completing one solder reflow cycle.



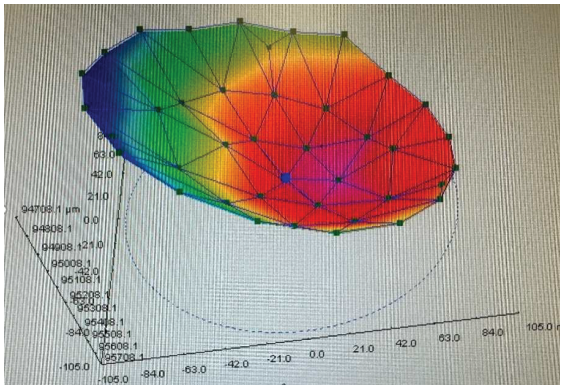


Figure 3: Warpage changes of the die with respect to temperature for 2 top dies (top and middle photos). Bottom photo shows the warpage of a bare bottom interposer after completing one mass reflow cycle and smiling warpage is observed at room temperature.

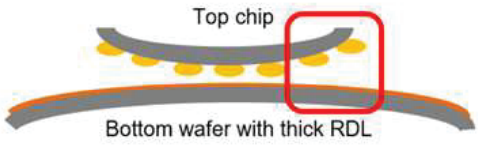


Figure 4: Warpage direction of both top chip and bottom wafer at reflow temperature.

As shown in Figure 3, with bump surface facing down, at peak reflow temperature, both top dies observed smiling warpage. With the thick Cu RDL layer facing up, the bottom wafer will have a crying warpage during peak reflow temperature because the higher CTE Cu RDL layer expands more compares to the silicon portion of the interposer wafer. Hence at high reflow temperature, warpage direction of both bonding surfaces is shown in Figure 4. The warpage behavior provides clues on the die bonding process approach to select. Also in this work, the impact of top die size and bottom wafer solder pad finishing on solder joint formation using solder reflow process will also be investigated. Solder reflow flip chip process is a high-speed process and should always be preferred compared to thermocompression when possible.

Test Vehicle Information

The summary of the test vehicle is shown in Table 1. The bottom wafer has approximately 12um thick RDL. As mentioned, 1 top die with size 6x4x0.05mm and 4 die with size 2x1.8x0.05mm will be bonded on every package of size 11 x 13mm. Bottom wafer is 200mm diameter 0.65mm thickness. Figure 5 showed the bump layout of the 2 top die under X-ray.

Table 1: Test Vehicle's Information

Item	Information
Die size 1	6 x 4 x 0.05mm 12 inch
Pitch and diameter	80um / 200um
Die Size 2	2 x 1.8 x 0.05mm 12 inch

Pitch and diameter	40um / 80um
Package sizes	11x13mm
Bottom Wafer	200mm diameter with 0.65mm thickness; 5µm pad diameter
Solder height	20um for both top dies
Solder Content	SnAgCu

Both SOP and bare Cu bonding pads are evaluated with thermocompression and solder reflow process to understand which process gives good bonding yield.

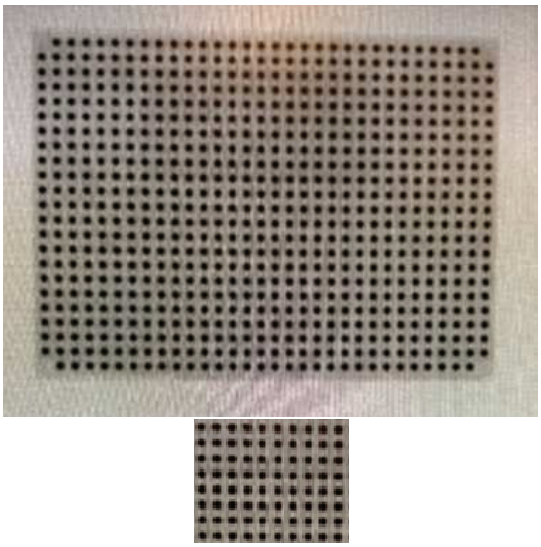


Figure 5: X-Ray Image of big and small die

A few daisy chain structures are designed into a package and can be used to gauge the robustness and integrity of the solder joints after thermocompression and solder reflow. As shown in Figure 6, 12 sets of daisy chain reading can be measured.

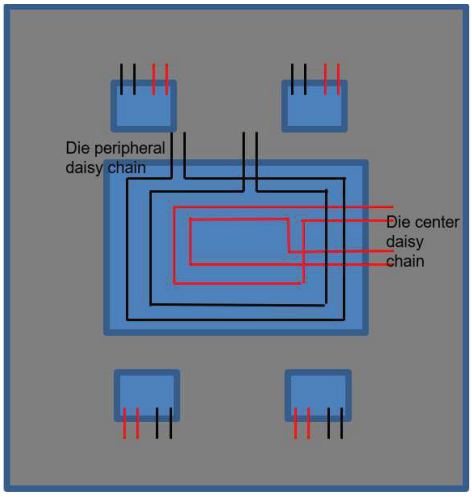


Figure 6: Daisy Chain Groups on the test vehicle

To prepare for the evaluation, firstly, both top dies are backgrinded down to 50um (inclusive of die passivation). Both dies are placed in a special low adhesive tape for ease of die pick up after wafer sawing. Secondly, a special needle pick up mechanism is devised to enable reliable pick up of thin die for bonding. Any die crack during ejection will add complication to the investigation of this work. A 10um dipping plate is use to coat water soluble flux to the solder prior to bonding. Typical thermocompression bonding profile and solder reflow profile is shown in Figure 7. For thermocompression, solder joints are formed directly during the bonding process. As shown in Figure 2, the bottom wafer and top die temperature setting is different. This allows some flexibility to design a bonding process that can cater for difference in CTE between top and bottom bonding material via different peak temperature setting, thereby mitigating the CTE mismatch between them, lowering the risk of interconnect cracking and package warpage. With solder reflow, the entire device experiences the same reflow temperature. The warpage study of top and bottom device shown in Figure 3 and figure 4 suggest that if the top die and bottom wafer is not held flat during bonding, the warpage at the 4 corners of the top die will cause open solder joint failure and no electrical connection. To understand all possible scenarios fully, both top dies with different size are bonded onto the bottom wafer, with and without SOP, using either thermocompression or solder reflow. Table 2 and Table 3 illustrated the tacking parameters for both thermocompression and solder reflow process, respectively.

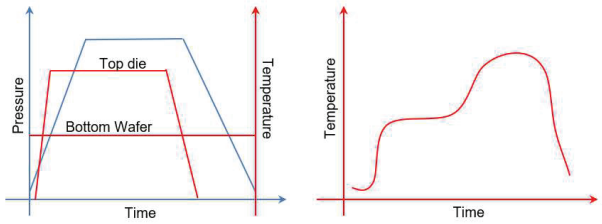


Figure 7: Bonding profile for thermocompression vs solder reflow profile for mass reflow process

Table 2: Thermocompression Bonding Parameters

Run	Temperature	Force (N)
Big top die	≥ 300°C	≥ 10
Small top die	≥ 300°C	< 10
Bottom wafer Temp	≤ 200°C	N.A

Table 3: C4 Bonding Parameters

Run	Force (N)	Bonding Time
Big top die	0.5	200ms
Small top die	0.2	200ms

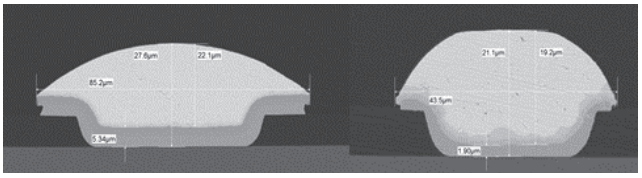


Figure 8: Cross sectional image of the SOP on the bottom wafer.

Figure 8 showed the cross sectional image of the SOP on the bottom wafer. Pure Cu pads will not work with TCB because a stage temperature setting of above 100°C will cause pad oxidation and lead to cold joint complication. On the othe hand, if TCB is done on SOP, there is a separate set of complication that must be overcome. Care must be taken when designing the TCB bonding profile to cater for more robust interconnect formation.

Evaluation of thermocompression versus solder reflow bonding on bottom wafer for 6 x 4mm die

Figure 9 shows post TCB cross sectional picture for 6 x 4mm top die on bottom wafers with SOP. As shown, with careful setup of TCB profile, good solder joint can be formed, Even with thick Cu RDL on the bottom wafer, correct setting of top die temperature and bottom interposer temperature prove it can remove risk of interconnect cold solder joint or solder joint crack. TCB is not done on bottom wafers Cu pad because it is not a feasible solution.

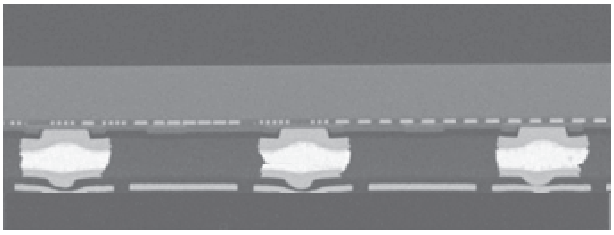


Figure 9: Post thermocompression cross sectional picture for both types of 6 x 4mm top die on bottom wafers with SOP.

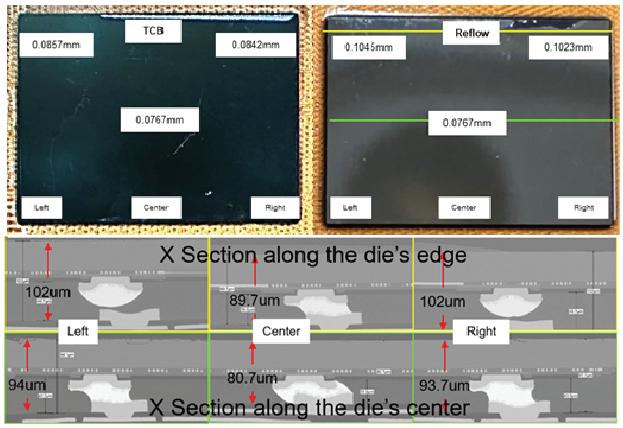


Figure 10: Top shows measured value and location of bottom wafer to top chip gap z height for TCB (left) vs Reflow (Right). Bottom shows different cross section location of solder reflow 6 x 4mm top die on Cu pad bottom wafer, indicating warpage induced cold joints at the 4 corners.

Next, the same experiment is repeated using solder reflow on bottom wafer with Cu pad. Figure 10 top images shows the difference in gap height at different location within a die, measured by focusing method. The result shows post TCB, the bonded top die maintains a uniform gap height. The presence of vacuum on the bonding head and bonding stage helps to hold the top die and interposer in place during TCB interconnect formation. In contrast, during a mass reflow process, both top die and bottom wafers warps freely hence no guarantee that the solders on both bonding surfaces can maintain contact throughout the reflow process. Post reflow gap height measurement result shown in top right image of Figure 10 also shows big gap height discrepancy between corner to die center, indicating warpage. Daisy chain measurement conducted on solder reflow samples also shows open circuit at die peripherals. This indicate that if the bottom wafers has thick RDL layers and warps during reflow temperature cycle, C2W bonding using solder reflow should be avoided.

Finally, reflow is done with SOP on the bottom wafer. As shown in Figure 11, SOP on bottom wafer increases the solder volume, higher solder joint formation yield is observed. The result shows 3 of the 4 corners maintains good solder joint connection while only one corner observed cold joints. The higher volume of solder material helps reduces open joints yield loss. Measuring the device gap height post bonding also helps to visualize advantage of TCB over solder reflow. As shown in Figure 12, TCB samples exhibit one magnitude lower gap height range compares to reflow samples. Gap height is measured by focusing the top of the die and top of the bottom wafer at top left, top right, bottom left and bottom right die corners, then minus die thickness value. TCB can maintain flatness of the top die and bottom wafer during the solder joint formation process while solder reflow with uncontrollable die or wafer warpage makes solder joint formation up to chance.

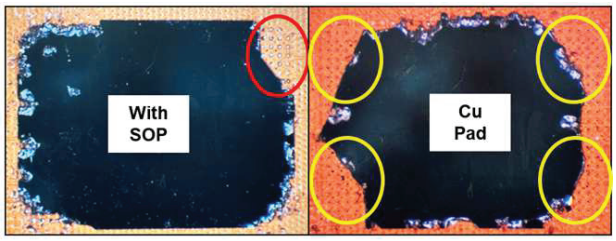


Figure 11: Post 6 x 4mm die shear failure mode inspection shows, solder joints still forms 3 out of 4 corners (cold joints observed on the red circles) for SOP bottom wafer on left image compare to right image uses solder reflow of top die to Cu pad bottom wafer with 4 corners having cold joint.

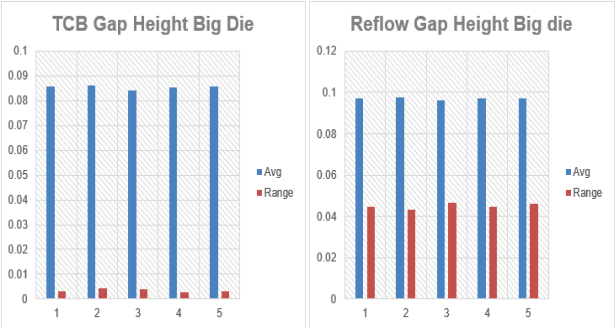


Figure 12: Left table is gap height of 6 x 4mm die bonded with TCB. Right Table shows same device gap height running reflow process. Result shows reflow gap height that is one magnitude higher compared to TCB.

Evaluation of thermocompression versus solder reflow bonding on bottom wafer for 2 x 1.8mm die

The experiment is repeated with smaller 2 x 1.8mm top die on the same thick RDL bottom wafer. As expected, the TCB result of smaller die is the same as 6 x 4mm TCB result. As shown in Figure 13, solder joint formed is similar to big die with no observed anomalies. Measured post TCB Gap height is shown in Figure 14. Gap height trend of 4 corners of the die are similar to TCB big top die.

Figure 13: Post thermocompression cross sectional picture for 2 x 1.8mm top dies on bottom wafers with SOP.

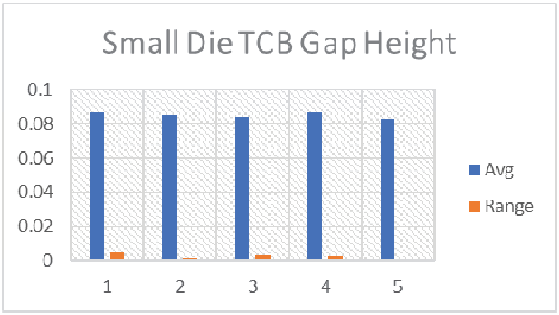


Figure 14: Gap height of 2 x 1.8mm die TCB on SOP bottom wafer

As shown in Figure 15, with solder reflow, small die can still form good solder joints despite the warpage of the bottom wafers during the reflow temperature range. This suggest smaller die area can better navigate and conform to bottom wafer warpage.

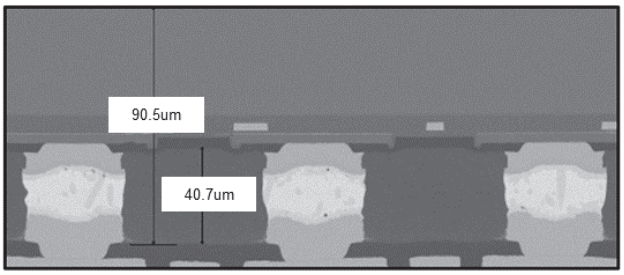


Figure 15: Post solder reflow cross sectional picture for 2 x 1.8mm top dies on bottom wafers with SOP.

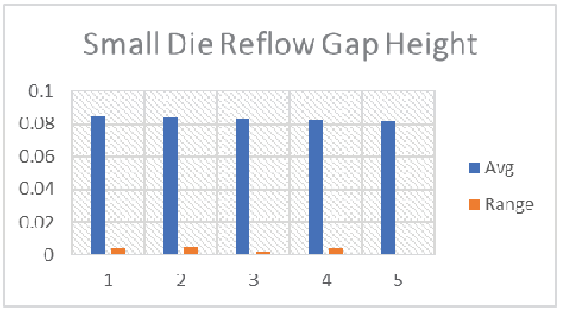


Figure 16: Gap height of 2 x 1.8mm die reflow on SOP bottom wafer

Figure 15 shows the cross section of the interconnect between top die and bottom wafer form with solder reflow process. No difference observed when comparing the gap height data of post bonded small die between TCB and reflow process as shown in Figure 14 and 16.

Results and discussions

Based on the cross-section result, gap height measurement and daisy chain resistance value measurement of the bonded dies using both TCB and solder reflow, the result overview is shown in Figure 17. For larger top die size devices, when performing C2W on thick Cu RDL bottom wafer with SOP, it is crucial to manage and mitigate the thermal induced warpage using TCB. Solder reflow process should only be chosen for small die size devices that is able to better conform to bonding surface warpage. In the beginning, it is important to measure thermal induced device warpage and perform gap height measurement of top die after bonding to the interposer. This will provide better judgement on bonding process selection with higher chance of success.

	TCB		Reflow	
	6 x 4mm	2 x 1.8mm	6 x 4mm	2 x 1.8mm
Cu Pad	⊘	⊘	⊘	○
SOP	○	○	⊘	○

○ Reliable Process ⊘ Not Reliable Process

Figure 17: TCB and Reflow Process Bonding Result based on cross section inspection, gap height measurement and daisy chain resistance measurement.

Conclusions

Chip-to-Wafer (C2W) Bonding process development study result summary comparing TCB and solder Reflow bonding on thick Cu RDL bottom wafer is shown below

(a) Understanding thermal induced warpage characteristic for both top die and bottom wafer from the get-go is important to aid bonding process selection
(b) Even with thin and flexible 50um die, using reflow process is not possible for silicon-to-silicon C2W bonding because of surface warpage at elevated temperature
(c) Presence of SOP on the bottom wafer is not sufficient to ensure reflow process bonding success.
(d) Gap height measurement can be used to gauge eligibility of using solder reflow during bonding process. Cross section and daisy chain measurement for confirmation
(e) The die shear and cross section result shows cold joint is magnified by having larger top die size and lower solder on pad cap height.

Acknowledgments

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