Design of a Current Sense Amplifier with Dynamic Reference for Reliable Resistive Memory

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***Abstract*—Resistive random-access memory (RRAM), as an emerging memory, has a resistance difference between a high resistance state(HRS) and a low resistance state(LRS). It has received a lot of attention due to its large R-ratio (R_{HRS}/R_{LRS}), high density, and low power consumption. However, the wide resistance variation of RRAM makes it suffer from read errors due to the limited sensing margin. To improve the sensing margin and resistance to variations, this paper proposed a current sense amplifier (CSA) assisted with dynamic reference (DR-CSA) for RRAM. Compared with the conventional CSA, the proposed sense amplifier reduces the read latency and energy by up to 53% and 30%, respectively. Simulation results show that the proposed DR-CSA achieves a read latency of 0.84 ns for a 64Kb RRAM array with a reading current of 1μA at 1.1 V.**

***Keywords*—resistive random-access memory (RRAM), high resistance state (HRS), low resistance state (LRS), current sense amplifier(CSA), dynamic reference current sense amplifier(DR-CSA), r-ratio, sensing margin**

I. Introduction

Due to the emergence of data-intensive applications such as data mining and cloud computing, high-density memories have become increasingly necessary [1]. As a result, hard disks have been replaced by flash memory, which is better suited to meet these requirements. However, flash memory is still limited by its write mechanism, which is based on tunneling [2-3]. As an alternative, resistive memory (RRAM) is highly regarded as a next-generation nonvolatile memory due to its various advantages such as non-volatility, high endurance, low latency in read/write operations, large R-ratio (R_{HRS}/R_{LRS}), compatibility with the CMOS process, and low supply voltage [1-6].

The structure of an RRAM device consists of three layers and two terminals, as shown in Fig. 1(a). The insulator layer is responsible for reversible electric-field-induced switch resistance from conductive filaments. This leads to a low resistance state (LRS) when the filament is formed. Similarly, a high resistance state (HRS) occurs when the filament ruptures. Typically, a bit-cell (1T1R) is created by combining an RRAM with a transistor, where the transistor controls the access of the bit-cell. Even though RRAM offers various benefits, there are still significant challenges to overcome, including resistance variations during fabrication and resistance drift over usage time. Fig. 1(b) demonstrates how resistance variation and drift can result in smaller R-ratios (R_{HRS}/R_{LRS}), which can cause read errors due to decreased sensing margins [4-8].

Different sensing schemes have been developed to incorporate resistance variations and increase sensing

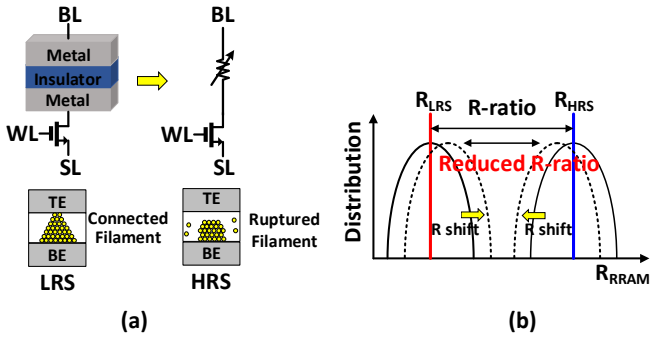

Fig 1. (a) 1T1R structure and equivalent circuit and (b) resistance variation in RRAM.

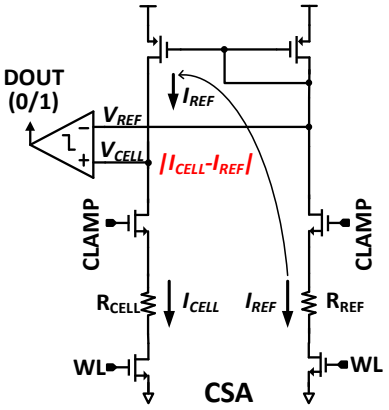

Fig. 2. Schematics of conventional current-mirror-based CSA [9].

margins, but these multi-step sense amplifiers require substantial sensing delay to achieve improved sensing margins [10,12]. This work proposes a current sense amplifier that uses dynamic reference voltage to enhance variation tolerance and sensing time without additional delay.

II. Background and Proposed Design

A. Conventional Current-Mirror-Based Sense Amplifier

Fig. 2 shows the conventional current-mirror-based CSA [9]. The reference current (I_{REF}) is determined as the average of the current values during both HRS and LRS (i.e., $I_{REF} = (I_{HRS} + I_{LRS}) / 2$). During a read operation, both V_{CELL} and V_{REF} are simultaneously generated based on the difference between the cell current (I_{CELL}) and the reference current (I_{REF}). The sensing margin is directly proportional to $|I_{REF} - I_{CELL}|$ [9]. However, the resistance fluctuations in R_{CELL} and R_{REF} result in a decrease in the worst-case $|I_{REF} - I_{CELL}|$, which compromises the sensing margin and sensing window. Additionally, the sensing margin is further decreased due to the offset voltage in the relevant devices, such as the comparator input devices, the PMOS current mirror, and the

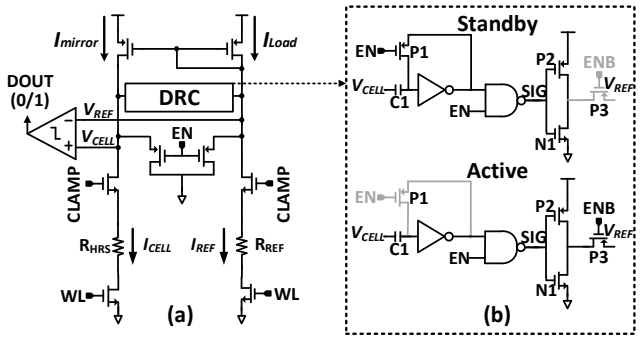

Fig. 3 (a). The proposed current sense amplifier and (b) the dynamic reference controller (DRC) architecture.

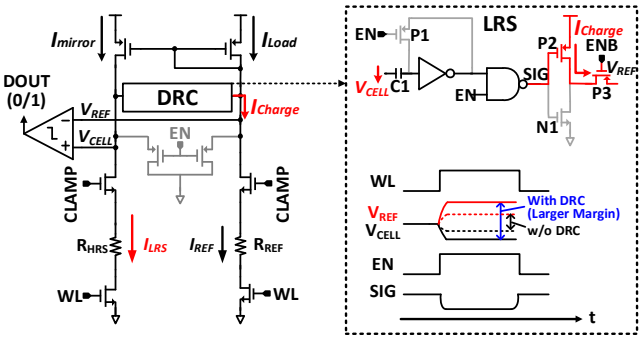

Fig. 4. Operation of DRC for sensing margin improvement in sensing LRS.

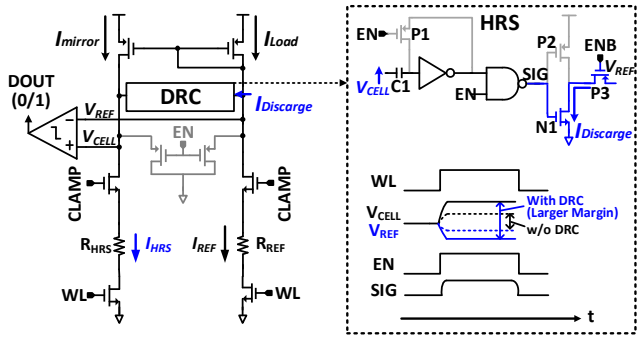

Fig. 5. Operation of DRC for sensing margin improvement in sensing HRS.

clamp devices [9-10]. As a result, the conventional CSA with a small R-ratio is not robust enough for RRAM.

To address this issue and improve the sensing margin, two alternative CSAs, namely the two-step (DS-CSA) and three-step (TS-CSA) current sense amplifiers, were proposed. The DS-CSA alters the current path and comparator input node using a switch with two steps to develop a sensing margin separately at V_{CELL} and V_{REF}. In the first step, the current path follows the pattern shown in Fig. 2, and the sensing voltage is developed for V_{CELL} (i.e., (I_{REF} - I_{CELL})) at the first input node of the comparator. In the second step, the current path is changed by a switch, and the sensing voltage for V_{REF} (i.e., (I_{CELL} – I_{REF})) is formed at the second input node of the comparator [10]. The TS-CSA utilizes a three-step process with a switch. When the sensing operation begins, a different overdrive voltage is generated for both I_{CELL} and I_{REF} at the current path load. This voltage is then replicated using capacitor coupling as another current path load, and the increased current from this load generates a larger current difference [12]. As a result, these two CSA types improve the sensing margin compared to the conventional CSA with the switches and the additional steps [10,12]. However, as mentioned earlier, both sense amplifiers improve the sensing margin at the cost of additional sensing delay.

A covalent-bonded current sense amplifier (CB-CSA) addresses this delay issue by increasing the sensing margin through its structural design, rather than by using switches and additional steps. The CB-CSA consists of two latches and three cells that use both a unit HRS cell and a unit LRS cell as a reference cell surrounding data cells, similar to a covalent structure. This CSA uses the unit cell reference current for sensing instead of a standard reference current (i.e., I_{REF} = (I_{HRS} + I_{LRS}) / 2), resulting in an improved sensing margin compared to the conventional CSA. The current sense amplifiers can be shared with the reference cell column current mirror in the array [13]. However, CB-CSA requires relatively more reference arrays due to the additional reference array used to house the unit cells, and the covalent structure creates difficulties when sharing a reference current [11].

B. Proposed Dynamic Reference Current Sense Amplifier

The proposed dynamic reference current sense amplifier for RRAM sensing is shown in Fig. 3(a), which comprises a CSA and a dynamic reference controller (DRC). The DRC is connected with a comparator and is enabled during RRAM sensing. It consists of a capacitor, basic logic gates, and PMOS switches that adjust the current mirror's reference current (I_{REF}) after the sensing capacitor (C1) detects the early-stage change at V_{CELL}.

In standby mode, V_{CELL} and V_{REF} are set to VDD/2 by turning on EN. The DRC can pull up and down around VDD/2 to detect cell states, while P1 maintains the inverter input and output close to the trip-point state with a large gain, and P3 decouples DRC from V_{REF} and V_{CELL}.

During sensing mode, the DRC block is activated after pulling up EN, and the feedback path controlled by P1 is disabled, and P3 connects the DRC output to the V_{REF} node. After C1 detects the cell state, an additional current path is formed by N1 or P2 and is connected to the V_{REF} node. This path is determined by 'SIG', which the NAND gate generates depending on cell states with another side '1' of EN.

For example, Fig. 4 shows the sensing of the LRS state. The initial voltage difference between equalized V_{CELL} and V_{REF} starts to develop when the sensing operation starts. When reading the LRS state (I_{CELL} > I_{REF}), I_{CELL} and I_{REF} flow through the clamping transistor, the accessed RRAM, and the selector. The LRS state pulls down V_{CELL} below VDD/2, which generates a small voltage drop at the inverter input node through capacitive coupling. Therefore, the 'SIG' node becomes '0,' which turns on P2 and provides an additional pull-up current (I_{Charge}) to I_{Load_Low}. Then, I_{REF} can be rewritten as 'I_{load} + I_{Charge},' resulting in I_{load} decreasing by I_{Charge}, which increases V_{REF}. The decreased I_{load} is copied to I_{Mirror}, decreasing V_{CELL} further, and developing the voltage difference between V_{REF} and V_{CELL} through the feedback operation in DRC.

Fig. 5 shows the sensing operation when accessing an RRAM in HRS. When reading HRS (I_{CELL} < I_{REF}), V_{cell} is formed slightly above VDD/2, which is coupled into DRC through C1, leading to an additional pull-down current path through P3 and N1. As a result, I_{Load_high} increases by the amount of $I_{Discharge}$, which is copied by the current mirror and

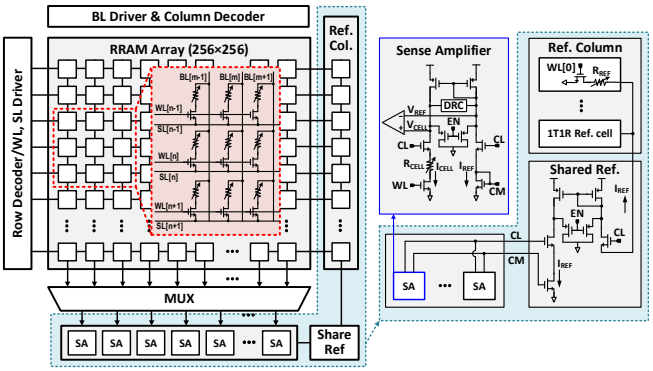

Fig.6. Architecture of the RRAM array and structure of sharing the way reference current.

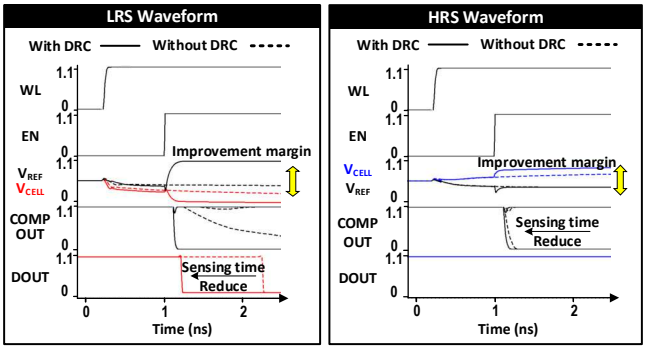

Fig. 7. The simulation results comparing the sensing margins of the CSA with the proposed DRC and the conventional CSA without DRC during LRS and HRS.

further raises V_{CELL} to a higher level, improving the sensing margin.

The proposed CSA is implemented in a 64Kb RRAM array architecture, as shown in Fig. 6. The reference current generator is shared with other sense amplifiers to minimize the reference area, and the array consists of 256 × 256 RRAM cells with 32 sub-arrays, requiring 32 sense amplifiers. The shared reference column consists of reference cells with combined LRS and HRS, which can be shared with multiple sense amplifiers by copying the reference current through 2-stage current mirrors.

III. Simulation Result And Comparision

The 64Kb RRAM array with the proposed sense amplifier is implemented using 40nm CMOS technology and simulated at a supply voltage of 1.1 V. The RRAM model used in the simulation incorporates HRS/LRS resistances of 950 KΩ/9 KΩ with a 10% variation. The RRAM model generates an I_{REF} of 1.5 µA, I_{HRS} of 300 nA, and I_{LRS} of 2.5 µA. The employed Verilog-A RRAM device is based on the TaO_X RRAM stack [15]. Fig. 7 illustrates the sensing operation of the proposed CSA in comparison with the conventional one.

During LRS sensing, DRC increases the voltage difference between V_{CELL} and V_{REF} by turning on WL and EN sequentially. The proposed CSA generates pull-up I_{Charge} when 'SIG' becomes '0', which decreases I_{load} to form a higher V_{REF}, as shown in Fig. 7. The lowered swing of V_{CELL} affected by V_{REF} further enhances the sensing margin (V_{REF} - V_{CELL}), improving the sensing speed significantly. In contrast, during HRS sensing, SIG of '1' injects an additional pull-down current that increases I_{load}, lowers V_{REF}, and raises V_{CELL},

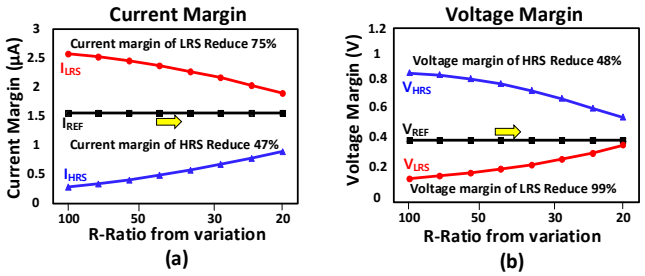

Fig. 8. Result of the conventional CSA (a) margin of current and (b) margin of the comparator with R-ratio.

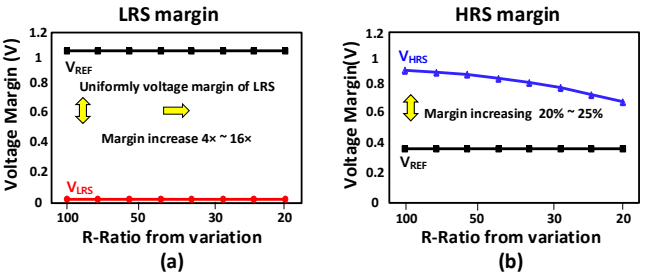

Fig. 9. Result of the proposed CSA margin of the comparator with R-ratio in the variation of (a) LRS, (b) HRS.

as shown in Fig. 7. However, the diode-connected load limits the lowering of V_{REF}, affecting the rising swing of V_{CELL}. Thus, the charge current effect is better than the discharge current effect. While the proposed sensing scheme may cause margin imbalance by improving the sensing margin for LRS more than for HRS, this technique effectively tackles the challenging LRS sensing issue in the conventional CSA. The robustness of the proposed sensing scheme is evaluated after considering RRAM variation. Given that RRAM devices exhibit larger variations, the investigation confirms the effectiveness of the proposed sensing scheme in improving overall sensing performance.

The simulated results of the current and voltage margins of the conventional CSA with R-ratio variations from 100 to 20 are shown in Fig. 8. Fig. 8(a) illustrates that the current margin decreases from 1 µA to 250 nA in the LRS and from 1.2 µA to 660 nA in the HRS as the R-ratio degrades from 100 to 20. The corresponding voltage margin is shown in Fig. 8(b), which reveals that the current and voltage margins for sensing LRS are more vulnerable to R-ratio degradation than those for sensing HRS. In fact, the sensing LRS experiences a voltage margin degradation of 99%, as indicated in Fig. 8(b). Thus, the conventional CSA with a current mirror load structure shows that R-ratio is vulnerable to LRS, mainly due to the increased delay of LRS sensing as the R-ratio decreases.

Fig. 9 shows the proposed CSA margin in a comparator with R-ratio degradation. As depicted in Fig. 9(a), the proposed CSA has no degradation in the margin for LRS by changing both V_{REF} and V_{CELL}, improving the margin by approximately by 4x~16x, since the reduced I_{load} remains consistent despite the decrease in the ratio. As explained earlier, Fig. 9(b) shows an increased margin of ~20% to ~25% more than the conventional CSA in reading HRS, although it is less than the increase rate of LRS.

Fig. 10 presents the simulated results of the comparator delay and the overall sensing time. It can be observed that the proposed CSA significantly reduces the comparator delay

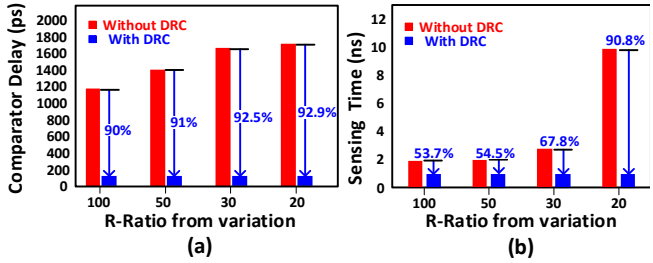

Fig. 10. Comparison of CSA with DCR and without DRC: (a) comparator delay and (b) sensing time.

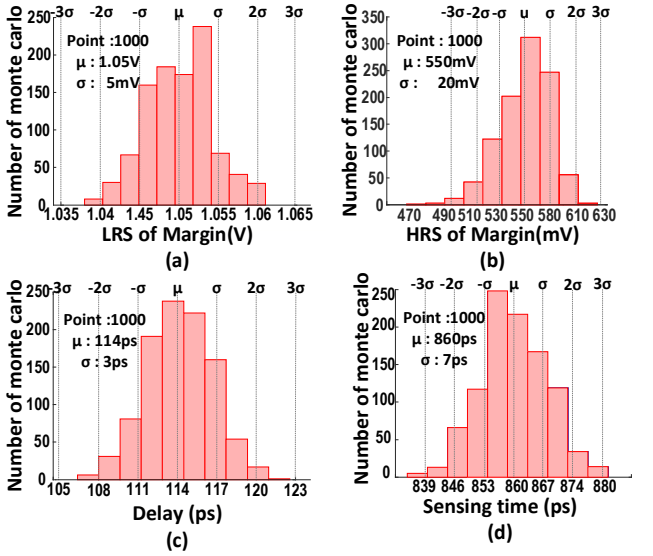

Fig. 11. Monte Carlo simulation results: (a) margins in LRS, (b) margins in HRS, (c) comparator delay and (d) sensing time.

due to the increased sensing margin. As shown in Fig. 10(a), when the R-ratio decreases from 100 to 20, the comparator delay increases from 1.2 ns to 1.7 ns in the conventional CSA. However, in the proposed CSA, the comparator delay is maintained at around 120 ps regardless of the R-ratio variations, thanks to the increased sensing margin. This represents a delay reduction of more than 90% compared to the conventional CSA.

Despite the decrease in the current margin that occurs with R-ratio variations, the proposed CSA can maintain sensing speed regardless of R-ratio. This is demonstrated in Fig. 10(b), which summarizes the sensing time comparison. The proposed CSA reduces sensing time by approximately 53% to 90%, even with R-ratio degradation from 100 to 20. In contrast, the conventional CSA increases the delay time for loading to compare the difference on the small sensing margin when the R-ratio is decreased. As a result, when the R-ratio is degraded to 20, the sensing delay increases significantly due to the sensing margin of a few tens of millivolts, as shown in Fig. 8(b). The simulation shows that the sensing time increases from 1.95 ns to 10 ns. On the other hand, the proposed CSA maintains the same sensing time average of around 1 ns from ~0.84 ns to ~1.07 ns. Additionally, the proposed CSA can improve energy efficiency based on the fast sensing time. Fig. 11 presents the Monte Carlo simulation result with 1000 samples to confirm the robustness of the proposed CSA scheme. Fig. 11(a) and (b) show the sensing margins of LRS and HRS. In LRS, the sensing margin has μ = 1.05 V and σ = 5 mV. HRS's sensing margin has μ = 0.55 V and σ = 2 mV, when employing 3σ variations. Fig. 11(c) and (d) show the comparator delay and the sensing time. The access time has μ = 0.86 ns and σ = 7p s. The proposed CSA have good robustness of performance.

TABLE I: PERFORMANCE WITH THE COMPARISON

	JSSC'20[12]	TCSAII'15[10]	ISSCC'15[11]	This work
Process	55 nm	45 nm	Sub-20 nm	40 nm
Supply voltage	1V	1V	1.5V	1.1V
Iread	–	15 uA	2 uA	1 uA
Sensing time	3.16 ns (Test Measure)	3.4 ns (Test Simulation)	9.1 ns (Test Measure)	0.84 ns (Test Simulation)
Array (Sub-array)	1Mb 128k(256X512)	32Mb (Sub unknow)	8Mb 0.5M(512x1028)	64Kb 2k(256X8)
	* : Simulation performance with same array, Iread , and 40nm CMOS			
Vmargin*	500mV(LRS) 483mV(HRS)	600mV(LRS) 700mV(HRS)	590mV(LRS) 550mV(HRS)	1050mV (LRS) 540mV (HRS)
Sensing time*	1.64n	1.8n	0.64n	0.84n
Read energybit*	44.922fJ(SA) 282.85fJ(Sub-array)	22.296fJ(SA) 260.722fJ(Sub-array)	10.77fJ(SA) 244.40fJ(Sub-array)	10.17fJ(SA) 235.16fJ(Sub-array)
Merit	Reference share Margin balance	Reference share Margin balance	Read speed Margin balance	Read speed Reference share
Drawback	Read speed	Read speed	Reference share	Margin imbalance

Sensing time* : measure from starting WL on to generate a digital output.
Vmargin* : (VCELL-VREF).
SA*: only sense amplifier power, Sub-array*: The power with sub array.
Set current: LRS 2.5uA, REF 1.5uA, 300nA

Table I summarizes the performance comparison with other styles of state-of-the-art CSAs. The table includes results from simulations conducted under the same conditions. The proposed DR-CSA improves sensing time by 2.3×, 2.1×, and 1.9× compared to the conventional CSA [9], DS-CSA [10], and TS-CSA [12], respectively. Additionally, the proposed DR-CSA improves energy efficiency by 17%, 9.8%, and 3.8% compared to DS-CSA, TS-CSA, and CB-CSA [11], respectively. Finally, this work achieves higher speed without requiring an additional reference array by sharing one reference column with multiple sense amplifiers.

IV. CONCLUSION

This paper proposed a novel dynamic-reference current sense amplifier (DR-CSA) that is specifically designed to ensure reliable RRAM sensing despite significant variations in RRAM device characteristics. The DR-CSA approach enhances the sensing margin by dynamically adjusting the load current based on the early-stage voltage change that occurs in the accessed column. The simulation results demonstrate that the DR-CSA outperforms several state-of-the-art CSAs in terms of robustness, access time, and energy efficiency. Therefore, the proposed DR-CSA is particularly well-suited for use in various resistive memory systems that require fast and reliable sensing capabilities.

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