Reduced TCF, High Frequency, Piezoelectric Contour-Mode Resonators with Silicon-on-Nothing

Sagnik Ghosh
Sensors, Actuators and Microsystems
Institute of Microelectronics, A-STAR
Singapore
Sagnik_Ghosh@ime.a-star.edu.sg

Jaibir Sharma
Sensors, Actuators and Microsystems
Institute of Microelectronics, A-STAR
Singapore
sharmaj@ime.a-star.edu.sg

Eldwin J. Ng
Sensors, Actuators and Microsystems
Institute of Microelectronics, A-STAR
Singapore
eldwin_ng@ime.a-star.edu.sg

Duan Jian Goh
Sensors, Actuators and Microsystems
Institute of Microelectronics, A-STAR
Singapore
Goh_Duan_Jian@ime.a-star.edu.sg

Srinivas Merugu
Sensors, Actuators and Microsystems
Institute of Microelectronics, A-STAR
Singapore
merugus@ime.a-star.edu.sg

Yul Koh
Sensors, Actuators and Microsystems
Institute of Microelectronics, A-STAR
Singapore
Koh_Yul@ime.a-star.edu.sg

Amit Lal
Electrical and Computer Engineering
Cornell University
New York, United States
amit.lal@cornell.edu

***Abstract*—This paper describes microelectromechanical systems (MEMS) contour mode resonators (CMRs) with 900MHz resonant frequencies suitable for radio frequency (RF) applications, using a ~2µm thick degenerately doped n-type silicon (Si) layer. The Silicon-on-Nothing (SON) process has been used to fabricate monocrystalline thin pre-released Si membranes over cavities with well-controlled thickness across the wafer. A thin layer of 15% scandium (Sc)-doped aluminum nitride (AlN) has been incorporated in the vertical stack of the CMRs for piezoelectric transduction. The CMRs were aligned to the <100> crystal orientation of a (100) Si substrate to obtain a reduced temperature coefficient of frequency (TCF) of -7.4ppm/°C.**

Keywords—Microelectromechanical systems (MEMS), contour mode resonators, radio frequency (RF), Silicon-on-Nothing (SON), degenerate doping.

I. Introduction

In the past decade, microelectromechanical systems (MEMS) resonators have been dominating the market for time and frequency reference devices in the state-of-art communication and signal processing circuits as compared to traditional quartz-based resonators, which are bulky and are not compatible with complementary metal oxide semiconductor (CMOS) fabrication processes. Surface acoustic wave (SAW) resonators and film bulk acoustic wave resonators (FBARs) are the mainstream resonators commonly employed towards moderate to high frequency applications. With the recent rising popularity of Internet-of-Things (IoT), there is a demand for small, low power, low-cost, radio frequency (RF) elements for wireless communication. The large size of SAW resonators have been a barrier towards small chip integration. Although FBARs are small, the resonant frequency of the FBARs is largely dictated by the thickness of the vertical stack of thin films, with only a narrow range of frequencies achievable with a given stack. MEMS contour mode resonators (CMRs) can be a potential alternative to the SAW resonators and FBARs owing to the small form factor and the ability to realize a broad range of frequencies on a single chip.

Modern communication system requires high precision commercial oscillators which must be stable across a wide range of parameters as well as across a wide temperature range [1]. Industrial applications commonly use temperatures ranging between -40°C to 85°C. Conventional MEMS piezoelectric-on-silicon resonators generally suffer from large temperature coefficient of frequency (TCF) which is typically around ±30ppm/°C, as compared to zero first-order TCF for quartz crystal resonators [2]. Both active and passive temperature compensation techniques have been applied to reduce the TCF of MEMS resonators. Although active temperature compensation techniques, such as electronic compensation [3] and micro-heater based ovenization [4], have resulted in near-zero ppm level of frequency stability with temperature, the need for additional circuitry adds complexity to the system as well as increases the overall power consumption. In contrast, passive temperature compensation techniques do not require any additional electronic circuits and are attractive for IoT applications that prize low power and cost. For passive temperature compensation, the intrinsic properties of constituent layers forming the device and the device geometry are tuned [5-8] to reduce TCF. As each constituent material within the vertical stack of the resonator contributes to the overall TCF of the device, adding materials with opposite temperature coefficient of elasticity (TCE), reduces the overall TCF of the resonator. While most materials have a negative TCE, silicon oxide has a strongly positive TCE and is often added to resonators for TCF reduction [5]. For silicon (Si) resonators, utilizing a high doping level [6] together with aligning the devices to particular crystal orientations [7] has been shown to achieve similar TCF reduction effects. Compared to silicon oxide, doped silicon resonators are able to access a lower second-order TCF and hence a lower total frequency variation over temperature, which is of great benefit for passively compensated frequency references.

Power consumption related to wireless communication in IoT can be reduced by employing frequency references directly at radio frequencies (sub-GHz to GHz range) to remove the need for active frequency generation. MEMS CMRs operating at sub-GHz and GHz resonant frequency levels require a thin device layer, which should be smaller than

the wavelength. Previously reported piezoelectric-on-Si MEMS CMRs have been fabricated from Si-on-insulator (SOI) or cavity-SOI (C-SOI) wafers, where it is challenging or expensive to reduce the thickness of the Si device layer to a few microns with good uniformity around the wafer [9,10]. Moreover, SOI and C-SOI wafers are fabricated using bonding processes where the yield is typically lower compared to the thin-film processes.

This report presents reduced-TCF MEMS CMRs with 900MHz resonant frequencies suitable for RF applications, using a ~2µm-thin doped Si layer formed using the silicon-on-nothing (SON) process [11,12] to achieve a controllable thickness. Subsequent sections describe the resonator design, fabrication process and measured results for these high frequency MEMS CMRs.

II. Resonator Design and Fabrication

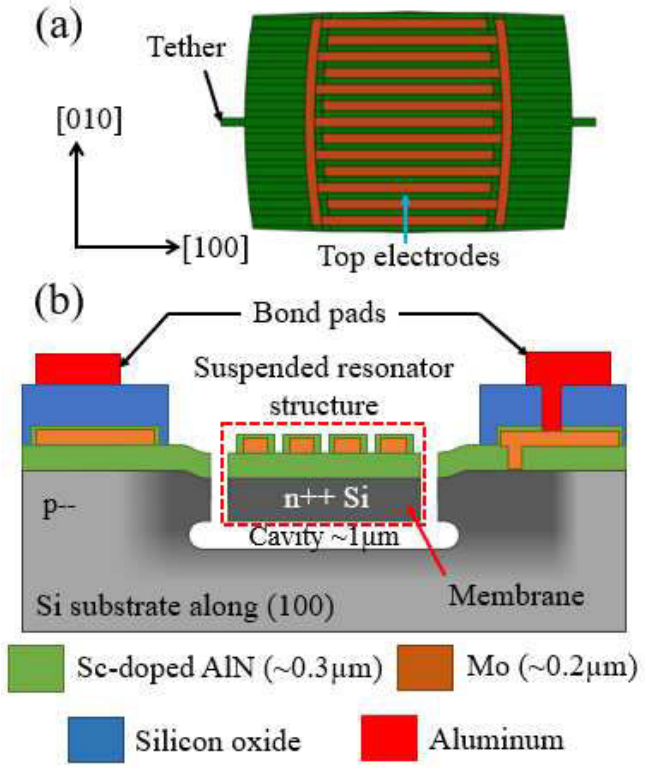

Fig. 1. (a) Top-view schematic showing the suspended portion of the MEMS CMR which consists of a resonator body and a pair of tethers connecting the resonator body to the Si substrate. No passivation layer is shown in the top-view schematic to clearly show the routing of top Mo electrodes; (b) Cross-sectional view of the MEMS CMR shows vertical stack along the suspended area as well as along the anchored area.

Fig. 1a shows a top-view schematic of the suspended section (which includes resonator body and a pair of tethers) of the MEMS CMR and Fig. 1b depicts the cross-sectional view of the CMR. As shown in Fig. 1b, the resonator body has a ~2µm thick degenerately doped n-type pre-released Si membrane that forms the device layer of the CMRs, allowing for reduced TCF. While the highly doped Si layer acts as bottom electrode of the CMRs, top electrodes are formed by patterning a ~0.2µm thick molybdenum (Mo) layer. A ~0.3µm thick scandium (Sc)-doped aluminum nitride (AlN) layer is sandwiched between the top and bottom electrodes and provides necessary piezoelectric transduction. The same piezoelectric layer has also been applied to passivate the top Mo electrodes from oxidation in air. It is worth noting that 15% Sc-doped AlN has been used as piezoelectric as well as passivation layers for this work. A pair of tethers attached to the resonator body connects the resonator to the lightly doped p-type Si substrate. As seen from Fig. 1b, a highly resistive p-n junction is formed between the degenerately doped n-type Si device layer and a high resistivity p-type Si substrate, provides the necessary electrical isolation between neighboring devices. The top view schematic in Fig. 1a does not include any passivation layer so to clearly show the pattern and profile of top electrodes.

Applying an AC electric field between the top and bottom electrodes (across the thickness of piezoelectric layer) excites lateral vibration modes due to the d_{31} coefficient of piezoelectric layer. The center frequency (f_0) of the lateral vibration mode is determined by the period (W_p) of the top electrodes and may be expressed as:

$$f_0 = \left(\frac{1}{W_p}\right)\sqrt{\frac{E_{eff}}{\rho_{eff}}} \quad (1)$$

Here E_{eff} and ρ_{eff} respectively denote the effective Young's modulus and density of the vertical stack of the resonator. The overall length and width of the resonator dictate the motional resistance and static capacitance of the CMR. The variation of f_0 with respect to temperature (T) can be expanded in a power series:

$$f(T) = f_0[1 + TCF_1\Delta T + TCF_2\Delta T^2 + TCF_3\Delta T^3 + \cdots] \quad (2)$$

Note that, we have considered the power series up to 3rd order polynomial. TCF_1, TCF_2 and TCF_3 are respective first, second and third order temperature coefficients of frequency and $\Delta T = T - T_0$ is the difference between the respective operating temperature (T) and the reference temperature (T_0).

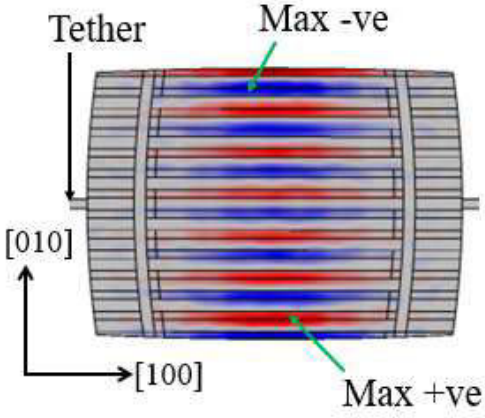

Fig. 2. In-plane displacement profile of a MEMS CMR along [010] as obtained from FE simulations using COMSOL multiphysics. The central axis of the resonator is designed along <100> crystal plane of a (100) single crystalline silicon substrate.

Finite element (FE) simulation using COMSOL Multiphysics was performed to primarily obtain the resonant frequency of the CMRs in accordance to device geometry and period of the top Mo electrodes. The lateral displacement profile associated with the contour modes is shown in Fig. 2. The shape of the resonant body and electrodes were tuned to maximize transduction, reduce parasitic capacitances, while suppressing spurious modes. The vertical stack of the FE model includes bottom Si layer, top Mo electrodes and a Sc-doped AlN layer sandwiched between top Mo and bottom Si layers.

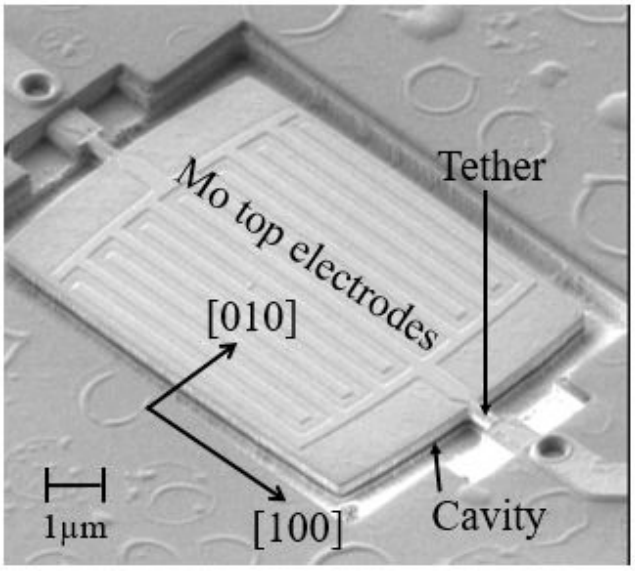

Fig. 3. Scanning electron micrograph (SEM) showing the top view of the fabricated MEMS CMR along <100> crystal plane of (100) single crystalline silicon substrate.

The resonator was fabricated in the piezoelectric over Silicon-on-Nothing (pSON) process [13], which starts with forming a pre-released Si membrane of well-controlled thickness over cavity using the SON process [11,12]. Next the Si membrane is selectively phosphorous-doped to a level of ~5 $\times 10^{20}$ at/cm^3. A 0.3µm layer of 15% Sc-doped AlN was deposited on the degenerately doped Si membrane; this was followed by a 0.2µm Mo layer deposited and patterned to form top electrodes over the piezoelectric layer. A 50nm 15% Sc-doped AlN layer was then deposited as passivation layer to prevent oxidation of top Mo electrodes. The routing layers were then formed with a dielectric silicon oxide layer and aluminum (Al) for the routing and pads. Finally, the Si membrane was etched to define the resonator body. A top-view scanning electron micrograph (SEM) of the fabricated MEMS CMR is depicted in Fig. 3. The fabricated resonator was cut using focused ion beam (FIB). A further SEM was taken around the cut location to verify the thicknesses of respective layers within the designed vertical stack of the resonator. The cross-SEM view around the cut location is revealed in Fig. 4, where the layer thicknesses correspond to the expected thicknesses of each layer in the vertical stack.

III. Measurement Results and Discussions

The fabricated wafer was probed inside a manual vacuum, temperature-controlled probe station with 2-port ground-signal-ground (GSG) configuration. A vector network analyzer (VNA) was used to obtain the S-parameters of the MEMS CMRs. Fig. 5 shows transmission (S_{21}) signal of a MEMS CMR, where a relatively spurious-free resonance peak is observed close to 900MHz.

To obtain TCF of the MEMS CMRs, S-parameters are obtained while varying the temperature inside the probe station under vacuum. The series resonant frequency (f_s) corresponding to each temperature point was recorded from the S_{21} transmission magnitude. The relative change in f_s was determined with respect to 25°C, which is considered as the reference temperature (T_0). The relative change $\Delta f_s / f_s$ was plotted with respect to temperature and the TCF_1 was obtained as shown in Fig. 6.

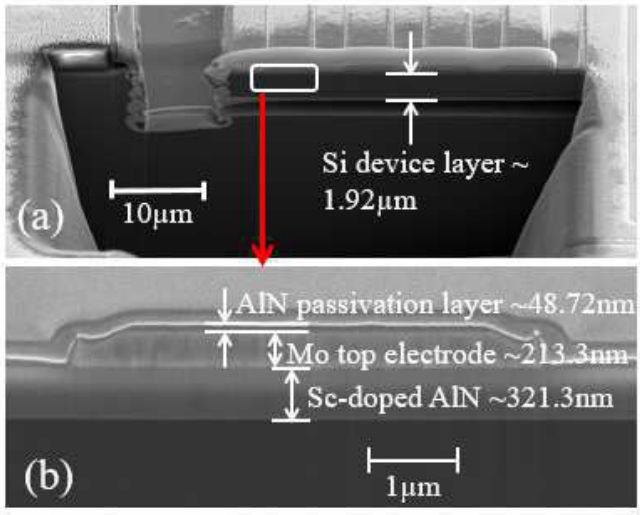

Fig. 4. (a) A FIB-SEM image of a cut across the device showing the thickness of bottom Si layer; (b) Zoomed-in SEM image showing the respective layer thickness of the suspended vertical stack.

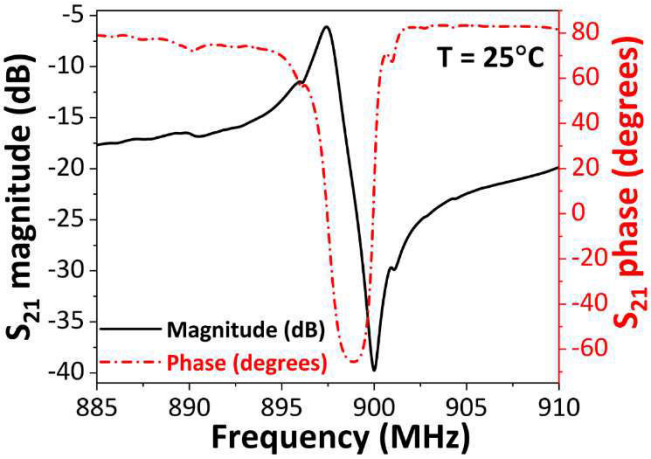

Fig. 5. Measured transmission S_{21} magnitude of the MEMS CMR at 25°C showing a nearly spurious-free resonance.

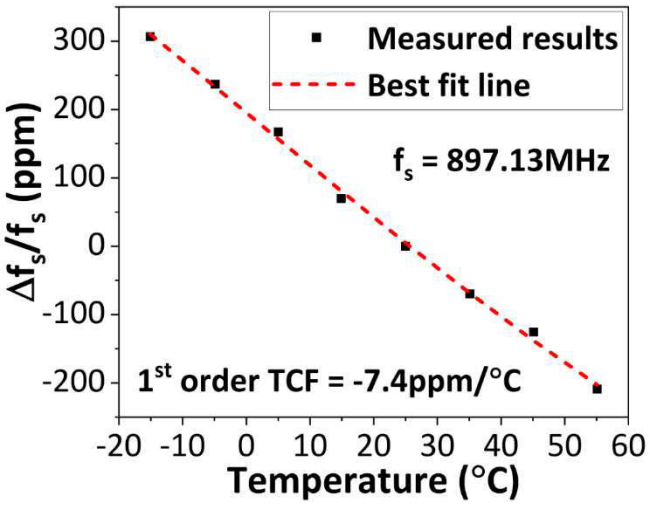

Fig. 6. Variation of series resonant frequency (f_s) with temperature. Fitting the measured values with equation (2) yields a 1st order TCF (TCF_1) of -7.4ppm/°C for the MEMS CMR.

The 1st order TCF value has been reduced significantly as compared to conventional piezoelectric-on-Si resonators. Adjusting the thicknesses of constituent layers in the vertical stack may reduce the TCF further and improve the resonator performance. In addition, the pSON process allows the flexibility to tune the thickness of device layer and provides the benefit of having multiple frequency temperature compensated resonators side-by-side on a single chip. It should be noted that there exist discrepancies between measured and simulated results which is possibly due to the extrapolated material properties.

IV. Conclusion

We have successfully demonstrated high frequency piezoelectric-on-Si reduced TCF MEMS CMRs with 900MHz resonant frequencies, using a ~2µm thick degenerately doped n-type Si device layer. The pSON process, herein, yields thin membranes with well-controlled thicknesses allowing the CMRs to operate at radio frequencies. Degenerate doping of the Si device layer in combination with specific crystal axis alignment and optimized thickness ratios between the constituent layers in the suspended vertical stack has achieved a reduced 1st order TCF of -7.4 ppm/°C. There is room for further improvement in reducing the TCF further by better tuning the device geometry as well as the thicknesses of respective layers.

Acknowledgment

This research was supported by A*STAR under "Nanosystems at the Edge" programme (Grant No. A18A4b0055).

References

[1] J. R. Vig, "Military applications of high accuracy frequency standards and clocks," IEEE Trans Ultrason Ferroelectr Freq Control, vol. 40, pp. 522-527, 1993.

[2] M. Shahmohammadi *et al.*, , "Temperature-compensated extensional-mode MEMS resonators on highly n-type doped silicon substrate," Digests Solid-State Sensors, Actuators, and Microsystems Workshop, p. 371, 2012.

[3] G. Wu *et al.*, "Wafer-level vacuum-packaged high-performance AlN-on-SOI piezoelectric resonator for Sub-100-MHz oscillator applications," IEEE Trans. Ind. Electron., vol. 65, pp. 3576–3584, 2018.

[4] A. Tazzoli *et al.*, "Ultra-high-frequency temperature-compensated oscillators based on ovenized AlN contour-mode MEMS resonators," Digests IEEE International Frequency Control Symposium, p. 327, 2012.

[5] R. Melamud *et al.*, "Temperature- compensated high-stability silicon resonators," *Appl. Phys. Lett.*, vol. 90, art. no. 244107, 2007.

[6] A. K. Samarao *et al.*, "Temperature compensation of silicon micromechanical resonators via degenerate doping," Digests IEEE Int. Electron Devices Meeting (IEDM), p. 1, 2009.

[7] W. Pan *et al.*, "Microelectromechanical resonators having offset [100] and [110] crystal orientations," U. S. Patent 9 090 451 B1, 2015.

[8] A. Jaakkola *et al.*, "Temperature compensated plate resonator," U. S. Patent 9 837 981 B2, 2017.

[9] A. Shchepetov *et al.*, "Ultra-thin free-standing single crystalline silicon membranes with strain control," *Appl. Phys. Lett.*, vol. 102, art. no. 192108, 2013.

[10] O. Elkhatib *et al.*, "Process induced stresses in cavity SOI wafers," *ECS Trans.*, vol. 33, pp. 543–552, 2019.

[11] I. Mizushima *et al.*, "Empty-space-in-silicon technique for fabricating a silicon-on-nothing structure," *Appl. Phys. Lett.*, vol. 77, pp. 3290-3292, 2000.

[12] J. Su *et al.*, "A review: crystalline silicon membranes over sealed cavities for pressure sensors by using silicon migration technology", J. Semicond., Vol. 39, 2018.

[13] J. Sharma *et al.*, "Piezoelectric over Silicon-on-Nothing (pSON) process," unpublished (to be published in IUS2021 proceedings).