3D Stacking of Heterogeneous Chiplets on Modified FOWLP Platform with Thru-Silicon Redistribution Layer

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***Abstract*— A 3D stacking of CMOS on RF device chiplet is demonstrated for significant reduction of areal form factor for Front-End Module (FEM) application. The salient points of the process integration of thru-silicon redistribution layer on the backside of RF device wafer, chip-to-wafer bonding and assembly, measurement of the interconnection and reliability assessment will be discussed.**

Keywords—3D stacking of chiplets, thru-Si RDL process integration, chip-to-wafer bonding, via chain measurement and reliability assessment

I. INTRODUCTION

The use of mobile devices for internet and video communication has been increasing tremendously recently. It is expected that multiple Front-End Modules (FEM) will be required to support the increasing demand growth in wireless connectivity of 5G and beyond. This has driven the need for continuous form factor miniaturization to accommodate additional modules in the limited space of the device. The standard single chip packaging that so far has been running volume production for the bulk of current manufacturing is no longer sufficient to cope and it is under tremendous pressure to change [1,2]. A more cost-effective manufacturable solution is needed to allow more efficient use of the limited space. Instead of the side-by-side configuration of packaged chips currently in use, a 3D stacking of chiplets seems to be a reasonable choice towards that goal [3-5]. We have embarked on work to demonstrate the feasibility of this approach, and we have successfully demonstrated a case whereby CMOS and RF device chiplets are stacked in a 3D configuration, achieving an areal form factor reduction of almost half.

In this paper, a heterogeneous 3D integrated packaging of chiplets built on a modified FOWLP platform with a TS-RDL approach will be described. The salient points of the process integration of TS-RDL on the backside of an RF device wafer, CMOS attachment on RF device wafer by chip-to-wafer bonding (C2W), wafer level mold encapsulation on the C2W assembly, measurement of various via chains, daisy chains and reliability assessment will be discussed. Daisy chain samples have been submitted for reliability assessment after wafer debonding and singulation to verify if there are any major weaknesses that need to be further addressed. Good results have been obtained for both the μ-bump solder joint and the TS-RDL via chains connecting between the CMOS and RF device chiplets.

II. 3D STACKING OF HETEROGENEOUS CHIPLETS DEVELOPMENT

A. Test vehicle package description

The demonstration test vehicle adopted in this work is consists of two chiplets: a CMOS die of 1.39mm x 0.87mm, and an RF device die of 1.56mm x 1.11mm. These chiplets were originally used in otherwise two single-chip packages for side-by-side configuration. They are adopted for the purpose of concept feasibility demonstration and packaging integration processability check and verification. In order to form a vertical interconnection between the RF device and CMOS chiplets, Thru-Silicon Vias (TSV) have been adopted. It is to be processed on the backside of the RF device so that a direct connection to the back of aluminum pads in the RF device can be achieved. This is followed by a redistributed layer (RDL) on the backside of the RF device to form the connection link between the TSV and the I/O bumps on the CMOS which is facing down on the RF device. The assembly is overmolded yielding an overall package thickness of not more than 0.5mm. The RF device is facing down with BGA solder ball attachment for connection to the application board. Fig 1 shows schematic of the proposed 3D stacking of CMOS on RF device configuration.

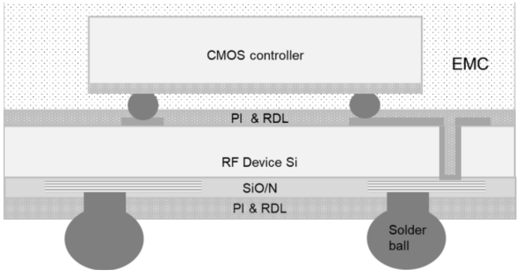


Fig 1: 3D stacking of CMOS on RF device chiplets

B. Wafer levek process integration consideration

The simplified process integration flow is shown in Fig 2. The process flow is a modified process flow from the Fan-Out Wafer Level Packaging platform in IME. The standard baseline materials such as the photo dielectric, temporary bonding adhesive, Cu RDL processes, wafer back-griding, wafer mold encapsulation, etc, are retained. Key features of the integration flow are described below:

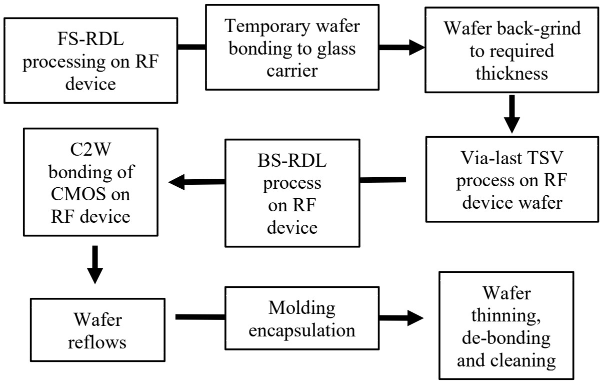


Fig 2: 3D stacking process integration flow of CMOS-on-RF device

- One-layer RDL processing is first carried out on the front-side of the RF device wafer with polymer dielectric passivation as protection layer. An underbump metallization (UBM) is added following the RDL process to ensure stand-off solder joint height control can be made with PCB assembly for a good BGA ball connection without solder bridge issues.
- After the front-side RDL and UBM processing, the RF device wafer is bonded face-down to a glass carrier using temporary adhesive bonding material. The glass carrier is coated with a layer material that allows a laser de-bonding process. This laser de-bonding can provide an almost stress free de-bonding as compared to a mechanical de-bonding method because only minimal physical de-debonding force is needed to separate the bonded wafers after laser application.
- Back grinding is carried out on the backside of RF device wafer bonded to glass carrier to the desired thickness in the silicon substrate.
- Via last TSV process is carried out on the backside of the thinned RF device wafer. After TSV via etching on silicon, low temperature liner oxide deposition is carried out followed by oxide etching on the via bottom for contact exposure to the Aluminum (Al) pad. This is followed by Ti-Cu seed layer PVD sputtering to ensure sidewall and via bottom contact to the Al pad are made.
- Electro-conformal plating is carried out on the backside of the RF device to form a TSV sidewall, via contact to Al pad, and the RDL layer all in one single electroplating step. Finally a dielectric film lamination process fills up the remaining via space in the sidewall plated TSV and then a top surface RDL layer is formed.

This is not a first time we have done such a Thru-Si RDL process but it is a deviation from standard FOWLP processes [3,4]. Some risks are involved, and using FIB-SEM and daisy chain measurements, we have been monitoring the quality on the TSV formation, the sidewall liner and Cu thicknesses, and the contact at the bottom being formed properly. Also we need physical inspection on bonded wafers and that the bonding adhesive will not have adverse effects such as bubble formation, warpage or crack issues when subjected the process integration.

- After the backside UBM process, the wafer processing is considered completed and it is ready for performing CMOS on RF device stacking, reflow, mold encapsulation, wafer back-grinding to the final package thickness and wafer de-bonding.

C2W bonding for the tiny CMOS dies on the RF device wafer can be a very challenging task. A high-speed pick and place tool will be needed for cost effective manufacturing consideration. Also, the use of long staging no clean flux material is required for the long duration of C2W bonding (this can take up to few hours per wafer) which is followed by a solder reflow process. This is the potential area where we will need a higher throughput P&P tool for a high volume manufacturing environment.

III. EVALUATION APPROACH

A few evaluations have been carried out in the work to study the feasibility, processability and material compatibility of the proposed design structure for a stacked CMOS chip on RF device wafer package.

- Initially short loop RF device wafers were employed to check if the wafer bonding on glass, back-grinding, TSV etching and RDL process exposures had any adverse effect on the functionality of the RF device. This has been carried out. Wafer probing and test characterization were used to check if there was any performance deviation as a result of the process exposure and only minimal changes were seen.
- The processing of TSV and subsequent RDL and C2W assembly on the thinned bonded wafer are new to the FOWLP platform. Some module developments have been carried out to identify potential issues and establish the process integration using dummy silicon wafers as well as short loop RF device wafers.

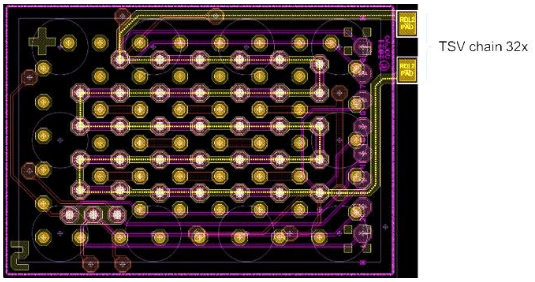


Fig 4a: TSV chain structure

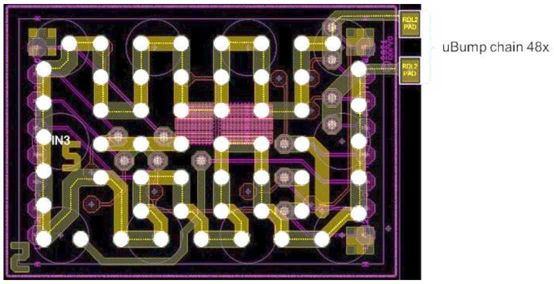


Fig 4b: Micro-bump chain structure

- Various combinations of design structures including daisy chains and via chains of μ-bumps and TSVs between the CMOS and RF device have been created. Such designs proved to be very useful for checking and verifying the process and materials set up. Reliability tests have been conducted on the packaged sample including MSL and TC to catch any weak connections or structure in the stacked chip package and allow changes or improvement to be made.
- Finally full flow CMOS and RF device wafers are processed through the established process integration and materials set for sample build and final test verification.

IV. RESULTS AND DISCUSSION

A. Wafer exposure to short loop process integration

A few RF device wafers have been subjected to the RDL process, wafer bonding, back-grinding to the desired thickness, and exposure to TSV process conditions (e.g. high vacuum exposure in the PVD, photo dielectric curing, etc). The testing results on these wafers are very encouraging. There is no indication that these process exposures have caused degradation or adversely affected the performance of the RF device.

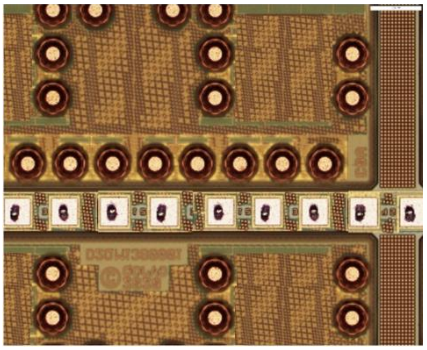


Fig 5a: Frontside of RF device wafer after de-bonding step from initial processes exposure evaluation

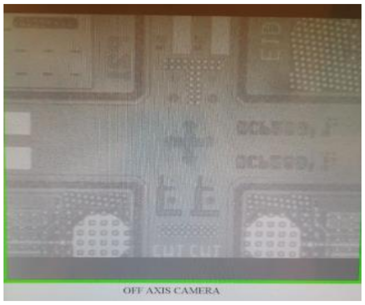


Fig 5b: IR image checking on litho tool from backside of RF device

The optical image of the de-bonded RF device wafer after the back-grinding, TSV and RDL process exposure shows there is no physical abnormality (Fig 5a). IR imaging is taken on a litho tool to verify it is cleared for backside litho processing (Fig 5b).

This is a very critical initial check in which the results have shown good feasibility of the process integration on the device wafer and therefore the work could proceed to the full demonstration.

B. TSV formation on backside of thinned RF device wafer

DRIE etching process development has been carried out initially on dummy silicon prior to implementing on RF device wafers. The sidewall profile has to be checked to ensure sufficient step coverage can be achieved in subsequent liner oxide and seed layer deposition. TSV via landing has no Si notching or Si under etch issues. As the TSV etching process is a time-controlled process it requires a good wafer thickness TTV control from back-grinding process to ensure via landing uniformity (Fig 6). The oxide etching must be controlled to prevent excessive over etch on the Al pad or under etch that prevents good contact to it. FIB-SEM is used extensively to check on the wafer center and wafer edge region for uniformity across wafer. Final verification is done after Cu plating with TSV via chain connectivity measurement between the backside of the RF device and the Al pad chain in the frontside, and Xray imaging to check for TSV to Al pad alignment (Fig 7).

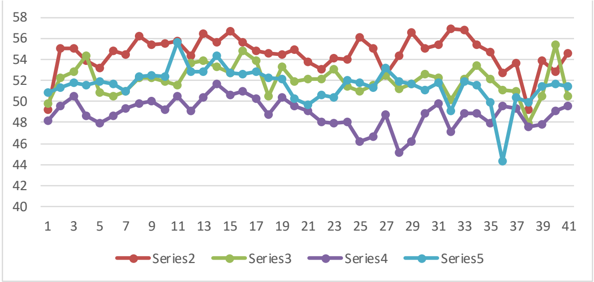


Fig 6: wafer TTV measurement after back-grinding

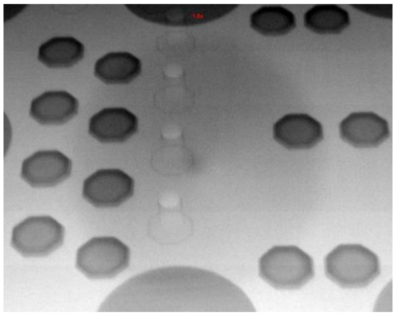


Fig 7: X-Ray show TSVs are well aligned with Al pad

C. Thru-Si RDL process

After seed-layer deposition on the TSV via, a photo-resist pattern layer is formed on the backside of RF device. An electro-conformal plating is carried out to increase the Cu layer thickness from via contact on Al pad at the bottom of TSV to the sidewall of TSV, and finally to the top surface of the backside of the RF device, to complete RDL distribution layer.

This is achieved in one single plating step using a well established RDL plating process. Optical and X-Ray inspection can be carried out to check for plating unformity and TSV via chain resistance measurements are employed for via contact verification across the wafer (Fig 8).

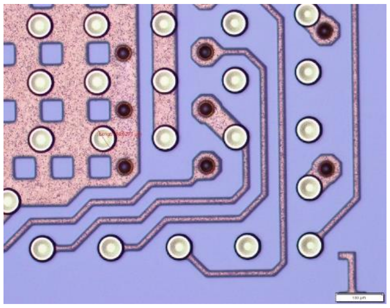
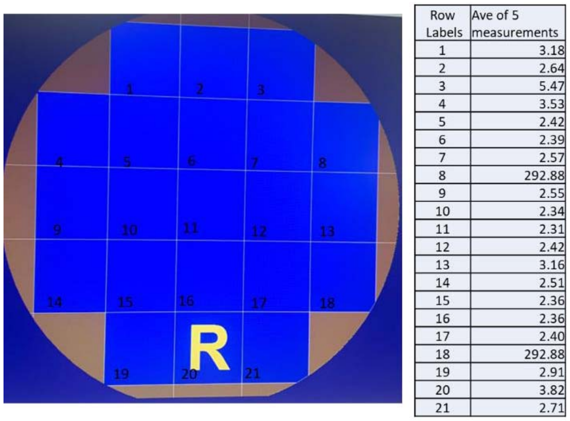


Fig 8a: Thru-Si RDL layer on the backside of the RF device



Row Labels	Ave of 5 measurements
1	3.18
2	2.64
3	5.47
4	3.53
5	2.42
6	2.39
7	2.57
8	292.88
9	2.55
10	2.34
11	2.31
12	2.42
13	3.16
14	2.51
15	2.36
16	2.36
17	2.40
18	292.88
19	2.91
20	3.82
21	2.71

Fig 8b: TSV via chain measurements (unit: Ohm) for different reticle locations on the RF device wafer

D. *Chip-to-wafer bonding*

C2W bonding starts with pick and place of the bumped CMOS chip on the RF device wafer backside with UBM finished. The tiny size of CMOS chip required a well-designed pick up tool and process control to ensure proper pick & place and minimize flying chip problems. Solder joint quality can be improved by reducing dishing on the UBM and by proper fluxing.

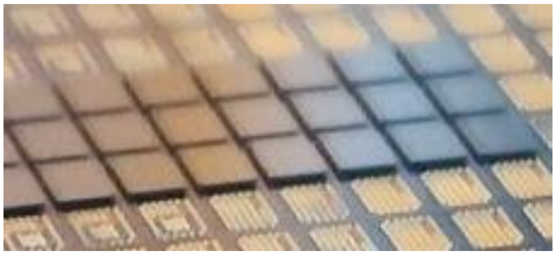


Fig 9: After C2W bonding of CMOS chiplets on the RF device wafer back side.

Quality checks on the C2W bonding process are done by cross-section to determine if solder bump formation is correct and whether there are any solder bridging issues. Solder voids are found on initial samples having dishing on UBM. These were resolved easily on subsequent wafer lots with improved UBM plating (Fig 10).

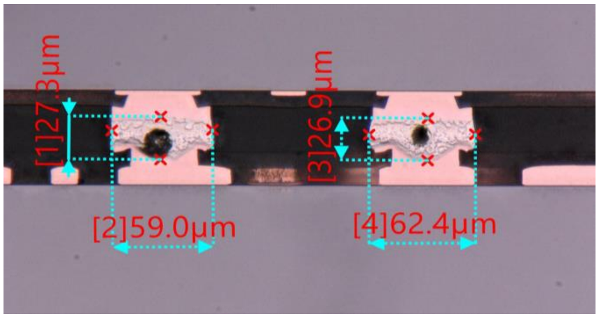


Fig 10a: Cross-section of solder joint after C2W and reflow

Fig 10b: RHS: Improved UBM plating with lower dishing

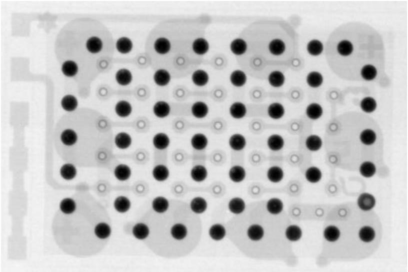


Fig 10c: X-Ray on C2W with improved UBM dishing

After C2W bonding, daisy chain resistance measurements are performed on the various test chip designs. This allows a more comprehensive connectivity check on the μ-bump chains, PI via chains, RDL chains, TSV via chains, and some kelvin test structures. It has been very useful to have these chips to verify each layer of connectivity in the 3D stacked chip structure. Fig 11 shows typical results of these measurements.

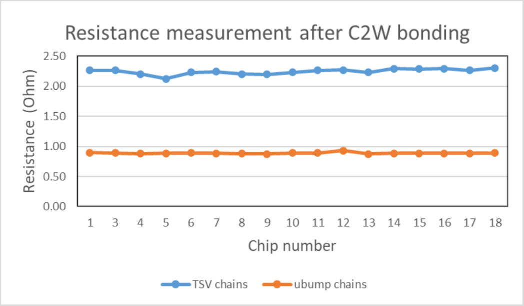


Fig 11a: TSV chain and µ-bump chain resistance measurements after C2W and reflow

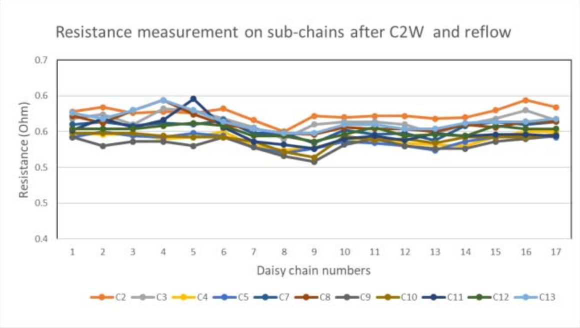


Fig 11b: Daisy chain resistance measurements on other test chips after C2W and reflow

E. *Wafer encapsulation and solder ball assembly*

After the molding process, wafer backgrinding to the final thickness can be performed. Then the wafer assembly can be de-bonded, cleaned, and receive solder ball placement to complete the assembly process.

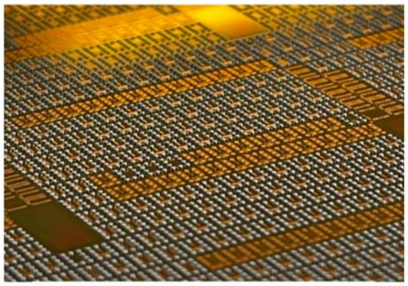


Fig 12a: After wafer level solder ball placement

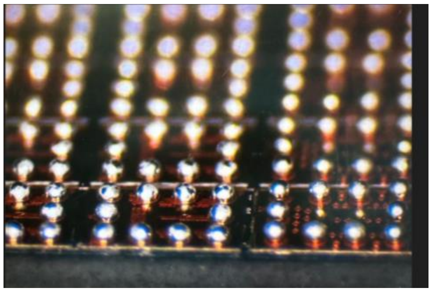


Fig 12b: After solder ball placement and dicing

F. *Reliability assessment*

A quick reliability assessment has been carried out by subjecting the stacked package with various design chips to Moisture Sensitivity Level 3 and Thermal Cycling (-40/+125 degree C) testing. This allowed a good check on package integrity and identifying any obvious weakness in the connectivity, materials and structures. Please note that there are via chains, TSV chains, µ-bump chains and kelvin structures on these samples built with the CMOS and RF device chiplets. A total of 60 units of these stacked packages have been tested and 100% of them have passed. We plan to continue the testing further for checking its robustness.

V. CONCLUSIONS

The feasibility of a 3D stacking of heterogenous (CMOS, RF device) chiplets has been successfully demonstrated. The process integration of a modified FOWLP platform by using Thru-Si RDL and solder bump for interconnection between the top and bottom chiplets has been achieved. The key processes, quality inspection, connectivity measurements, and quick reliability tests have all shown very encouraging results.

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