A Novel Method for Air-gap Formation around Via-Middle (VM) TSVs for Effective Reduction in Keep-Out Zones (KOZ)

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Abstract—**Significant stress is induced in the crystalline Si area around a Cu-filled Through Silicon Via (TSV) due to the large mismatch in the co-efficient of thermal expansion (CTE) between Si and Cu. As a result, CMOS devices fabricated within the stressed Si region will show undesired variations in their electrical performance. This paper reports a novel method to isolate the TSV-induced stress from active CMOS devices through the formation of embedded air-gaps. As the air-gaps are embedded in the Si, stress isolation can be done without compromising on the usable Si area. Formation of the air-gaps have been demonstrated experimentally using a high temperature anneal in a de-oxidizing ambient. Stress reduction in the Si lattice, in the presence of the embedded air-gaps, will be studied through thermo-mechanical stress simulation. Effect of the impact of air-gap design will also be discussed.**

Keywords- Air-gap, Via-Middle, Through Silicon Via (TSV), Stress, Anneal.

I. INTRODUCTION

The advent of 3D IC integration brings about many benefits including small form-factor, reduced power consumption and higher data bandwidth [1]. Through-Si-Via (TSV) is an essential building block for the realization of 3D IC integration. However, apart from the immense benefits TSV brings, there are also problems and issues that come with it. Large mismatch between the thermal expansion coefficient (CTE) of Cu and Si introduces high stress in the Si area surrounding each Cu-filled TSV. This in turn modifies the Si bandgap and transport properties of carriers in bulk Si. As a result, the device performance of logic CMOS transistors, in the vicinity of a TSV, will deviate from its intended specification. In view of this, a keep-out-zone (KOZ) is defined, around each TSV, within which no active logic devices should be placed. This results in a reduction in active Si area which in turn relates to higher cost. To reduce the TSV keep-out-zone (KOZ), some reports have suggested isolating the TSVs by etching trenches around them and filling these trenches with dielectric or polymers [2], [3]. However, although the size of TSV keep-out-zone (KOZ) has been reduced, these isolating trenches themselves still take up usable Si area on the chip.

In this paper, we report a novel method to embed air-gap within the Si substrate to mechanically and electrically isolate TSVs from surrounding active devices. This is done by first patterning and etching vias / trenches around each TSV, followed by a high temperature anneal process to seal up the etched vias / trenches. As a result, air-gaps are formed inside the Si substrate. The presence of these air-gaps can reduce the area of the KOZ, thus 'freeing up' more space for active logic devices. In addition, unlike other methods of forming air-gaps using dielectrics, the Si area on top of these air-gaps can still be used for other passive Si devices. This process of forming air-gap is also relatively simpler and more cost effective as less processing steps are involved.

Section II of this paper describes the concept of the air-gap formation and how it can be integrated into a conventional Via-Middle (VM) TSV process flow. Feasibility of this concept will be demonstrated. Lastly, design of the air-gap on the impact of the stress around the TSV will be investigated via thermal mechanical modeling in Section III.

II. CONCEPT AND PROCESS FEASIBILITY

Large mismatch between the thermal expansion coefficient of Cu and Si can induce significant stress levels in the Si channel of logic CMOS devices [3]–[5]. This alters the band-gap and mobility of the carriers in the Si channel, resulting in undesirable fluctuations in device performances of CMOS logic chips. The induced stress propagates through the Si crystal, decreasing with distance away from TSV [5]. This defines a keep-out-zone (KOZ) region, within which no active devices should be placed. The extent of this TSV keep-out-zone (KOZ) can be significantly reduced by means of adding a barrier to truncate the propagation of stress through the Si crystalline structure. This paper reports an alternative method to terminate the stress propagation in the Si crystalline structure by the removal of Si to form an air-gap.

A detailed description of the air-gap formation process flow is given in Figure 1. Vias / trenches are first patterned to define the desired position of the air-gaps. Dry plasma etching process is then used to etch the trench or via to the required depth. Next, the etched trenches and vias are then subjected to a high temperature annealing process to allow the migration of Si to seal up the open trenches and vias. As a result, air-gaps are formed in the bulk Si, defined by location of the trench or via during patterning. Figure 2 illustrates the cross-section schematic of how the air-gap is embedded within the Si substrate. Compared to other methods of isolating stress (by etching trenches and filling up with other materials), this method of forming air-gaps to isolate induced stress is relatively simpler and more cost-effective. The Si area on top of the air-gap can also be used for other Si devices where performance is not affected by stress. As a result, this

helps to increase the active Si area on the chip, enabling a smaller foot-print and lower cost.

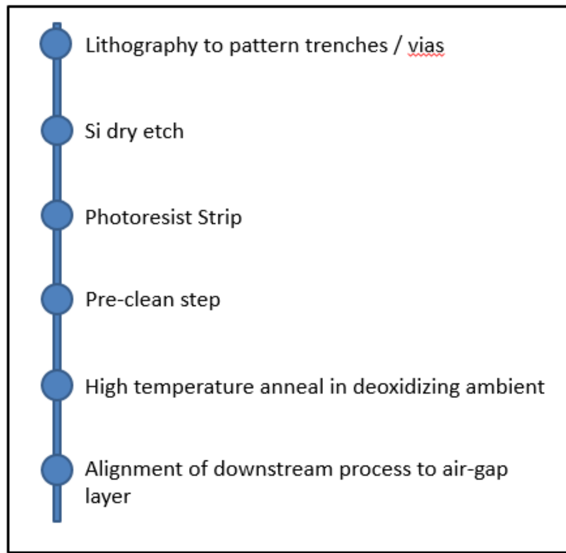

Figure 1 : Detailed description of the process sequence for the formation of air-gap in bulk Si.

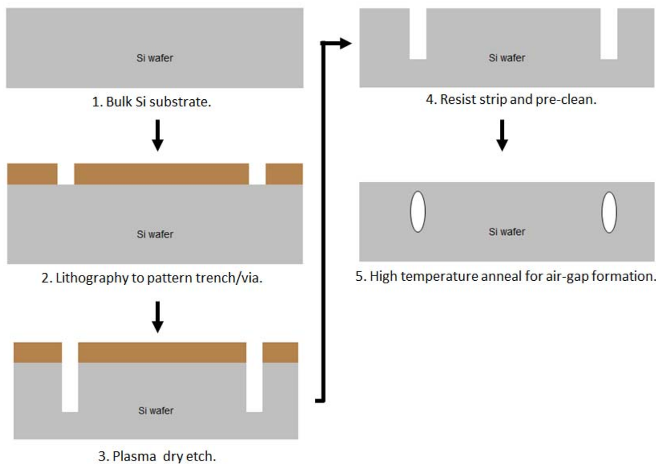

Figure 2 : Cross-section schematic illustration on formation of air-gap in Si.

A process feasibility study has been carried out on 200mm Si wafers. Arrays of vias with different via dimensions and spacings are patterned using a 248nm scanner. Concurrently, alignment marks with 100µm widths are patterned on the same masking layer. Plasma dry etching is then performed to etch vias to depths of around 4µm. Figure 3(a) shows the DRSEM images of the different arrays of etched vias. A pre-clean treatment is done before subjecting the etched wafers to annealing at 1100^{0}C in a de-oxidizing ambient. During annealing, the Si near the wafer surface will migrate to fill up the etched openings to minimize surface energy [6]. From Figure 3 (b), it can be clearly seen that via openings have been sealed up after anneal. Figure 3 (c) and (d) shows a magnified image of a specific via array with 200nm dimension and 600nm spacing before and after anneal respectively. Similarly, it can be observed that the etched vias on the wafer was sealed and covered up as a result of the high temperature anneal process. In addition, the surface of the sealed array of vias was studied using atomic force microscopy (AFM) and found to be flat with reasonable surface roughness of less than 20Å (Figure 4).

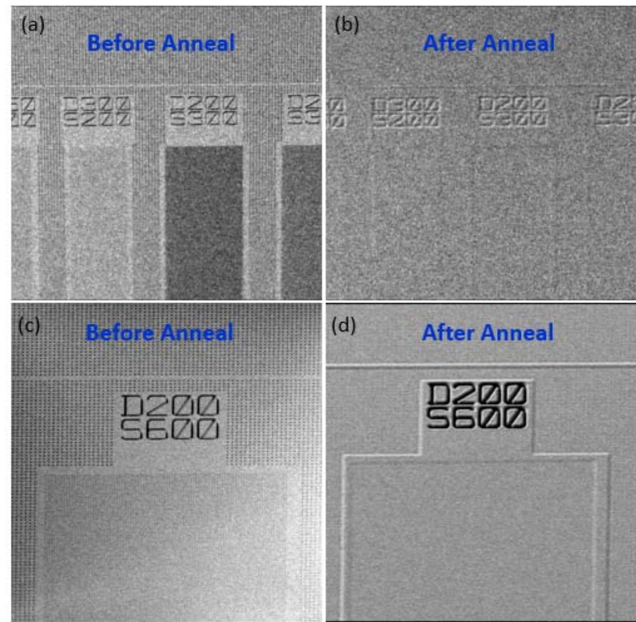

Figure 3 : (a) Different arrays of etched vias before annealed. (b) Etched vias have been sealed up, implying the formation of air-gap, for all the different via arrays of varying critical diemnsion and spacing. (c) Larger magnification image of etched vias with 200nm CD and 600nm spacing before anneal, (d) Larger magnification image of etched vias with 200nm CD and 600nm spacing after anneal.

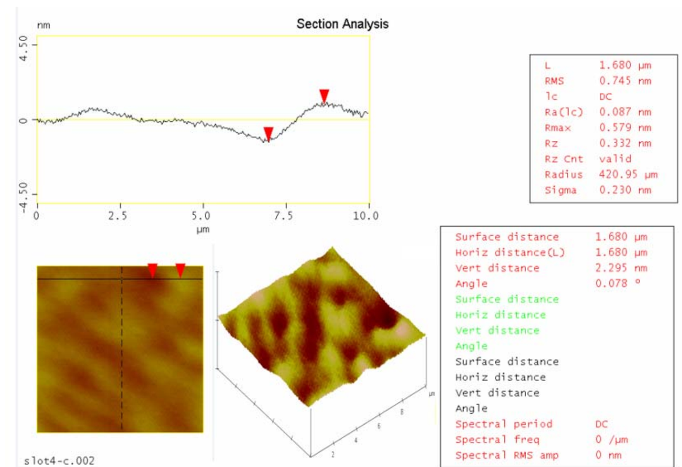

Figure 4 : Atomic Force Microscopy (AFM) analysis performed on Si surface after high temperature anneal to seal up the open vias. Reasonable surfacer roughness with a RMS value of less than 20Å is obtained across a 1.68µm x 1.68µm scanned area.

The cross-section SEM image of a via array before and after the high temperature anneal is as shown in Figure 5 (a) and (b) respectively. Transmission Electron Microscopy

(TEM) was performed at the Si region on top of the embedded air-gap to investigate its crystallinity. It can be seen that the Si region on top of the air-gap is crystalline with no observed defects. The diffractogram (Figure 5 (c) insert) derived from the Si region (depicted in yellow box) in the TEM image further verified that the layer of Si above the air-gap is crystalline and suitable for the fabrication of Si devices.

Structures, with larger feature size, however are not affected by the annealing step. For example, alignment mark structures, as seen in Figure 6, remain unchanged and visible even after air-gap formation. This is because Si migration for air-gap formation are only limited to vias / trenches with small feature size. From our study, via or trench openings with the smallest physical dimension of more than 1µm will remain as openings. Therefore, this allows for the alignment of the air-gap layer to subsequent downstream lithography processes.

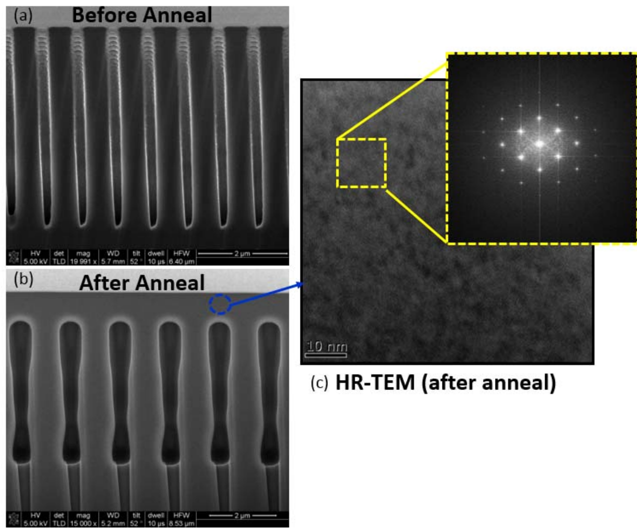

Figure 5 : (a) DRSEM cross-section after Si via etch. (b) DRSEM cross-section after high temperature anneal, Air-gaps are formed as a result of the sealing up of the openings of the etched vias (c) TEM was done to confirm the Si quality and crystallinity (diffractogram in inset).

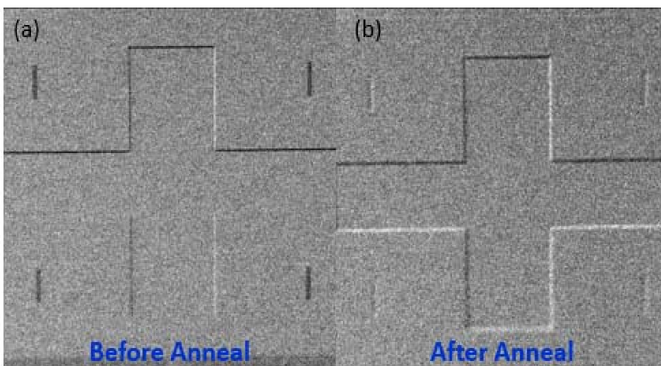

Figure 6 : DRSEM image of 100mm x 100mm alignnment mark (a).before high temperature anneal and (b) after anneal. In contrast, columns of open vias placed at the 4 corners of the mark have almost been sealed up and flattened.

III. Mechanical Stress Modeling Analysis

Large CTE mismatch between Cu and Si can induce significant stress in the Si lattice around a Cu-filled TSV. This paper proposes the formation of the embedded air-gap, discussed in Section II, to minimize the outward propagation of stress through the crystalline Si lattice from the TSV. With regards to process integration, the air-gap can be formed before TSV formation. TSV lithography can be aligned to the air-gap layer because alignment mark will not be affected by the high temperature annealing step during air-gap formation. A cross-section schematic of the proposed integration flow is as depicted in Figure 7.

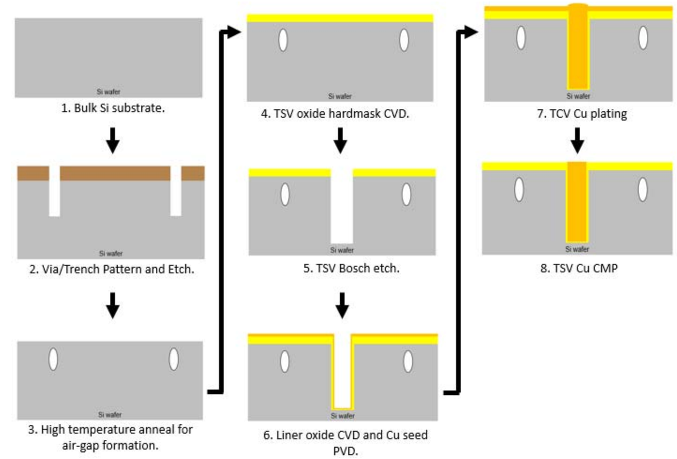

Figure 7 : Proposed flow to integrate air-gap with TSV. After air-gap formation, TSV oxide hardmask is deposited by CVD process. TSV is then patterned and aligned to the air-gap layer. This is followed by Si Bosch etch, liner oxide CVD and Cu seed PVD. Cu electroplating is used to fill the TSV before finally undergoing Cu CMP to remove the overburden.

Finite element thermo-mechanical stress simulation using ABAQUS software is employed to investigate and validate the effect of an additional air-gap embedded around the Cu TSV. An illustration of the proposed simulation schematic is given in Figure 8. In this model analysis, a 10µm x 50µm TSV, lined with SiO2 and filled with Cu is used. The size (height) of the air-gap, h and its depth from the Si surface, y, are varied while keeping its distance from the edge of the TSV, x fixed.

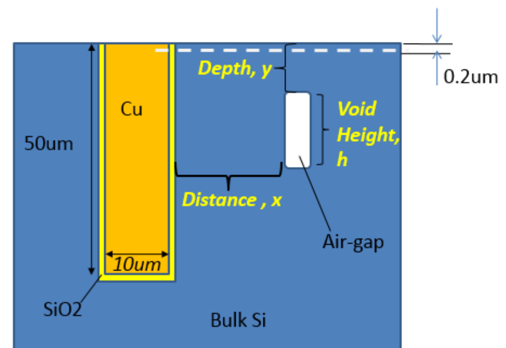

Figure 8 : Schematic of proposed structure used in the stress simulation The structure consists of a 10µmx50µm Cu-filled TSV with an air-gap adjacent to it. Depth of the air-gap (y) and size (height) of the air-gap are varied while keeping distance (x) costant.

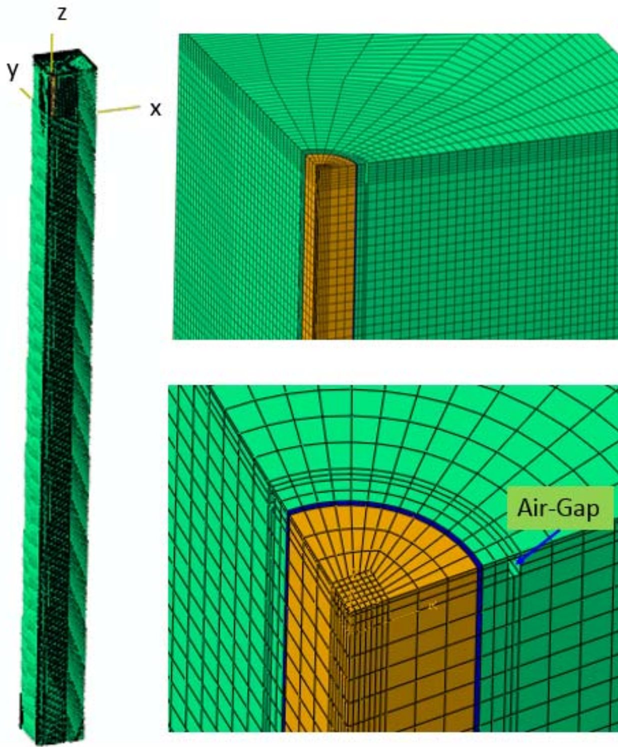

Figure 9 : Final simulated structure (with meshing) used in the thermo-mechcanical stress analysis. Finer mesh is defined for Si (in green) closer to the edge of Cu TSV (in orange) as the stress profile tends to be more likely to show larger spatial stress variation.

The final simulated structure used in the stress analysis is as given in Figure 9. The Cu TSV is represented by the orange region while the green region denotes Si. The oxide liner (given by the thin blue region) has also been incorporated in the model. In cases where air-gaps are present, they are placed at a distance of 1µm from the TSV edge (bottom right hand picture). All 1D stress profiles are taken at a depth of 0.2µm from the surface. Figure 10 shows the comparison of the 1D vertical stress (σ_{yy}) profiles with air-gaps positioned at different depths from the Si surface (0.1µm and 0.2µm). It can be observed that, with the air-gap, vertical stress is reduced in both cases. Assuming a keep-out-zone (KOZ) of 5µm from the edge of TSVs, the implementation of the air-gap will result in an almost negligible KOZ. In addition, as the air-gap moves closer to the Si surface, this reduction in σ_{yy} increases. This implies that position of the air-gap from the surface plays a role on the vertical stress reduction.

The 1D lateral stress (σ_{xx}) profiles with air-gaps at different depth from Si surface is depicted in Figure 11. The induced lateral stress (σ_{xx}) is tensile in nature and similarly observed to be reduced in the presence of an air-gap. Like in the case of σ_{yy}, reduction in σ_{xx} increases with decreasing distance of air-gap from the Si surface. However, a sudden increase in σ_{xx} is observed in the Si region between the TSV edge and air-gap. σ_{xx} starts to drop below the reference (without air-gap) only beyond the position of the air-gap. This observation could be, as a result of the air-gap, due to the lack of Si for the effective propagation of stress. This caused the built-up of stress accumulated at the Si region between the TSV and the air-gap.

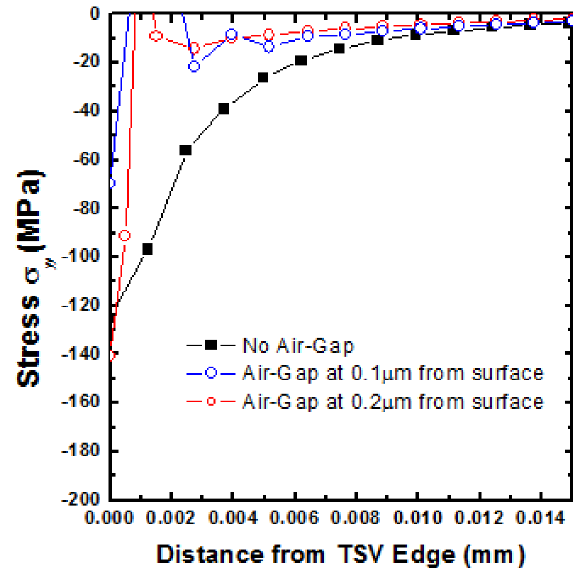

Figure 10 : Compressive stress in vertical direction, σyy, decreases with increasing distance from TSV. The closer the air-gap to the Si surface, the greater reduction in vertical stress.

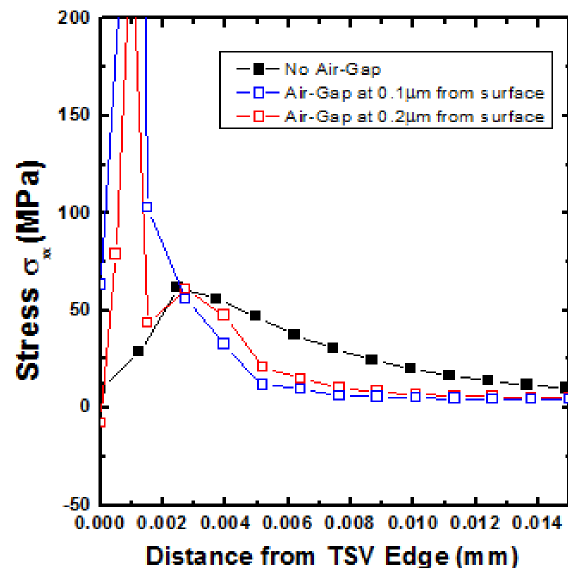

Figure 11 : Tensile stress in the lateral direction σ_{xx}, decreases with increasing distance from TSV. The closer the air-gap to the Si surface, the greater reduction in lateral stress.

Next, we analyze the impact of the air-gap size (height) on the propagation of vertical and lateral stress around the TSV. Air-gaps with different sizes (heights) of 1µm, 5µm and 10µm are included in the stress modelling to understand how σ_{xx} and σ_{yy} will vary. Figure 12 shows the vertical stress σ_{yy} induced in the Si starting from the edge of a Cu-filled TSV. Similarly, the addition of an air-gap around the TSV is found to decrease σ_{yy}. And the larger the size of the air-gap, the larger the reduction in σ_{yy}. An air-gap of about 1µm around the TSV have little effect on the reduction of the induced vertical stress, σ_{yy}. On the other hand, a larger air-gap of >3µm height can result in a much more significant drop in σ_{xx}. This implies that detailed design (in terms of via size

/spacing and annealing condition) is required to achieve an optimal stress reduction in the Si lattice around the TSV. The impact of the air-gap size (height) on the lateral stress, σ_{xx} profile is illustrated in Figure 13. Again, it is observed that a larger air-gap size causes an increased reduction in σ_{xx}.

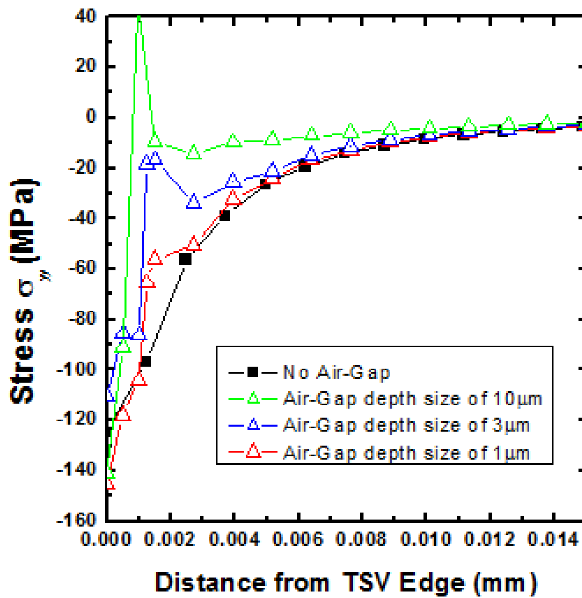

Figure 12 : Compressive stress in vertical direction, σ_{yy}, as a function of distance from TSV edge for air-gap of different depth sizes (10µm, 3µm and 1µm).

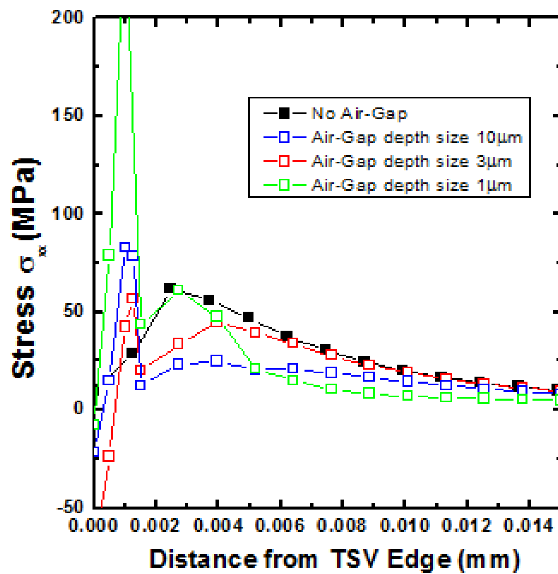

Figure 13 :: Tensile stress in the lateral direction σ_{xx}, as a function of distance from TSV edge for air-gap of different depth sizes (10µm, 3µm and 1µm).

CONCLUSION

A simple and novel method to isolate the stress induced in the Si around Cu-filled TSVs is discussed. Air-gaps can be embedded in the Si around the TSVs. This is done by first patterning and etching vias / trenches into the Si around each TSV. The vias / trenches are then annealed at high temperature in a de-oxidizing ambient. By Si migration process, the openings of the vias / trenches will be sealed up to form air-gaps. Compared to conventional method of using polymer or dielectric to fill up the vias / trenches, this method frees up more Si area for devices where their electrical performances are not sensitive to stress effects. Formation of the air-gaps have been demonstrated and verified by experimental data. Large structures like alignment marks are not affected by the anneal process, allowing for alignment with subsequent downstream process. Through thermo-mechanical stress modeling, formation of air-gaps around TSVs is shown to result in significant stress reduction in both the vertical and lateral directions, σ_{yy} and σ_{xx}. However, process optimization in the design and formation of the air-gap is required to achieve optimum reduction in stress and KOZs around each TSVs.

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