

An Integrated Wireless Power Management and Data Telemetry IC for High-Compliance-Voltage Electrical Stimulation Applications

Jianming Zhao, *Student Member, IEEE*, Lei Yao, *Member, IEEE*, Rui-Feng Xue, Peng Li, Minkyu Je, *Senior Member, IEEE*, and Yong Ping Xu, *Senior Member, IEEE*

Abstract—This paper describes a 13.56-MHz wireless power recovery system with bidirectional data link for high-compliance-voltage neural/muscle stimulator. The power recovery circuit includes a 2-stage rectifier, 2 LDOs and a high voltage charge pump to provide 3 DC outputs: 1.8 V, 3.3 V and 20 V for the stimulator. A 2-stage time division based rectifier is proposed to provide 3 DC outputs simultaneously. It improves the power efficiency without introducing any impact on the forward data recovery. The 20 V output is generated by a modified low ripple charge pump that reduces the ripple voltage by 40%. The power management system shows 49% peak power efficiency. The data link includes a clock and data recovery (CDR) circuit and a load shift keying (LSK) modulator for bidirectional data telemetry. The forward and backward data rates of the data telemetry are 61.5 kbps and 33.3 kbps, respectively. In addition, a power monitor circuit for closed-loop power control is implemented. The whole system has been fabricated in a 24V HV LDMOS option 1.8 μ m CMOS process, occupying a core area of around 3.5 mm².

Index Terms—Rectifier, CDR, charge pump, wireless power, stimulator.

Jianming Zhao is with the Department of Electrical and Computer Engineering, National University of Singapore, 117576 Singapore. He is also with Institute of Microelectronics, Agency for Science, Technology and Research, Singapore (e-mail:zhaojianminghit@gmail.com).

Lei Yao and Peng Li are with the Institute of Microelectronics, Agency for Science, Technology and Research, Singapore (e-mail:yaol@ime.a-star.edu.sg).

Rui-Feng Xue is with the Philips Research China, Shanghai, China (e-mail:Ruifeng.Xue@philips.com).

Minkyu Je was with Institute of Microelectronics, Agency for Science, Technology and Research, Singapore. He is now with Department of Information and Communication Engineering, Daegu Gyeongbuk Institute of Science & Technology, Daegu, Korea (e-mail:minkyu.je@gmail.com)

Yong Ping Xu is with Department of Electrical and Computer Engineering, National University of Singapore, 117576 Singapore, (e-mail: yongpingxu@nus.edu.sg).

This work is supported in part by Agency for Science, Technology and Research SERC (Science and Engineering Research Council) TSRP iNPBi 102152 0013 and in part by A*Star SERC BMRC (Biomedical Research Council) 13302FG060, Singapore. The scholarship from Economic Development Board (EDB) Singapore.

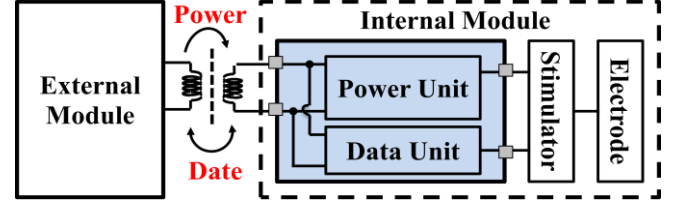


Fig. 1. Diagram of a wireless implantable stimulator.

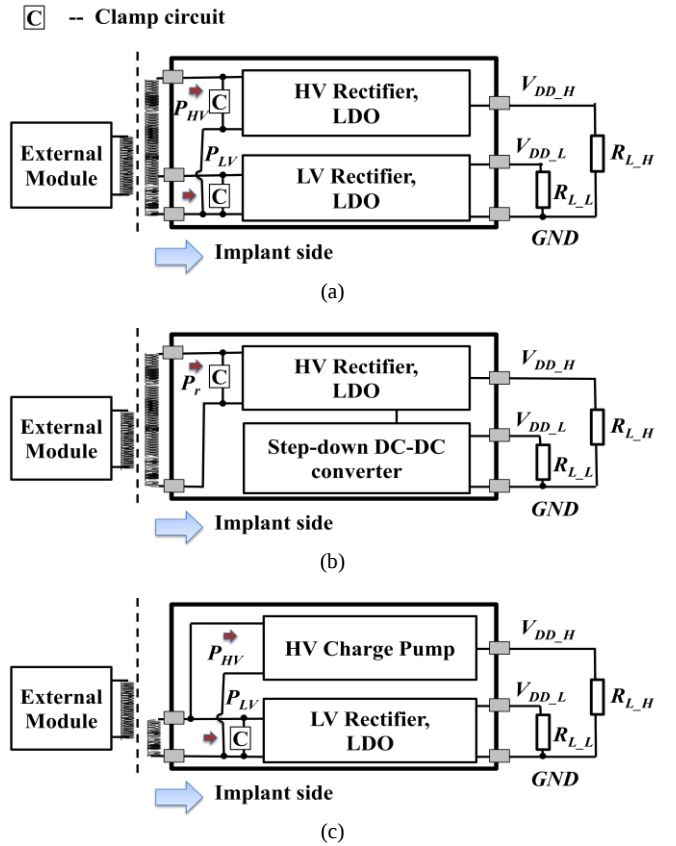


Fig. 2. Illustration of power management system architectures to generate both high and low voltage supplies through coupling coils: (a) architecture in [4,5], (b) Architecture in [6] and (c) architecture in [7-10].

I. INTRODUCTION

IMPLANTABLE stimulator systems have been used in biomedical applications, such as retinal prosthesis [1], pain

control [2] and functional electrical stimulation [3]. In these applications, stimulator with wireless power/data transmission is preferred, as it avoids wound infection caused by power/data wire through the skin. High voltage compliance is usually required in order to deliver sufficient stimulation current to the electrode [4,5]. Fig. 1 shows the diagram of a typical wireless stimulator system. It includes an internal and an external module. The internal module consists of a stimulator, power and data recovery circuit. The external module provides the power and data for the internal module through a wireless link, a pair of mutual-coupling coils.

Several wireless multi-voltage power modules have been reported for high-voltage-compliance stimulator. In general, they can be divided into two categories. In the first category, the secondary coil supplies high voltage (HV) to the power management circuits. Thus the HV output can be obtained via a HV rectifier and a LDO regulator. The low voltage (LV) output can be derived from either an additional coil or from LV tap in the secondary coil, as shown in Fig. 2(a) [4,5]. In this case, the power efficiencies of HV and LV circuits cannot be simultaneously optimized since the required amounts of power on HV and LV circuits are not proportional but the configuration of coil is fixed after implantation. To overcome this, a step-down charge pump can be used to supply LV output [6], as shown in Fig. 2(b). In the second category, the secondary coil only provides LV output. Thus, the LV output can be easily obtained through a LV rectifier and a LDO regulator, while the HV output needs a step-up DC-DC converter, as shown in Fig. 2(c) [7-10].

Depending on the distance of the coupling coils and the loading conditions, the voltage from the secondary coil may fluctuate in a wide range, and cause circuit failure. A clamp circuit is usually required to protect the power management

circuit as the voltage goes excessively high. It provides a leakage path whenever the coil voltage exceeds a prescribed level. The clamp circuit consumes large energy when activated and reduces the power efficiency significantly. To avoid this, a closed-loop power control has been included to control the power in the external module and transmit just right amount of energy to internal module [11,12]. However, for wireless high-compliance-voltage stimulator with multi-supplies, the clamp current problem and high power efficiency techniques haven't been well addressed yet. Regardless whether there is a closed-loop control, a wireless data link is required to send/receive commands. DPSK (differential phase shift keying), OOK (on off keying) and PSK (phase shift keying) modulations have been used for the data link [4], [6] and [7,8,13]. Among them, OOK modulation shuts down the power transmitter when it is in off phase and thus consumes less power, whereas PSK and DPSK modulations may provide high data rate.

In this paper, a power management chip with data telemetry for neural/muscle stimulation is described. A LV 2-stage rectifier is proposed to generate three DC outputs for two LDOs (1.8/3.3-V) and a 20-V charge pump to enhance power efficiency without compromising the performance of the data link. The two LV supplies are directly obtained through the two LDOs, respectively, and the HV supply is generated by the step-up 20-V charge pump. A low ripple voltage step-up HV charge pump based on the pulse-frequency-modulator (PFM) technique is proposed to reduce the output ripple and achieves high power efficiency. A wireless bidirectional data telemetry is also implemented on chip. With a power monitor circuit, the power system is able to transfer power status data from the internal module backward to the external module to support the wireless closed-loop control of the power transmitted from the

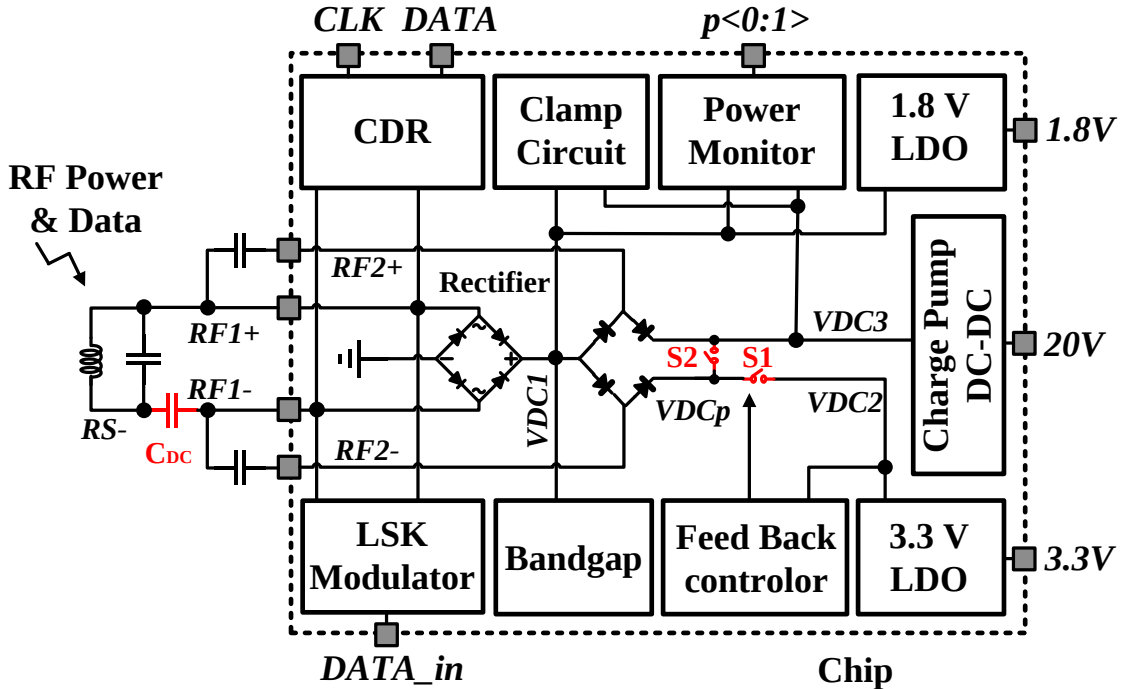


Fig. 3. Functional blocks of the power/data recovery system.

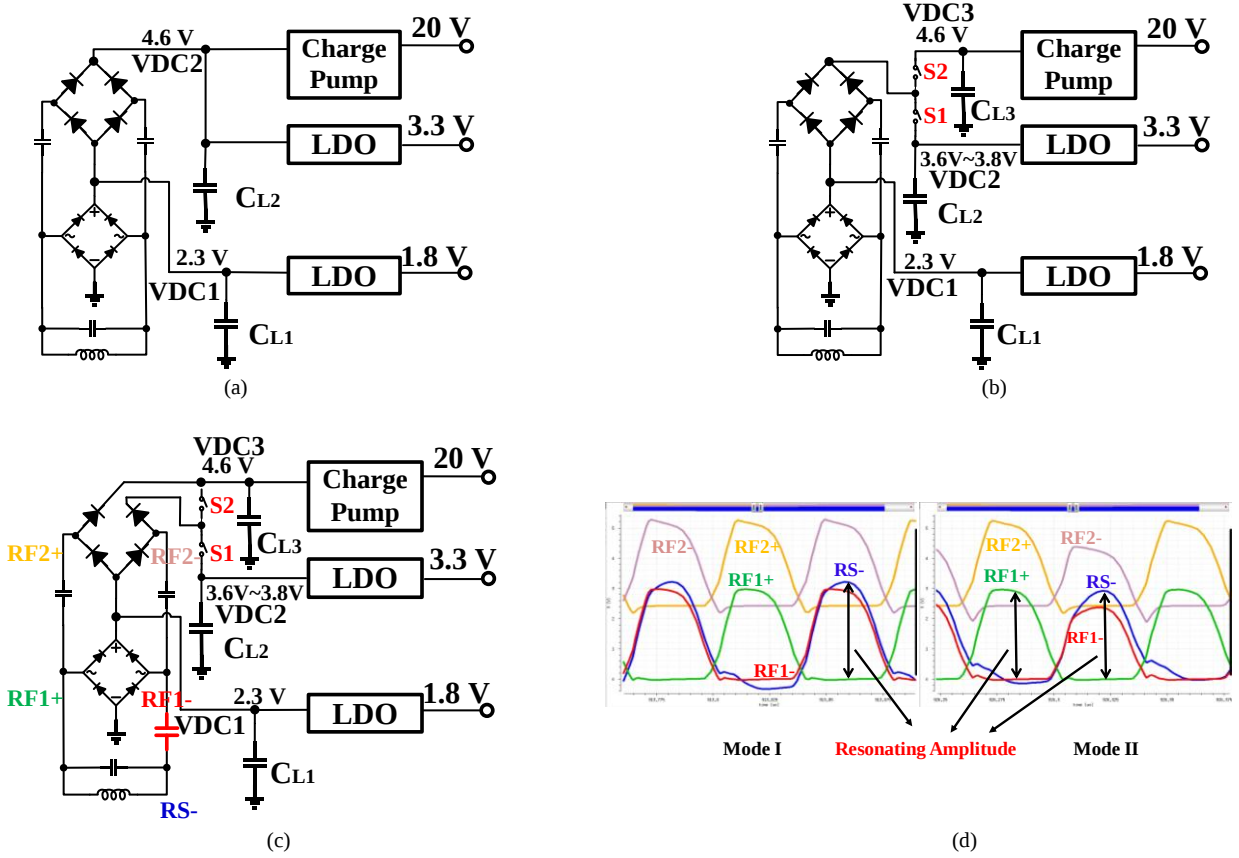


Fig. 4. (a) Conventional 2-stage rectifier. (b) A 2-stage 3-outputs rectifier based on time division technique. (c) The proposed 2-stage 3-outputs rectifier and (d) waveforms of the proposed rectifier.

external module to the internal module.

The rest of the paper is organized as follows. Section II describes the system architecture, as well as the 2-stage rectifier and the low ripple step-up charge pump. Section III, circuit implementations. Section IV presents the measurement results and discussion. Section V is the conclusion.

II. SYSTEM DESCRIPTION

Fig. 3 shows the functional blocks of the power/data recovery IC and its targeted application is to supply high-compliance-voltage stimulator. Three output voltages are 1.8 V for digital control circuit, 3.3 V for analog circuit and 20 V for HV-compliance output stage of the stimulator. A wireless bidirectional data link is also included on chip.

A 13.56 MHz power carrier is chosen for both power and data telemetry. A LV L-C resonator tank on the secondary side receives the transmitted power. A 2-stage rectifier generates three LV DC voltage sources. A capacitor, C_{DC} is inserted between the L-C tank and RF1- for DC voltage shifting. The 1st stage rectifier generates the lowest voltage, which is regulated by a LDO to obtain 1.8 V. The 2nd rectifier stage can be configured into either a full-wave rectifier or two half-wave rectifiers through two switches and generates two slightly different voltages: 3.6 and 4.6 V for the 3.3-V LDO and the charge pump in a time-division fashion. A feedback control circuit controls the time-division or the working mode of the 2nd rectifier stage. The detailed operation principle of the proposed

2-stage rectifier will be described in section II-A.

For wireless data telemetry, CDR circuit is connected to RF1+ and RF1- for clock and data recovery. The clock signal is directly recovered from the 13.56 MHz carrier, RF1+. The ASK forward data signal is extracted by an envelope detector, also from RF1+. A LSK modulator for backward data telemetry takes feedback data, such as that from simulator, and modulates the loading on RF1+ and RF1- [14-17]. A data reader at the external module can recover the backward data.

The power monitor block monitors the voltages at VDC1 and VDC3 and generates a 2-bit power status signal for closed-loop power control.

A. The proposed 2-stage rectifier

In this design, the minimum input voltage for 1.8-V and 3.3-V LDOs are 2.1 V and 3.6 V, respectively. For the step-up charge pump, a highest possible input voltage is preferred to reduce the number of charge pump stages. However, the gate-source break down voltage of the HV transistor is 6 V for the chosen CMOS process. Thus, the desired input voltage range for the charge pump is 4.2 ~5 V after leaving a safe margin for HV transistors in the charge pump. Based on aforementioned considerations, a 2-stage rectifier could be used to generate all three output voltages, as shown in Fig. 4(a). The 1st stage provides the supply for 1.8-V LDO and it should be higher than 2.1 V whereas the 2nd stage should be higher than 4.2 V for the charge pump. The 3.3 V can be derived from 4.2 V

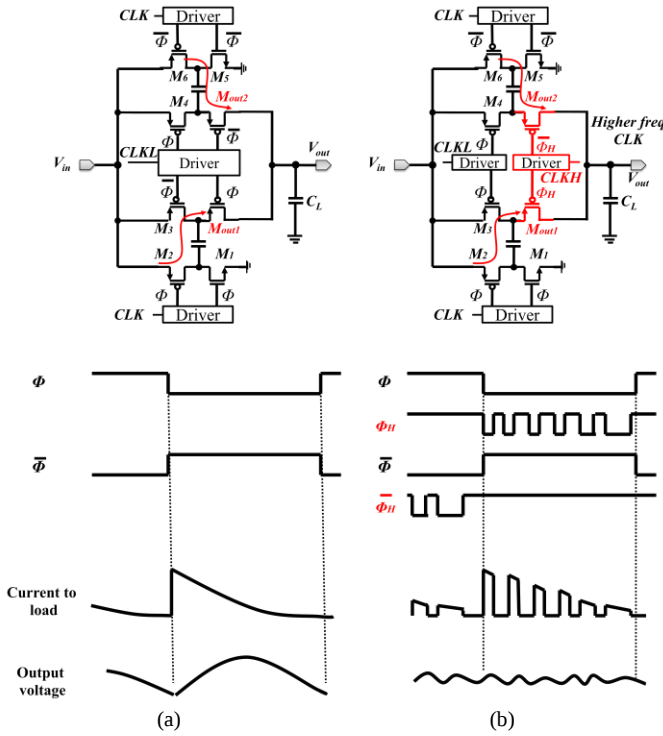


Fig. 5. Illustration of the proposed charge pump ripple reduction method: (a) conventional single clock and (b) the proposed 2-clocks work principle.

output with a LDO. However, by doing so, it would incur extra power consumption in the LDO, which reduces its power efficiency. In this work, a 2-stage rectifier is proposed to supply three different voltages, e.g. 2.3 V, 3.6 V and 4.6 V, where 3.6 and 4.6 V, in a time-division manner. In such an arrangement, the 3.3-V LDO is able to maintain good power efficiency.

Fig. 4(b) shows a possible rectifier arrangement based on the time-division, in which the 2nd stage rectifier supplies two outputs through switches S1 and S2. One problem with such an arrangement is that the ASK data will be corrupted by the resonating amplitude change caused by the switching between VDC2 and VDC3. Another drawback is that when the second stage switches between VDC2 and VDC3, it causes the 1st stage rectifier output to jump between VDC2/2 and VDC3/2. Fig. 4(c) shows the proposed 2-stage rectifier that can overcome these two problems. In the proposed 2-stage rectifier, a DC shifting capacitor C_{DC} is inserted between the resonator tank and the 1st stage rectifier to make the L-C tank resonating normally. The 2nd stage is divided into two half-wave rectifiers to supply two different voltages, simultaneously. The rectifier works in 2 modes. When VDC2 is larger than 3.8 V, the rectifier switched to mode I (S1 is open and S2 is closed). The 2nd stage rectifier now works as a normal full wave rectifier to supply VDC3, charge C_{L3} . When VDC2 is lower than 3.6 V, it switches to mode II (S1 is closed and S2 is open). The 2nd stage rectifier works as two half-wave rectifiers to supply VDC2 and VDC3, respectively. Thus, VDC2 is maintained between 3.6 V and 3.8 V, the rest of the energy is stored on the load capacitors at VDC1 and VDC3. Fig. 4(d) shows the waveforms in both mode I and II for the proposed 2-stage rectifier. The rectifier is same

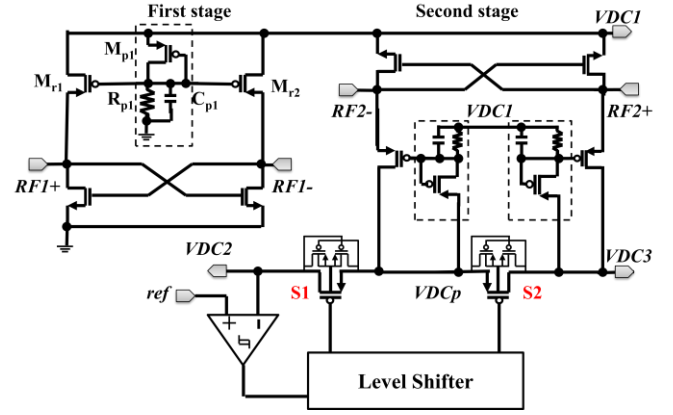


Fig. 6. Schematic of the 2-stage rectifier.

as the conventional 2-stage rectifier in mode I. In mode II, the AC amplitudes of RF1+ and RS- are different. But the resonating amplitude, $|(RF1+) - (RS-)|$ is constant, referred to as “unbalance resonating”, that is, RF1+ and RF1- have different peak voltages, but the same bottom voltage. The same applies to RF2+ and RF2-. Since the received power between mode I and mode II is slightly different, the amplitude voltage change of RF1+ is small. Thus, unlike the rectifier in Fig. 4(b), ASK signal on the 13.56 MHz power carrier is not affected in the proposed 2-stage rectifier.

B. Low ripple voltage multi-stage charge pump

The step-up charge pump is chosen as it can be fully integrated on-chip and has better transient response than the inductor based DC-DC converters. Since the stimulator is not always firing, charge pump is in light load most of the time. PFM is well suited for such applications [18]. The power loss of the charge pump can be expressed as

$$P_{loss} = f_{clk} C_{par} V_{sw}^2 + N_{sta} R_{on} I_{load}^2 \quad (1)$$

where f_{clk} is the switching clock frequency, C_{par} is the capacitance of the parasitical capacitor, V_{sw} is the voltage swing of the switches, N_{sta} is the stage number, R_{on} is the switch on-resistance and I_{load} is the load current. For a multi-stage HV charge pump, lowering the clock frequency can enhance the charge pump power efficiency. However, low clock frequency results in large ripple at the output. Some ripple voltage reduction techniques have been reported [19-21]. Controlling the voltage drop of power transistor [19] shows lower power efficiency in light load than PFM since its clock frequency is fixed. The interleaving regulation with multi-phase clocks [20] reduces the ripple, but needs a dual power stage, which increases the circuit complexity and number of capacitors. Dynamically changing the size of the charge pump driver together with PFM in [21] can reduce the ripple, but results in higher clock frequency and degrades the power efficiency.

In this work, we propose a simple ripple reduction scheme where the last transistor in the output stage of the 4-stage charge pump is controlled by a high frequency clock. This scheme can reduce the ripple voltage without significant impact on the power efficiency of the charge pump since the switch drivers

consume most of the power of the charge pump. Fig. 5(a) shows the conventional PFM control scheme. Charge pump transfers large amount of power in every clock phase at a low clock frequency for high power efficiency, resulting in a large ripple. Fig. 5(b) shows the proposed low ripple control method. A higher frequency clock is used only for the last transistor in the output stage, M_{out} . The time sequence of low frequency clock and high frequency clock is also included in Fig. 5. This allows the charge to be delivered more accurately and smooth the voltage ripple at the output. For the proposed 2-clocks scheme, Equation (1) can be modified as follows,

$$P_{loss} = 6 \cdot f_{clk_low} C_{par} V_{sw}^2 + 2 \cdot f_{clk_high} C_{par} V_{sw}^2 + R_{on} I_{load}^2 \quad (2)$$

The implementation of the high-frequency clock is based on the current re-use. It works well with the PFM control scheme and will be discussed in the next section.

III. CIRCUIT IMPLEMENTATION

A. 2-stage 3-outputs rectifier

The RF power received through the L-C tank is rectified by the 2-stage rectifier with dynamic body bias, as shown in Fig. 6. In the 1st stage of the rectifier, M_{p1} and R_{p1} provide bias voltages to reduce the forward conduction voltage V_{ds} of M_{r1} and thus improve the power efficiency [22-24]. The resultant increase of reverse current and quiescent power consumption on M_{p1} and R_{p1} (2.5 M Ω) can be limited to a small amount by carefully selecting design parameters. The designed range of V_{DC1} is 2.1-2.5 V. The same bias circuit is implemented for the 2nd stage rectifier which is divided into two independent half-wave rectifiers. S1 and S2 are two PMOS switches to connect V_{DCp} to either V_{DC2} or V_{DC3} . The range of V_{DC2} is 3.6-3.8 V while the range of V_{DC3} is 4.2-5 V. S1 is closed and S2 is opened when V_{DC2} is discharged to 3.6 V. After V_{DC2} reaches 3.8 V, S2 is close and S1 is open, the two half-wave rectifiers join together to charge V_{DC3} . S1 and S2 are two PMOS switches, with 1/4 size of M_{r1}/M_{r2} , which cause less than 20 mV voltage drop when turned on.

S1 and S2 are controlled by a hysteresis comparator and a level shifter which directly drives S1 and S2. Cross-coupled PMOS pairs are used to supply higher voltage to bulk of S1 and S2 to eliminate latch-up. In simulation, the control circuit consumes only 5 μ A current which mainly from the comparator. The power consumption of level shift is negligible.

Fig. 7 shows the simulation results of the proposed rectifier, compared with a conventional one. Both 1.8-V and 3.3-V LDOs have 360 μ A current load. V_{DC3} is connected to an 800 μ A current source to mimic the charge pump current consumption when driving 100 μ A load. The conventional rectifier in Fig. 4(a) with the same load conditions is used for comparison. Fig. 7(a) shows the simulated input and output waveforms of the proposed rectifier in both operation modes, where $VDCT$ is the output of conventional 2-stage rectifier. V_{DC3} gradually becoming higher than $VDCT$ indicates that under the same current loads, more power is stored on capacitor, C_{L3} , which is

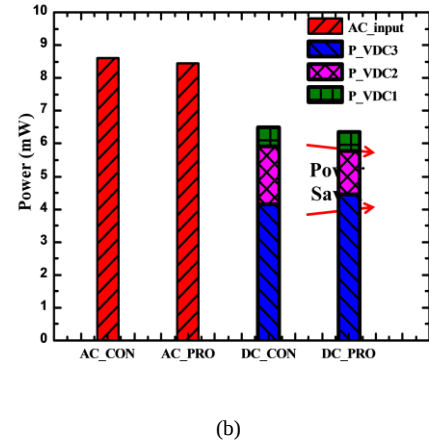
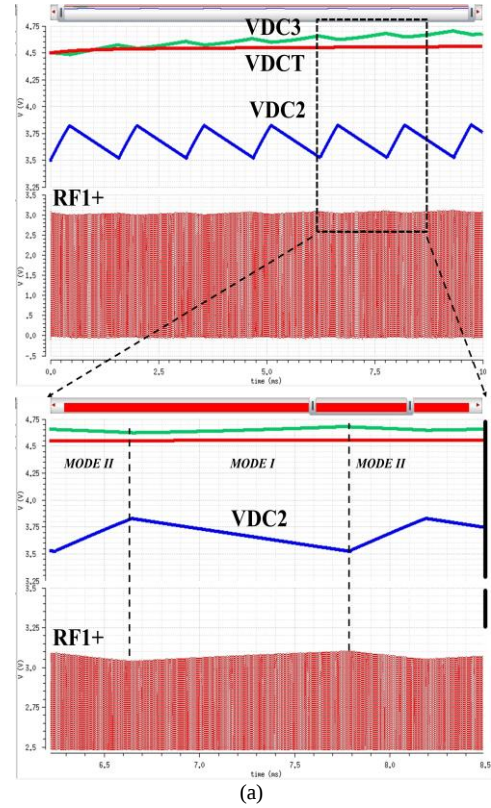


Fig. 7. Simulation results of the proposed rectifier: (a) waveforms of V_{DC2}/V_{DC3} in the proposed rectifier and Waveform of $VDCT$ in the conventional rectifier. (b) Power comparison of the proposed rectifier with the conventional one. AC_input is wirelessly received power by the conventional (AC_CON) and the proposed rectifiers (AC_PRO), respectively. P_V_{DC3} , P_V_{DC2} and P_V_{DC1} are the DC power consumed on V_{DC3} , V_{DC2} and V_{DC1} , respectively. DC_CON and DC_PRO denote DC output power of the conventional and the proposed rectifier, respectively. (for the conventional rectifier the 2nd stage DC power is $V_{DC3}+V_{DC2}$).

desirable, while V_{DC2} is maintained between 3.5V and 3.8V. Fig. 7(b) shows that there is a power saving in the V_{DC2} 3.3-V LDO in the proposed rectifier, which results in 6.3% improvement in power efficiency (DC_CON/AC_CON) of the whole system. In the zoomed-in view of $RF1+$ in Fig.7(a), the transition between mode I and mode II causes very tiny change on $RF1+$. This means that the mode change does not have any impact on ASK signal.

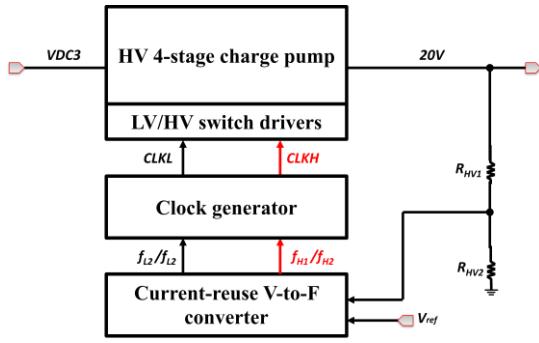


Fig. 8. Block diagram of the HV charge pump.

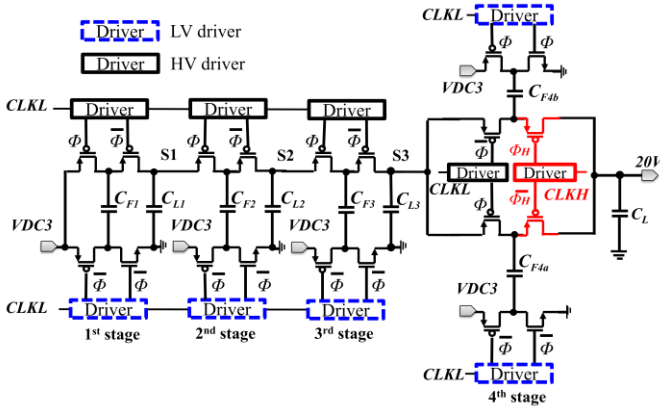


Fig. 9. Core circuit of the 20 V charge pump.

B. Low ripple HV charge pump and LDOs

A step-up charge pump is used to boost the output of the rectifier (VDC3) to 20 V. Fig. 8 shows the complete block diagram of the PFM controlled HV step-up charge pump. It consists of core circuit of charge pump, a current reuse V-to-F converter, clock generation circuit and LV/HV drivers. The

core circuit is a 4-stage charge pump, as shown in Fig. 9. The 4th stage of the charge pump employs cross-coupled structure to reduce the voltage ripple at the 20V output. In charge mode, ϕ is “0”, C_{F1} , C_{F2} , C_{F3} and C_{F4a} are charged by their preceding stages. C_{F4b} discharges to C_L at the output. Voltages at S1, S2 and S3 nodes decrease and the output is maintained by $V_{S3} + V_{C_{F4b}}$. In discharge mode, ϕ is “1”, C_{F1} , C_{F2} , C_{F3} and C_{F4a} are discharged and C_{F4b} is charged by S3. Voltage at S1, S2 and S3 increase and output voltage is supplied by $V_{S3} + V_{C_{F4a}}$. V_{S3} is the voltage of S3. $V_{C_{F4a}}$ and $V_{C_{F4b}}$ are the voltages on capacitors C_{F4a} and C_{F4b} , respectively.

The PFM control circuit includes a voltage sensing circuit consisting R_{HV1} and R_{HV2} , the proposed current re-use V-to-F converter, clock generation circuit and LV/HV drivers. The current reuse V-to-F converter performs error comparison and converts the voltage error to frequency through a differential VCO pair. Fig. 10 shows the detailed schematic of the V-to-F converter. It is modified from [25] with current re-use technique. A differential pair (M_{I1} and M_{I2}) drives four ring oscillators with two on each side. Since both sides are symmetrical, only one side is shown in Fig. 10. OSC_1Lf is a 7-stage ring oscillator whereas OSC_1Hf is a 3-stage ring oscillator. Two ring oscillators are connected in serial and re-use the same current. This not only saves the power, but also makes the two oscillators track each other. OSC_1Lf and OSC_1Hf outputs swing from 2.1 to 3.3 V and 1.2 to 2.1 V, respectively. The oscillating signals need to be shifted to full logic scale of 0 to 3.3 V, thus level shifters are needed. OSC_1Lf is directly shifted to the full logic scale, OSC_1Hf is shifted to 0-to-2.1V first and then 0-to-3.3V through two stages level shifters, as shown in Fig. 10. The level shifter chain must be carefully designed to prevent it from self-oscillating. The startup of the V-to-F converter is controlled by signal ST which is enabled after 1.8-V LDO and 3.3-V LDO successfully startup.

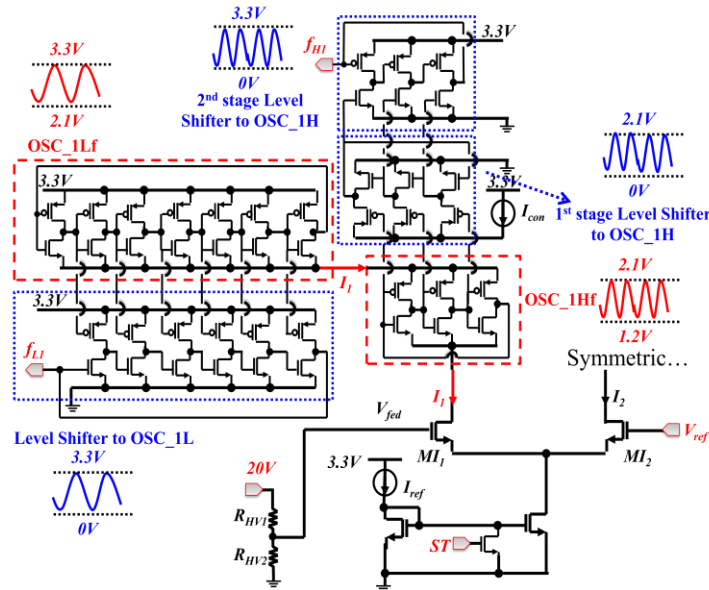


Fig. 10. Schematic of the current -reuse V-to-F converter.

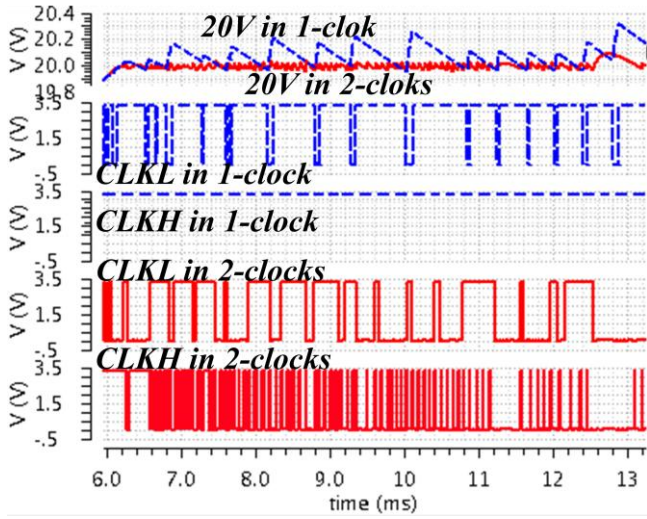


Fig. 11. Simulation results of the charge pump 2-clocks ripple reduction.

The clock generation circuit monitors the frequencies of these four oscillators (f_{L1} , f_{H1} , f_{L2} and f_{H2}) and generates two clock signals ($CLKL$ and $CLKH$) to control the 20 V charge pump through LV/HV drivers. $CLKL$ determines the entire charge pump clock phase shifting and $CLKH$ controls the switches in the output stage and reduces the output ripple. The frequency of $CLKL$ is designed to be low (< 10 kHz) to avoid significant switching power consumption on parasitic capacitance. The frequency of $CLKH$ is set to be around $6 \times CLKL$, above which the ripple reduction shows little further improvement. The LV/HV switch drivers are designed to have low current dissipation and sharp clock edge. Protect circuit is also included in the high voltage charge pump [26].

Fig. 11 shows the simulation results of the charge pump with/without the high-frequency clock, $CLKH$. When $CLKH$ is activated, the ripple voltage at 20-V output is reduced by more than one half compared with that uses only low frequency clock $CLKL$. In simulation, input voltage is 4.6 V and load current is 500 μ A.

Two LDOs are powered by $VDC1$ and $VDC2$, and generate 1.8 and 3.3 V, respectively. The schematic of LDOs is shown in Fig. 12. By inserting a source follower, the pole at $M2$ gate is pushed to higher frequency than unit-gain bandwidth to guarantee the stability. The same structure is utilized for both LDOs.

C. Clock and Data Recovery and Power monitor

The clock recovery circuit is based on a schmitt trigger inverter, as shown in Fig. 13(a) [27]. $RF1+$ is fed into the circuit through a capacitor. The data recovery circuit is shown in Fig. 13(b). The forward ASK modulated RF carrier signals, $RF1+$ and $RF1-$, are connected to a PMOS transistor, M_D , acting as a detector. A passive low pass filter consisting of R_A and C_A is used to extract the data envelope from the detector output. Another passive low pass filter with lower cut-off frequency is used to extract the average voltage of the envelope. The data is recovered through a comparator and a buffer by comparing the envelope at A with average voltage of the

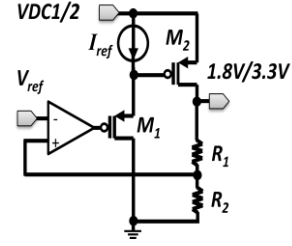


Fig. 12. Schematic of the LDOs.

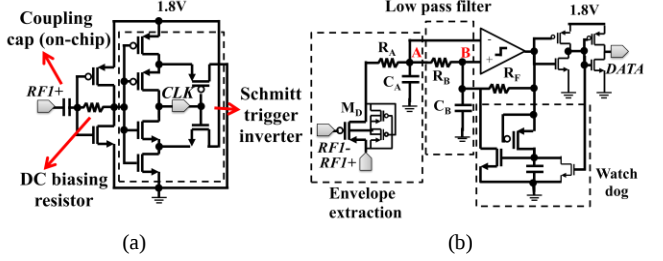


Fig. 13. Schematic of CDR: (a) clock recovery circuit and (b) ASK data recovery circuit.

envelope at B. A feedback resistor R_F is used to introduce a small hysteresis voltage (+30mV) between A and B to increase the robustness of the data recovery circuit. The correct standby state of DATA should be '0'. However, there is a risk to form a false latch through R_F where the voltage between A and B is -30mV, causing DATA to be '1' in standby state. To prevent the false standby state, a watch-dog circuit is implemented to avoid the false latch.

The LSK modulator is a set of switches, which short $RF1+$ and $RF1-$ with different resistors thus change the loading of the L-C tank. The modulation depth can be adjusted based on the trade-off between the power requirement and the demodulation of the data by the external reader.

Power monitor circuit consists of two comparators powered by 1.8 V. It monitors the voltages of $VDC1$ and $VDC3$. A 2-bit output digital signal $p<0:1>$ indicates three states: "00" for under-powered or startup, "01" for proper-powered and "11" for over-powered.

IV. MEASUREMENTS AND DISCUSSION

The wireless power management and bidirectional data telemetry circuit was fabricated in a 0.18- μ m CMOS technology with 24V LDMOS option. Fig. 14(a) shows the microphotograph of the chip. Fig. 14(b) shows the measurement setup for the functional verification of the wireless power management. $RF1+$ and $RS-$ are connected to the secondary coil. The external primary coil is driven by a class-E power amplifier whose supply voltage is controlled by FPGA. The space between the two coils is 0.5cm and the detailed information can be found in table I. The load currents for 1.8-V LDO, 3.3-V LDO and charge pump are set to be 360 μ A, 360 μ A and 100 μ A, respectively. All the subsequent measurements are done under the same loads, unless specified otherwise.

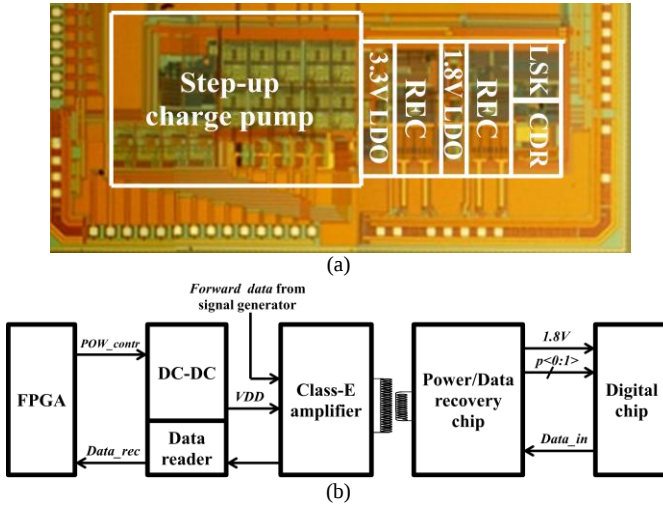


Fig. 14. (a) Die photo of the power/data recovery module and (b) measurement setup.

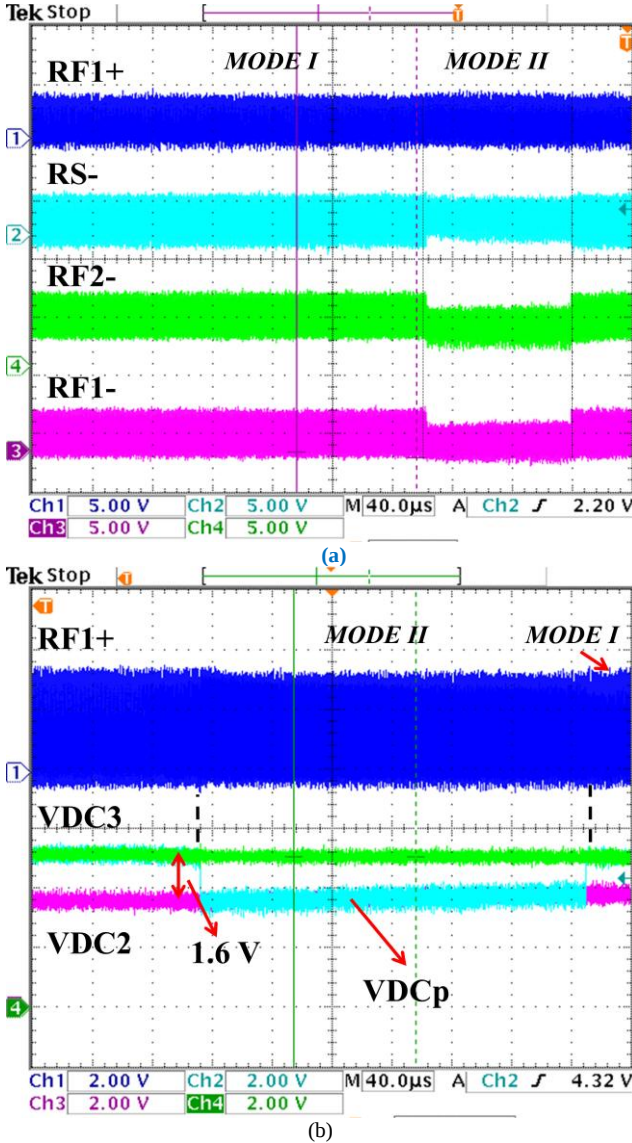


Fig. 15. Measured waveforms at inputs and outputs of the proposed 2-stage rectifier in different modes: (a) inputs to the rectifier and (b) input (RF1+) and outputs (VDC2 and VDC3) of the rectifier.

The measured performance and circuit parameters are

TABLE I. SYSTEM PARAMETERS

System	
Technology	0.18 μm CMOS
Area	$\sim 3.5 \text{ mm}^2$
Coupling Coils	
External coil	9.6 μH
Internal coil	2.1 μH
Coils' distance	5 mm
Wireless Power Management	
Carrier frequency	13.56 MHz
Outputs	1.8V/3.3V/20V
Rectifier PE	77 %
LDOs I_{standby}	30 μA^*
Charge pump PE	82 %
Total PE	49%
Bidirectional Data Telemetry (forward/backward)	
Mode	ASK/LSK
Data rate	61.5k/33.3k bps
Power	17 μW /1.2 μW^*

*Simulation results

summarized in Table I. Power efficiency (PE) of individual block is measured using different optimal loads. The total PE denotes the peak power recovery efficiency and is calculated with three 100 μA /300 μA /500 μA current loads connected to 1.8V/3.3V/20V outputs, respectively, that is,

$$\begin{aligned}
 \text{PE}_{\text{overall}} &= \frac{\text{effective DC output power}}{\text{AC input power}} \\
 &= \text{PE}_{\text{rec}} \cdot \left(\frac{\text{LDO current}}{\text{total current}} \cdot \text{PE}_{\text{LDO}} + \frac{\text{charge pump current}}{\text{total current}} \cdot \text{PE}_{\text{CP}} \right) \quad (3)
 \end{aligned}$$

where $\text{PE}_{\text{overall}}$ is the total PE. PE_{LDO} and PE_{CP} are the PEs of LDOs and charge pump, respectively.

Table II is the comparison with the similar works reported previously.

A. Rectifier measurement

Fig. 15(a) shows the measured waveforms of the resonator tank output and the rectifier inputs. Operation mode I or II is determined by voltage of VDC2 that should be maintained at an average voltage of 3.7V (3.6~3.8V). If it is less than 3.6 V, the rectifier is switched to mode II. If it is higher than 3.8 V, the rectifier is switched to mode I. In mode I, RF1+ and RS- have same waveform (out of phase) and same amplitudes. In mode II, RF1+ maintains its shape since its connection doesn't change from mode I. However, RS- amplitude decreases due to different loadings. Fig. 15(b) shows RF1+ and the two outputs waveforms of the 2nd stage rectifier. It can be clearly seen that VDC2 is being charged up in mode II.

Fig. 16 shows the measured power saving in the proposed 2-stage rectifier as compared to the conventional rectifier. The conventional rectifier is formed by simply connecting VDC2 to VDC3 off-chip. Since VDC2/VDC3 voltage now needs to reach at least 4.2V for the charge pump, more DC power is consumed on VDC2 in the conventional rectifier. The conventional rectifier shows higher wireless power transmission efficiency. However, the proposed rectifier still shows better system

TABLE II. COMPARISON WITH PREVIOUS WORKS

	[4]ISSCC 2013	[6]TBCAS 2012	[8]TBCAS 2011	This work
Process	32 V 0.18 μ m CMOS	20 V HV CMOS	0.35 μ m CMOS	24 V 0.18 μ m CMOS
Area (mm ²)	NA	4/9	1.5 x 1.6	~ 3.5
Frequency (MHz)	2	13.56	0.256	13.56
Power Supply (V)	± 12 V, ± 1.8 V	50 V/20 V **	5.8 V, 2 V, 1.4 V	20 V, 3.3 V, 1.8 V
Power Efficiency (%)	81(HV rectifier)	90(rectifier, sim)	NA	49
DC-DC type	HV/LV rectifier + LDO	HV rectifier + step-down charge pump	LV rectifier + step-up charge pump + LDOs	2-stage LV rectifier + step-up charge pump + LDOs
Forward Data modulation	DPSK	OOK	PSK	ASK
Data Rate (kbps)	2 Mbps @ 20 MHz carrier*	300	~ 60	61.5
Backward data rate	Non	Non	Non	33.3 kbps (LSK)
Closed-loop power control	Non	Non	Non	Yes

* The forward data link uses another antenna.

** The step-down DC-DC is not integrated in the same chip.

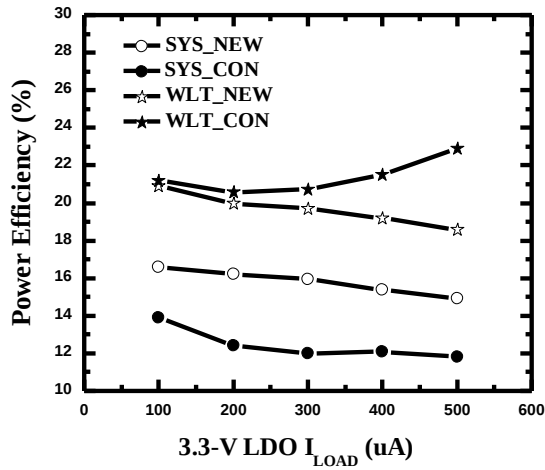


Fig. 16. Measurement results of the proposed rectifier: SYS_NEW and SYS_CON are the overall power efficiencies, from signal generator to the output of the proposed and the conventional rectifiers, respectively. WLT_NEW and WLT_CON are the wireless power transmission efficiencies, from signal generator to the secondary coils, for the proposed rectifier and the conventional rectifier, respectively.

overall PE with maximum 4% improvement. In measurement, the load currents are 360 μ A/800 μ A for VDC1/VDC3, respectively, whereas the load current for VDC2 is changed from 100 μ A to 500 μ A.

B. Charge pump ripples voltage reduction

Fig. 17 shows the comparison measurement of charge pump with and without high-frequency clock for ripple reduction. It can be clearly seen that with the high-frequency clock, the ripples voltage is significantly reduced. As shown in Fig. 18(a), the ripple reduction in the proposed 2-clocks charge pump is around 40% when the load current is below 600 μ A. When the load current further increases, the DC output becomes lower than 20V (Fig. 18(b)), CLKL increases by the PFM control (>

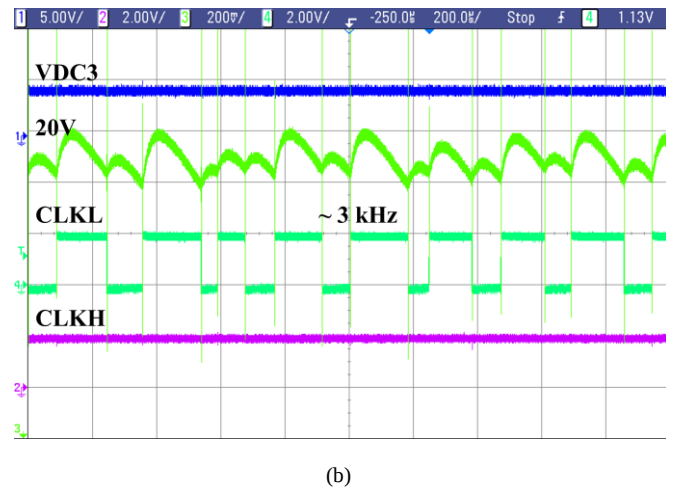
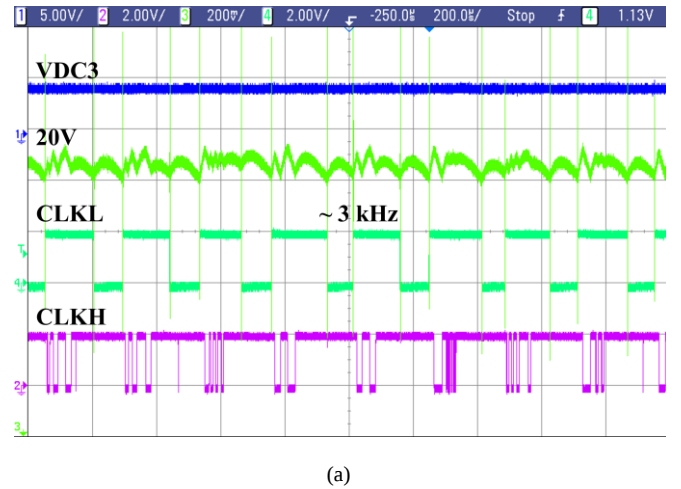


Fig. 17. Measurement results of the 20 V charge pump: (a) with and (b) without high frequency clock for ripple reduction.

1MHz) and thus the ripple is low and shows no difference between the two cases. As shown in Fig. 18(b), the charge

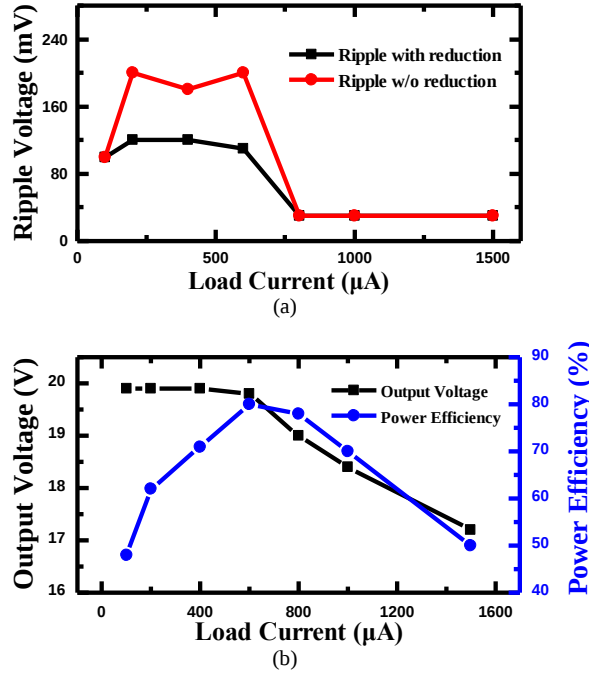


Fig. 18. Measurement results of (a) charge pump output ripple and (b) the charge pump power efficiency versus load current.

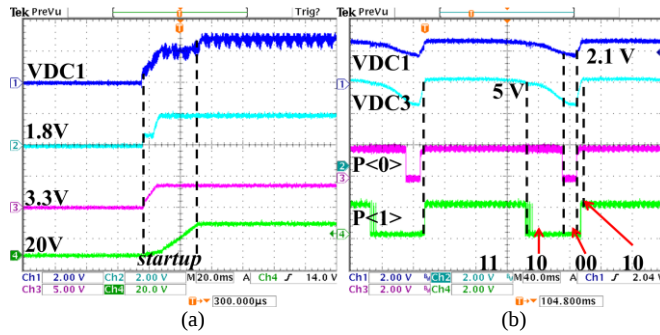


Fig. 19. Measurement results of startup of the power unit and power monitor: (a) Waveforms of the power unit startup and (b) Waveforms of the power monitor measurement.

pump achieves 82% peak efficiency at 600 μA load current. The output voltage can not be maintained at 20 V if load current further increases. The proposed 2-clocks scheme has no effect on the power efficiency.

C. System functional verification

Fig. 19 shows the startup sequence of the power management and power monitor function. Charge pump's startup is controlled by 1.8 V power-on-reset (POR) and VDC3. Hence, it is the last one to start working, as shown in Fig. 19(a). After the charge pump is started, VDC1 reaches its highest value. This means that the charge pump absorbs large power during startup to charge the flying and load capacitors. Power monitor is measured when RF signal is modulated with low frequency to produce a varying RF power. Fig. 19(b) shows the power monitor states. When VDC1 < 2.1 V, $p<0:1>$ is "00", it means the received power is not enough or the circuit is starting up.

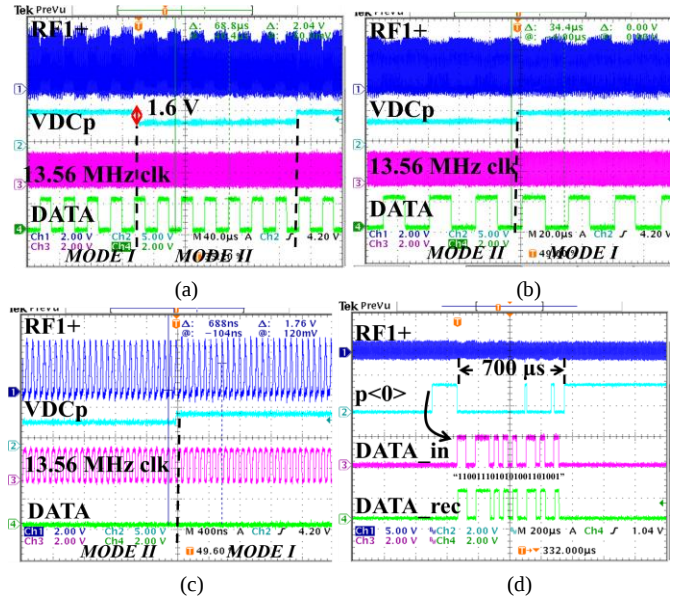


Fig. 20. Measurement results of the bidirectional data link: (a) forward data link, DATA is the data recovered by CDR. (b) is the zoomed-in view of (a) and (c) is the further zoomed-in view of (b). (d) is backward data link. DATA_in is the data feed into LSK modulator and DATA_rec is the data recovered by the external data reader.

When VDC1 > 2.1 V, $p<0:1>$ is "10", it means the received power is normal. When VDC3 > 5 V, $p<0:1>$ changes into "11", which means too much power is received and the clamp circuit is already activated. The closed-loop power control circuit should be activated to reduce the input power.

In forward data link measurement, a signal generator is used to generate power carrier with ASK modulation. Fig. 20(a) shows the forward data and clock recovery waveforms. The change of VDCp indicates that the rectifier changes from mode I to mode II and then back to mode I. RF1+ is not influenced by the sudden rectifier mode change because of the unbalance resonating. The signal on the carrier is successfully recovered by the CDR circuit. Fig. 20(b) is the zoomed-in view of Fig. 20(a), where it shows that during the mode change, the ASK modulation on RF1+ is not affected. Fig. 20(c) shows that the 13.56-MHz clock is correctly recovered. In measurement, when VDC3 voltage is below 5V, the rectifier mode transition cause <200 mV voltage change in RF1+ envelope. But the CDR won't be affected as long as the voltage change is below 500 mV.

Fig. 20(d) shows the backward data link measurement. Power monitor's status change is detected and transferred to the external module in a data packet (DATA_in) through LSK modulator. The bottom trace shows the same data recovered by an external reader circuit. When LSK modulator is active, it will drain some current from the secondary coil. This temporarily causes the voltage to drop and $p<0>$ changes to "0". This status won't be captured since the data sampling frequency is 1 kHz whereas the "0" duration is only 700 μs , and the next sampling is another 300 μs later. After data transmission is completed, $p<0>$ goes back to "1" again.

Fig. 21 shows measurement of the closed-loop power control function. POW_contr is a 1-bit signal that controls the supply

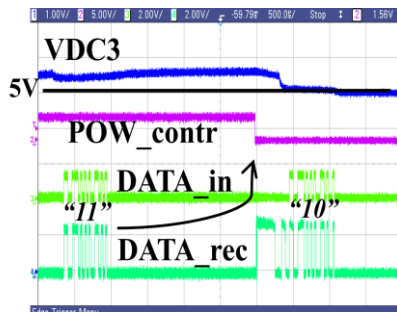


Fig. 21. Measurement results of the closed-loop power control. *POW_contr* controls supply voltage of external class-E amplifier. *DATA_in* and *DATA_rec* are the data fed into LSK modulator and the data recovered by an external data reader.

voltage of the class-E power amplifier to regulate the power transfer. Initially, *VDC3* exceeds 5 V, $p < 0:1$ turns into “11”. This information is transferred backward to the external module through coupling coils. The power control is done through FPGA, which decodes the *DATA_rec* and turns *POW_contr* from high to low. The supply voltage of the class-E amplifier then decreases and reduces the power transferred to the secondary coil. Hence *VDC3* starts decreasing until $p < 0:1$ becomes “10”, which is represented by the second data of *DATA_in* in Fig. 21. This new data is fed back to the external module again, completing the closed-loop power control.

V. CONCLUSION

A wireless power management and data telemetry IC for high-compliance-voltage electrical stimulation applications is demonstrated in a 0.18- μm CMOS technology. The chip is powered by 13.56MHz RF carrier and generates 1.8 V, 3.3 V and 20 V supplies. The proposed unbalance resonating L-C tank and the time-division 2-stage rectifier generate three supplies for two LDOs and the charge pump, respectively, to improve the power efficiency. In the 20V charge pump implementation, the 2-clocks technique is proposed and reduces the ripple voltage by 40 % without degrading the charge pump efficiency. Bidirectional data link is successfully verified in the measurement with data rate of 61.5 and 33.3 kbps respectively. Closed-loop power control is also verified based on the power monitor integrated in the chip. The power management and data telemetry module could be used for fully implantable HV compliance nerve/muscle stimulator.

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