# Stress Analysis and Design Optimization for Low-k Chip with Cu Pillar Interconnection

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***Abstract*—Cu pillar technology can cater for high I/O, fine pitch and miniaturization requirements compared to wire bonding and conventional solder flip chip technologies. However, chip-package interaction (CPI) of Cu pillar and low-k chip is a critical challenge during assembly process due to stiffer Cu pillar structure compared to conventional solder bump. Thermo-compression bonding (TCB) process was adopted and used for fine pitch Cu pillar assembly on Cu/low-k chip to reduce the package warpage and low-k stress. In this study, a novel TCB process modeling methodology by using a 2D axisymmetric finite element model with global-local technique was demonstrated by considering step-by-step process conditions. The TCB modeling method was validated by experimental data. The simulation results show that TCB process results in much lower package warpage and low-k stress compared to conventional reflow process. Based on the proposed TCB modeling method, the comprehensive parametric studies were conducted to optimize TCB process and Cu pillar design for package reliability improvement, including bonding process conditions, Cu pillar structure design, package geometry, and packaging materials selection. Reflow process induced package warpage and low-k stress were also simulated for comparison. The final package and assembly solution was successfully achieved based on suggestions and recommendations provided by simulation results.**

***Index Terms*—Chip-package interaction, CPI, Cu/low-k, Cu pillar, finite element modeling, flip chip, stress analysis, thermo-compression bonding, TCB.**

## I. INTRODUCTION

As the demands for higher performance, further miniaturization, higher I/O density, and fine pitch in electronic packaging, Cu pillar technology can cater for these demands compared to wire bonding and conventional flip chip technologies. Cu pillar is stiffer than conventional C4 bump, which leads to several challenges for chip-package interaction (CPI), especially for chip with Cu/low-k structures. Recently, the CPI study was widely conducted by researchers through numerical simulation and experimental methods to optimize Cu pillar structure design and material selection [1]-[4]. Usually, the conventional reflow process is used to assemble chip with Cu pillar to substrate. However, when the pitch of Cu pillars shrinks further to around 100μm, the conventional reflow process encounters challenges like die shift, high low-k stress, and short connection. Thermo-compression bonding (TCB) process can cater for the requirements of fine pitch Cu pillar assembly on the Cu/low-k chip [5]. During TCB process, the substrate has lower temperature than the chip, which reduces the CTE mismatch induced stresses and package warpage. In addition, the alignment of interconnection can be precisely controlled for fine pitch Cu pillar assembly.

Finite element analysis (FEA) of assembly process can lead to the possibility for virtual experiment, leading to an improved knowledge of how parameters influence the bonding process induced stresses. However, most published methods focused on reflow process induced stresses [1], [2] or thermal cycling loading induced stresses [3], [6] on Cu pillar and Cu/low-k structures. A global-local technique was one effective modeling method to study the reliability of the interconnection in package or chip level. Gils et al [7] used a multi-scale modeling method to analyze delamination in Cu/low-k bond pads. Lee et al [8] implemented sub-modeling procedures for the impact prediction of interfacial crack in complicated Cu/low-k interconnects and an approximated criterion for determining the dimensions of sub-model was suggested and demonstrated. Shen [9] investigated thermal stress in Cu/low-k structures using 3D FEA simulation under process temperature and the results showed that low-k material with low CTE and high modulus is more reliable under thermal loading. Paik et al [10] studied the effect of low-k material on stress and stress-induced damage in Cu/low-k structures using FEA simulation. Results proposed that thermal fatigue under thermal cycling is thought to be more effective in the failure analysis of Cu/low-k interconnections rather than high temperature storage test. There is lacks of TCB process simulation study from published literatures. In this study, a TCB process modeling methodology was established considering the process condition step by step. In the reliability study of electronic assembly, both 2D and 3D FEA models were commonly used in FEA modeling. Lin et al [6] used 2D and 3D FEA models to optimize design of Cu pillar structure to reduce low-k stress. Lee et al [8] implemented a 2D half model with global-local modeling method to study interfacial cracking of the low-k chip. In our previous study, 2D and 3D FEA models were used to investigate fatigue life of solder joints subjected to thermal cycling (TC) [11]. Results comparisons among different models were carried out. Simulation results showed that 2D axisymmetric FEA model can give more accurate and reasonable results than 2D plain strain model when compared with 3D quarter model [11]. Therefore, a 2D axisymmetric model with global-local technique was implemented in this study to reduce model size without loss of accuracy. The simulation results show that TCB process results in much lower package warpage and low-k layer stress compared to reflow process. The results demonstrated the advantages of TCB process used for fine pitch Cu pillar assembly.

The TCB process parameter and pillar structure design still need to be further optimized. In this study, comprehensive parametric studies were conducted, including bonding process and conditions, Cu pillar structure design, package geometry, and packaging materials selection such as underfill, substrate core material. It was found that the following parameters are critical ones affecting warpage and low-k stress during TCB process: substrate core thickness and CTE, substrate temperature, and underfill CTE. Simulation results were used to optimize TCB process condition and Cu pillar design for

CPI study and package reliability improvement. Finally, a reliable assembly with Cu pillar interconnection was successfully achieved.

## II. TCB Process and Test Vehicle

Compared to the conventional C4 process, TCB process can cater for the requirements of fine pitch Cu pillar assembly [5]. During TCB assembly process, non-conductive paste (NCP) as an underfill encapsulation material will be used to prevent low-k layer from fragile cracking [12], [13]. The partially cured NCP encapsulation layer during TCB process absorbs thermo-mechanical stress induced by CTE mismatch between the chip and the substrate, which mitigates and protects interconnects from transferring large stress to the low-k layer.

The test vehicle used in this study is shown in Fig. 1. A large low-k chip with 28 nm node and chip size of 18 mm × 18 mm is attached onto a low CTE substrate using the TCB process. The Cu pillar joint has a pitch of 130 µm, a diameter of 65 µm, and joint height of 40 µm. The package size is 25 mm × 25 mm. TCB-NCP process for a large low-k chip is difficult to achieve. Typically, very high bond force is required to ensure no cold joint and defect-free bonding. The process flow starts by applying plasma cleaning on substrate surface to reduce surface tension for better NCP flow and to remove any surface contamination. NCP is then dispensed onto the substrate surface with preheating about 80°C. The low-k chip is pre-aligned accurately with respect to the substrate and thermo-compression bonding with specific thermal and bond force profile is applied to complete the interconnect formation and cure the NCP simultaneously. The bonding profile parameter setting includes chuck temperature, bond force, bond temperature, force and temperature trigger timing and NCP dispense pattern [14]. Fig. 2 shows the Cu pillar interconnections with using Sn3.5Ag solder joints after TCB process.

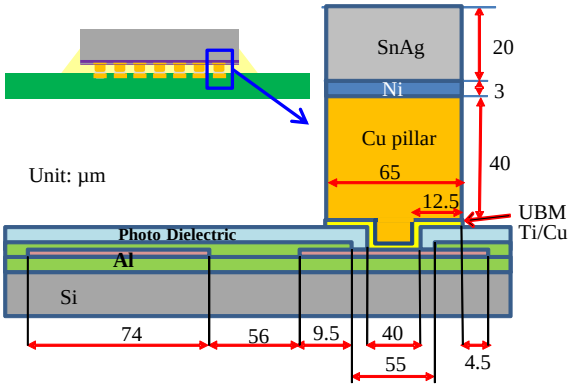



Fig. 1. Schematics of test vehicle with Cu pillars.

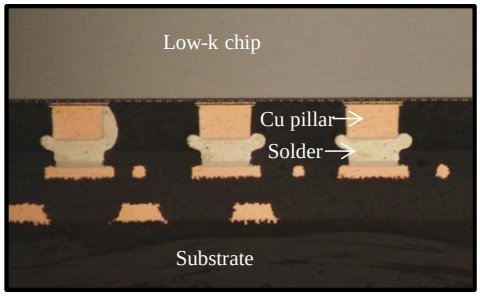



Fig. 2. Cross section view of bonded Cu pillar interconnection using TCB process.

## III. Modeling Methodology for TCB Process

In the TCB process, the temperature loading for all the parts is not isothermal condition like reflow (RF) process. Substrate is maintained at a constant temperature such as 80°C by the heat block. The temperature of the chip increases with time and the maximum temperature is more than 250°C to make the solder melt. At the same time, the bonding pressure is added onto the chip to make NCP fill to the gap between the chip and substrate and make good Cu pillar joints. The TCB process modeling is more complicated than reflow process modeling in terms of loading conditions. In this study, a TCB process modeling methodology was established with considering loading condition step by step.

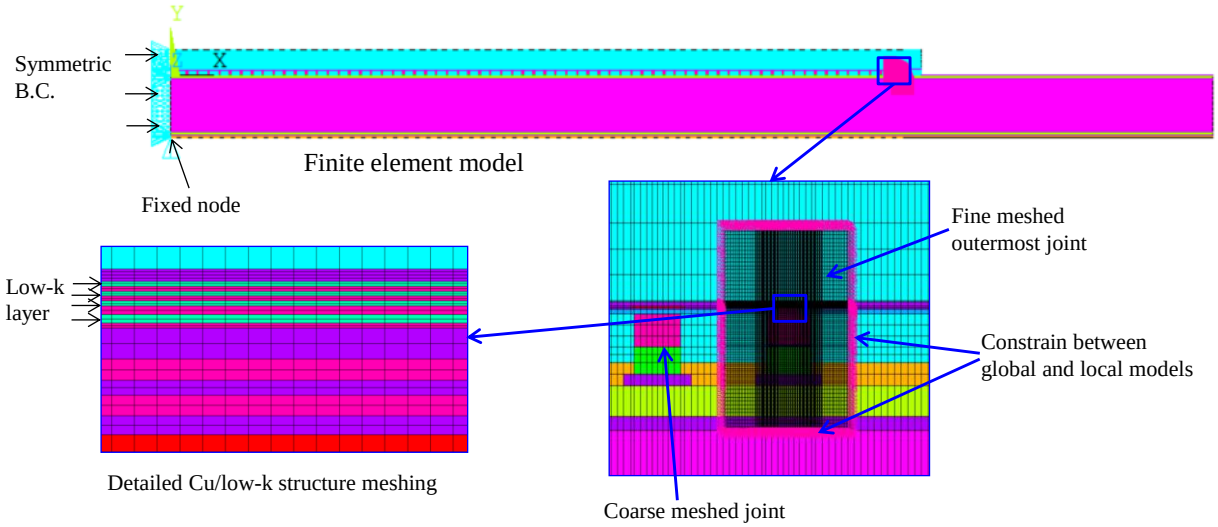



Fig. 3. 2D finite element model for TCB process modeling using a global-local technique.

A 2D half model was implemented due to symmetric package layout. Fig. 3 shows a 2D axisymmetric finite element (FE) model cutting along package diagonal for fine pitch Cu pillar assembly. The Cu/low-k structures were simulated by simplifying the structure to 4 low-k layers. The outmost corner joint is the most critical joint due to the largest distance to neutral point (DNP) of the package. Therefore, the outermost Cu pillar joint was modeled in detail and the other joints were simplified in the global model with coarse meshing. Such treatment achieves accurate results at the critical joint and also considers the effect of critical joint location with saving huge computing resources. Constrain equation was applied between the global model and the fine meshed local model of the outermost joint to make the displacement transfer between the global and local models. Element birth and death technique was adopted in the TCB process modeling to let NCP and solder materials deactivate and reactivate in the FE model at a reasonable time step.

Six steps were simulated sequentially in the TCB process modeling to match the temperature loading as shown in Fig. 4. The static analysis was conducted for TCB process modeling, in which time or rate-dependent material properties, such as viscoelastic behavior of polymer-based materials and creep behavior of the solder joints, were not modeled due to short process duration. The critical and specific temperature loadings in the real TCB process were approximately modeled with different steady state steps. The substrate has a constant temperature of 80°C during the TCB process. Temperature of 150°C is a curing temperature of NCP material. Temperature of 220°C is a melting temperature of the solder. Temperature of 250°C is the maximum temperature for the low-k chip. Different stress free temperatures were modeled for different materials according to a real process condition. The deformation and stress can be simulated at different temperatures. The purpose of the simulation is to investigate the low-k stress under the TCB process and to reduce low-k stress through optimization of Cu pillar design and TCB process condition. Table 1 lists the materials and their mechanical properties used in the FE model. For metal materials, such as Al, Cu, Ni, and SnAg, an elastic-plastic behavior was simulated. For solder mask, solder, NCP, temperature-dependent material properties were used. Substrate core and build-up materials were considered as orthotropic material properties.

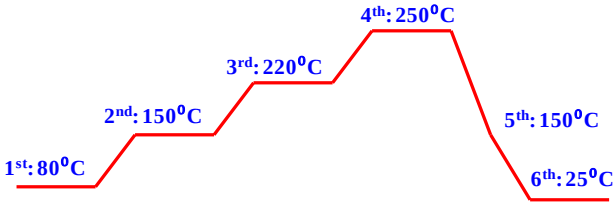



Fig. 4. Loading profile used in TCB process modeling.

Reference model for TCB process modeling includes Cu pillar height of 40 µm, solder joint height of 20 µm, photo dielectric thickness of 6 µm and opening of 30 µm, die thickness of 300 µm, and substrate core thickness of 800 µm. Fig. 5 shows the stress results at the maximum temperature of 250°C along low-k layer 4 closing to Cu pillar as shown in Fig. 6. The maximum stresses occur under the pillar position corresponding to pillar opening. Normal stress (Sy) and principal stress (S1) are almost the same in low-k layer at 250°C. Normal stress (Sy) at low-k layer is tensile stress at 250°C. After TCB process completes and cools down to room temperature, normal stress (Sy) at 25°C at low-k becomes compression stress under Cu pillar as shown in Fig. 7. The maximum tensile stress at 250°C and compression stress at 25°C were compared as shown in Fig. 8 for four low-k layers. The tensile and compression stress values are almost the same for different low-k layers at 250°C and 25°C, respectively. The low-k layer 4 was chosen for stress analyses because it has slightly higher stress than other layers due to close to pillar bump. Normal stress (Sy) is a critical stress component controlling the low-k layer delamination or cracking, which will be selected for stress analysis.

TABLE I
MATERIAL PROPERTIES USED IN FINITE ELEMENT MODEL

| Materials | CTE (ppm/°C) | Young's modulus (GPa) | Poisson's ratio |
|---|---|---|---|
| Silicon die | 2.6 | 130 | 0.278 |
| SiO2 | 1 | 71 | 0.17 |
| SiN | 3 | 310 | 0.27 |
| Al | 25 | 70 | 0.33 |
| Cu | 17 | 121 | 0.34 |
| Ni | 13.1 | 207 | 0.31 |
| Sn3.5Ag | 22 | 47.6 (25°C) | 0.4 |
| Photo-dieletric | 70 | 1.8 | 0.3 |
| Solder mask | 50/160 (Tg=110°C) | 3.2/0.11 | 0.32 |
| Substrate core | 7 (in) 30 (out) | 26.9/11 | 0.39, 0.19 |
| Build-up | 23/78 (Tg=170°C) | 7.5/0.75 | 0.32 |
| NCP UF | 27.2/63.3 (Tg=177°C) | 10.8/1.6 | 0.3 |
| Low k | 23 | 7.7 | 0.3 |

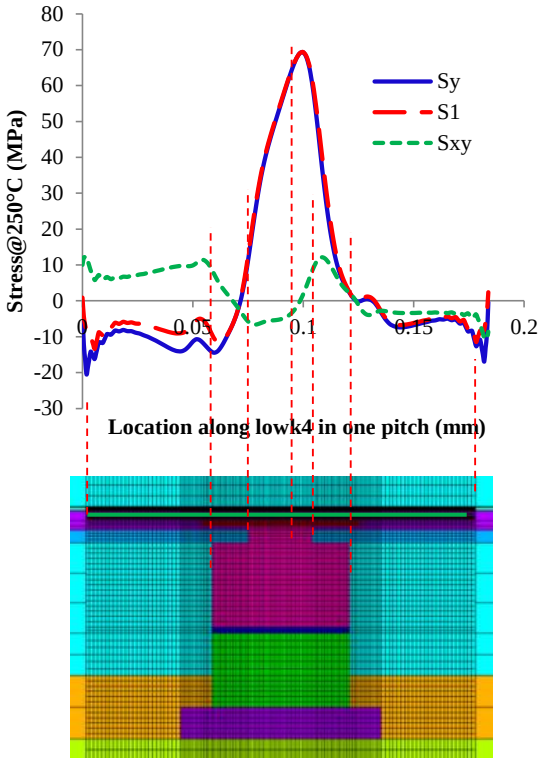



Fig. 5. Low-k layer stress at 250°C under TCB process.

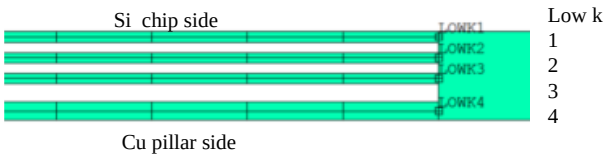



Fig. 6. Cu/low-k layers and numbering.

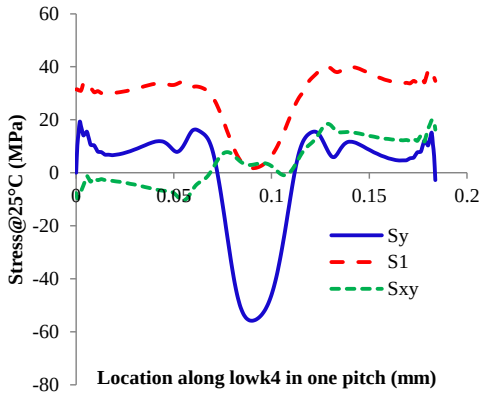



Fig. 7. Low-k layer stress at 25°C after TCB process.

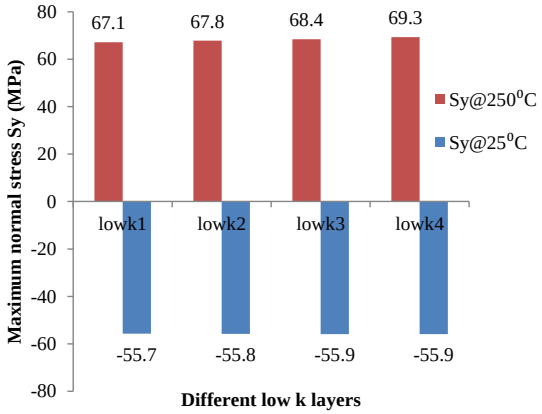
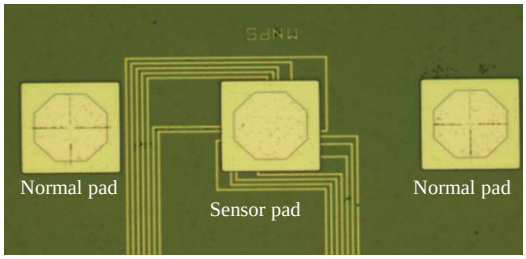



Fig. 8. Maximum stress comparison for different low-k layers at 250°C and 25°C.

## IV. Validation of TCB Process Modeling

In order to validate the TCB process FEA modeling results, the piezoresistive stress sensors were designed under the bond pad on a (100) p-type wafer to in situ measure the stresses during TCB assembly process. There are totally 8 sensors in a tested pad with 4 n-type (0° and 90° orientation) and 4 p-type (45° and 135° orientation) piezoresistive resistors. The effective length of the sensor is 12 µm and the width is 1.2 µm. The stress sensors were fabricated on 8-inch p-type wafer using 130 nm complementary metal-oxide-semiconductor technology with doping concentration about $10^{15}$ $cm^{-3}$ [15]. Fig. 9 (a) shows the stress sensors fabricated beneath an Al bond pad. The resistance of sensors will change due to stresses induced by TCB bonding process. The relationship between resistance change and stress can be used for stress calculation and analysis. Stress measurement and analysis have been successfully demonstrated in our previous work for wire bonding modeling validation [16].

Prior to the stress sensor chip being attached on a substrate, the connections for stress sensor measurement were routed out from each tested pad to adjacent bond pads, which were then connected to pads on substrate for electrical current sourcing and output measurement as shown in Fig. 9 (b). TCB bonding process induced stresses change the resistance of sensors which can be captured through an in-situ measurement system. Before the solder joints were formed, it is difficult to measure resistance change because the circuit closed loops were not formed between sensor chip and substrate. This is a challenge to link exact bonding time to bonding temperature. The TCB process was repeated 3 times to compare the measurement results. The good repeatability was achieved based on measurement data. Fig. 10 shows the stress change with adjusted bonding process time. The maximum stress occurs at the peak temperature. Then stress reduces with cooling down to substrate temperature about 80°C, at which in-situ measurement was stopped.




(a)

(b)

Fig. 9. Stress sensor and measurement (a) stress sensor fabrication under bond pad and (b) stress measurement.

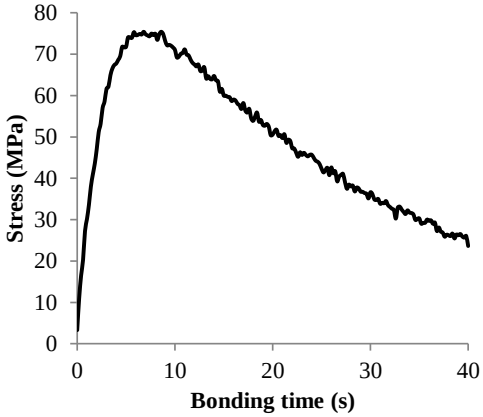



Fig. 10. Stress measurement during TCB process.

Because the sensors were fabricated at silicon surface through implant process, the simulation stress was obtained from the same location of sensor chip. Averaged stress based on the area of sensor was calculated for comparison. In the TCB process modeling, separate key temperature points, not real process time, were simulated. Therefore, stress measurement and simulation results cannot be directly compared based on the same scale. Fig. 11 shows the simulation stress at different bonding temperatures. Through comparison of stress between measurement and simulation results, it can be seen that the peak stress value and the trend of stress changing with temperature are consistent. The validated TCB process modeling method was then used for optimizing Cu pillar design and CPI study.

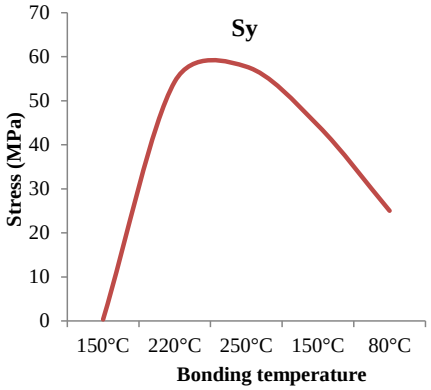



Fig. 11. Simulated stress at different bonding temperatures.

## V. Results and Discussion

### A. Effect of Bonding Pressure

Bonding pressure used in the TCB process is to ensure no cold joint and make underfill flow. The selection of bonding pressure is critical for the successful TCB process. In this study, the effect of bonding pressure on low-k stress and package warpage was investigated through the numerical simulation. Three cases were studied including 0, 2.5, and 5MPa bonding pressure. The simulation results show that the final package warpage at 25°C is almost the same for three cases because the bonding pressure is released during the cooling stage. The effect of bonding pressure on the maximum low-k stress as shown in Fig. 12 is not significant. Therefore, the bonding pressure can be ignored in the numerical simulation for the TCB process without loss of accuracy in terms of low-k stress and package warpage.

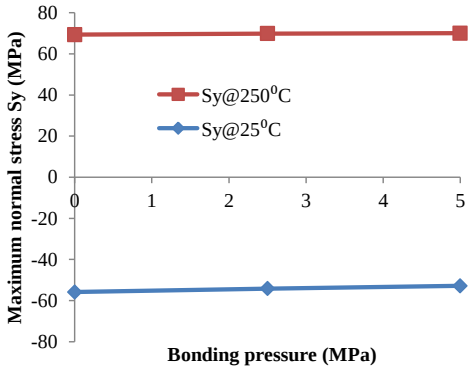



Fig. 12. Effect of bonding pressure on low-k stress.

### B. Effect of Assembly Process

The TCB process and reflow process were simulated for comparison. For reflow process simulation, all the materials have the same temperature condition (isothermal condition) and the temperature variation from reflow temperature (250°C) to room temperature was simulated. Three steps were simulated for reflow process: 1st step from 250°C to 25°C without underfill (UF), 2nd step from 25°C to 150°C for underfilling and underfill curing, and 3rd step from 150°C to 25°C. Fig. 13 shows the low-k stress at 25°C after 1st and 3rd steps. The 1st step is more critical for reflow process with higher low-k stress because underfill is not applied in this step. It can be seen that the stress distribution at low-k layer as shown in Fig. 14 is different for reflow and TCB process. The reflow process induced higher low-k stress than the TCB process. Fig. 15 shows the warpage results for both TCB and reflow processes. The TCB process reduces package warpage significantly compared to the reflow process.

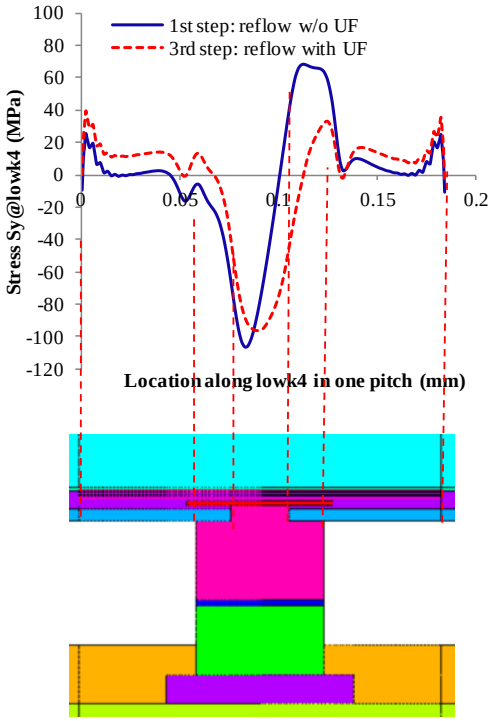



Fig. 13. Low-k layer stress under reflow process.

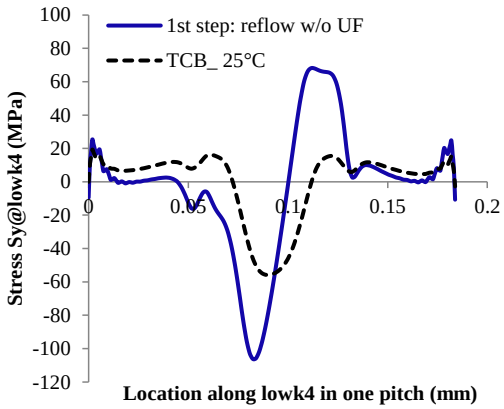



Fig. 14. Low-k layer stress induced by TCB and reflow processes.

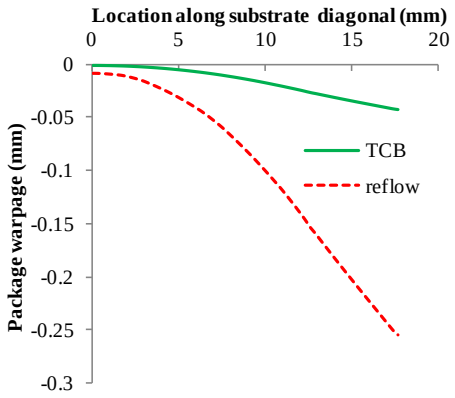



Fig. 15. Package warpage after TCB and reflow processes.

*C. Effect of Substrate Core Thickness and CTE*

Two substrate core thicknesses, 400 µm and 800 µm, were simulated for both TCB and reflow processes. Fig. 16 shows the effect of substrate core thickness on package warpage. Thicker substrate core leads to lower warpage for both TCB and reflow processes because thicker core provides stiffer structure, which makes package deform more difficultly. Fig. 17 shows the effect of substrate thickness on low-k stress. The effect of substrate thickness on low-k stress is not significant. Reflow process induces larger compression stress than TCB process.

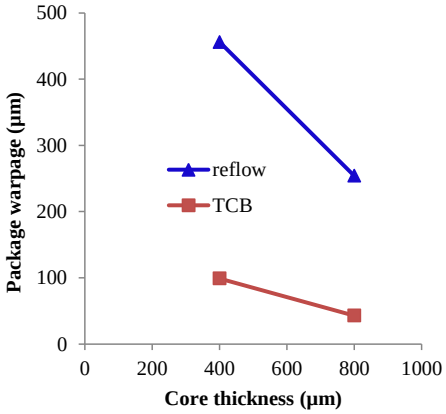



Fig. 16. Effect of core thickness on package warpage.

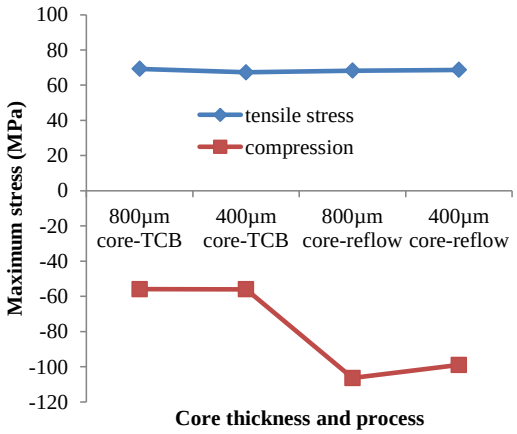



Fig. 17. Effect of core thickness on low-k stress.

CTE is a very important parameter for substrate material affecting package warpage and low-k stress. Substrate core CTEs of 3, 7, 10, and 15ppm/°C were simulated. Figs. 18 and 19 show the effect of core CTE on package warpage and low-k stress, respectively. Package warpage increases significantly with increasing core CTE for both TCB and reflow processes. Lower core CTE leads to smaller substrate deformation, which is compatible with low CTE chip deformation and thus reduces package warpage. The effect of core CTE on package warpage in the reflow process is more significant compared to its effect in the TCB process. In the reflow process, all package materials are subjected to the same temperature profile, which makes CTE mismatch (between the chip and substrate) induced package warpage larger than that in the TCB process in which the substrate is under lower temperature load than the silicon chip. Low assembly temperature of substrate leads to approximately consistent deformation between the substrate and chip when the package is cooled down to ambient temperature. Therefore, TCB process induces lower package warpage than reflow process. Low-k stress increases significantly with increasing core CTE for reflow process. Large low-k stress may cause brittle failure or delamination of low-k layers. However, the effect of core CTE on low-k stress is not significant for TCB process. Therefore, the TCB process is a desirable assembly method for low-k chip with fine pitch Cu pillar bumps compared to reflow process in terms of reducing package warpage and low-k stress.

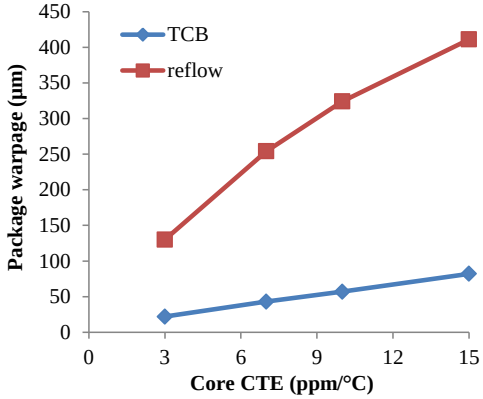



Fig. 18. Effect of core CTE on package warpage.

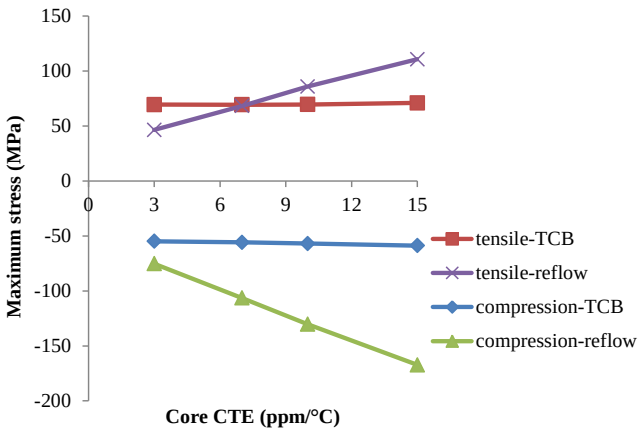
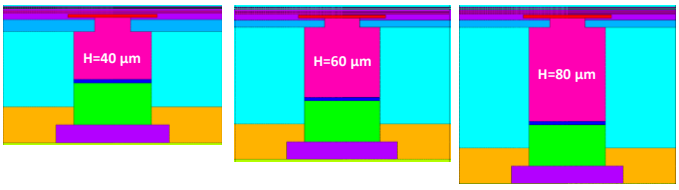



Fig. 19. Effect of core CTE on low-k stress.

*D. Effect of Cu Pillar Height*

Cu pillar height of 40, 60, and 80 µm were simulated as shown in Fig. 20. For different Cu pillar height models, the same solder joint height of 20 µm was modeled. The effects of Cu pillar height on package warpage and low-k stress are shown in Figs. 21 and 22, respectively. Warpage reduces slightly with increasing pillar height. However, the maximum low-k stress increases with increasing Cu pillar height for both TCB and reflow processes. Lower Cu pillar height is preferred for improving low-k chip reliability and reducing CPI concerns.




(a) (b) (c)

Fig. 20. Different Cu pillar height models (a) 40 µm, (b) 60 µm and (c) 80 µm.

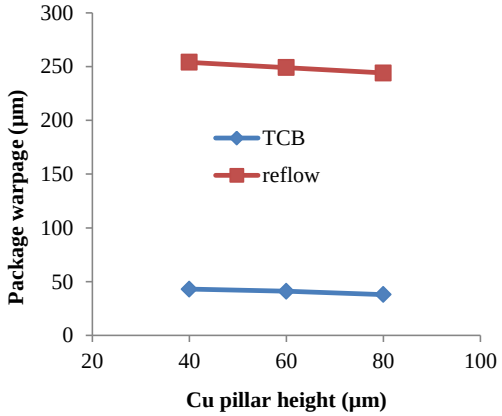



Fig. 21. Effect of Cu pillar height on package warpage.

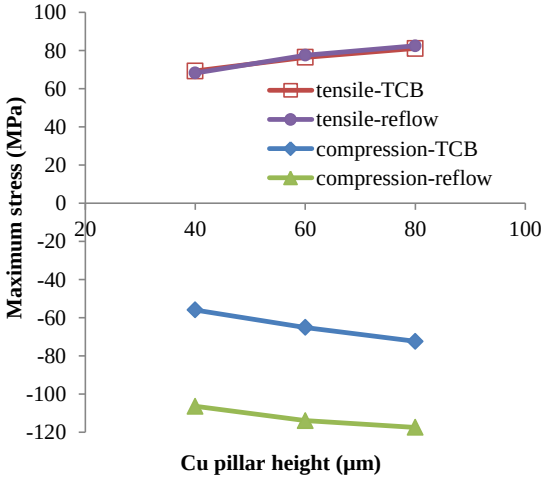



Fig. 22. Effect of Cu pillar height on low-k stress.

*E. Effect of Ratio of Cu Pillar to Solder Height*

The total height of Cu pillar and solder joint keeps a constant of 60 µm. The ratio of Cu pillar to solder joint height, 1.5, 2, and 3, were simulated and its effect on low-k stress is shown in Fig. 23. Low-k stress slightly increases with increasing ratio. Higher solder joint (lower ratio) helps reduce low-k stress because it provides more flexible joint structure. Because the total height of joint structure is the same, the package warpage is almost the same for different height ratios.

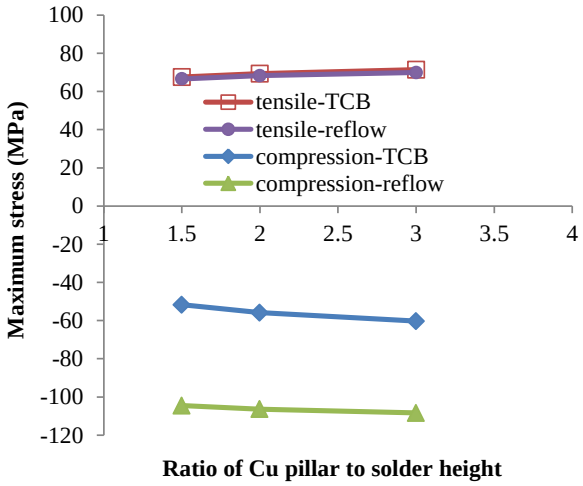



Fig. 23. Effect of ratio of Cu pillar to solder bump height on low-k stress.

*F. Effect of Die Thickness*

Die thicknesses, including 150, 300, 500, and 750 µm, were simulated and its effects on package warpage and low-k stress are shown in Figs. 24 and 25, respectively. For reflow process, thicker die helps to reduce package warpage. However, the effect of die thickness on package warpage is not significant for TCB process. Reflow process induced low-k stress increases with increasing die thickness. Low-k stress slightly reduces with increasing die thickness for the TCB process. Therefore, package warpage and low-k stress are more sensitive to die thickness when using the reflow process for assembly compared to TCB assembly process.

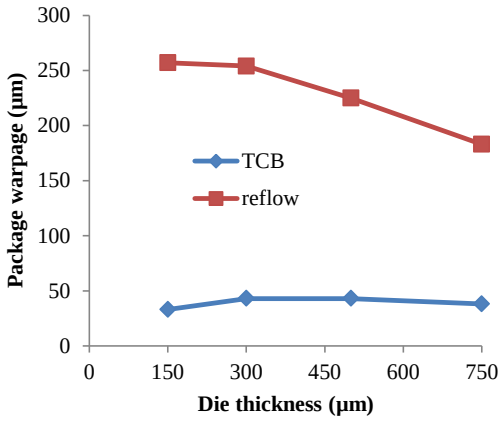



Fig. 24. Effect of die thickness on package warpage.

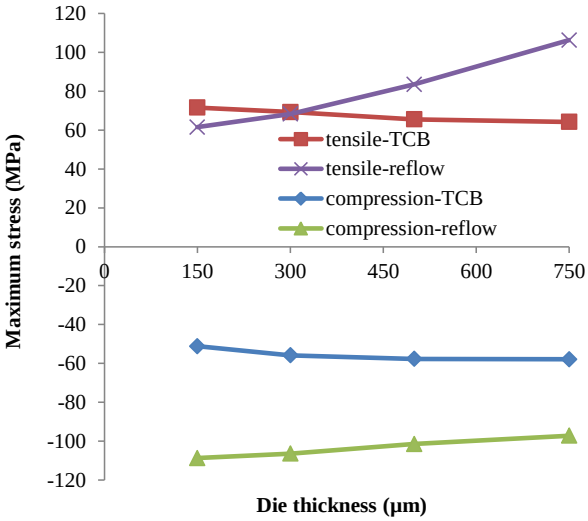



Fig. 25. Effect of die thickness on low-k stress.

*G. Effect of Photo Dielectric Opening*

Photo dielectric (PD) openings of 20, 30, and 40 µm as shown in Fig. 26 were simulated and its effect on low-k stress is shown in Fig. 27. For TCB process, the maximum low-k stress decreases with increasing opening. For reflow process, the maximum low-k stress increases with increasing opening. The effect of photo dielectric opening on overall package warpage is not significant.

(a) (b) (c)

Fig. 26. Different photo dielectric opening models (a) 20 µm, (b) 30 µm and (c) 40 µm.

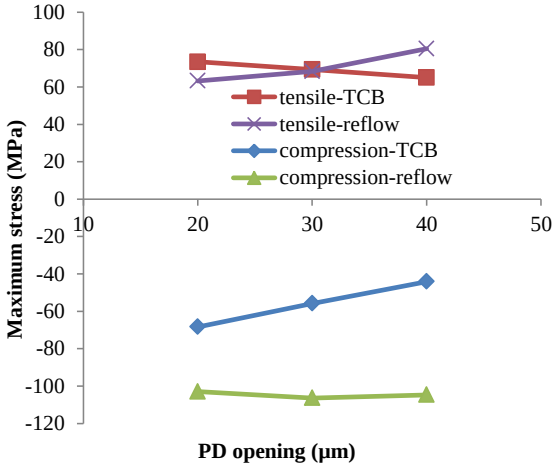



Fig. 27. Effect of photo dielectric opening on low-k stress.

*H. Effect of NCP Material*

NCP as an underfill material was used to prevent low-k layer from fragile cracking during TCB assembly process. The partially cured NCP during TCB process reduces thermo-mechanical stress induced by CTE mismatch between the chip and the substrate. Selection of NCP material is important for low-k chip assembly to overcome CPI challenges. In this study, three different NCP materials as listed in Table II were investigated through FEA modeling. NCP-1 has the lowest CTE and the highest Young's modulus than NCP-2 and NCP-3. Fig. 28 shows the effect of NCP material on low-k stress. NCP-1 leads to the highest tensile stress while NCP-3 leads to the lowest tensile stress. In the TCB process, the maximum tensile stress of low-k layer occurs at peak temperature. NCP-3 is the softest material with very low modulus compared to the other two NCPs so that NCP-3 leads to the lowest tensile stress on low-k layer. However, NCP-3 leads to the highest compression stress when package was cooled down to room temperature due to its highest CTE below glass transition temperature (Tg). Based on simulation results, an ideal NCP material used in the TCB assembly process could be with lower CTE below Tg and lower modulus above Tg to reduce low-k stress and CPI risks.

TABLE II
MATERIAL PROPERTIES OF DIFFERENT NCP MATERIALS

| Materials | CTE (ppm/°C) CTE1/CTE2 | Young's modulus (GPa) E1/E2 | Poisson's ratio | Tg (°C) |
|---|---|---|---|---|
| NCP-1 | 27.2/63.3 | 10.8/1.6 | 0.3 | 177 |
| NCP-2 | 35/110 | 7.4/0.22 | 0.3 | 180 |
| NCP-3 | 79/217 | 2.54/0.023 | 0.3 | 150 |

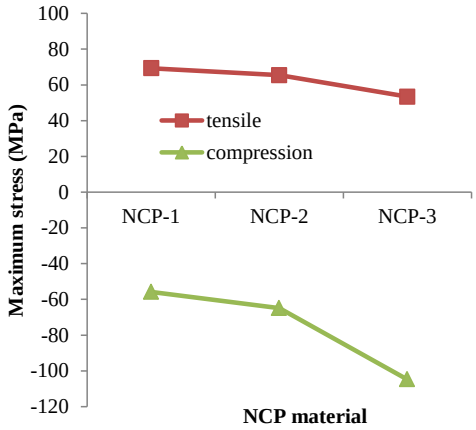
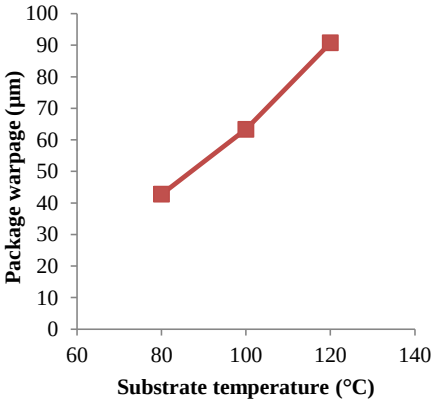



Fig. 28. Effect of NCP material on low-k stress.

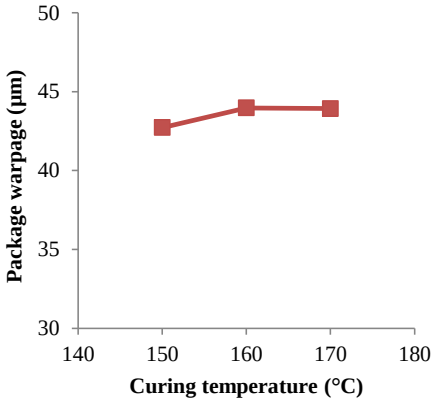
*I. Effect of TCB Bonding Condition*

In the TCB process, substrate temperature, underfill temporary curing temperature and chip temperature can be controlled separately. TCB bonding condition was optimized through FEA modeling to reduce low-k stress and package warpage. Figs. 29 and 30 show the effects of bonding temperatures on low-k stress and package warpage, respectively. Package warpage increases significantly with increasing substrate temperature, while the maximum low-k stress decreases with increasing substrate temperature. Both package warpage and low-k stress increase with increasing underfill curing temperature, but not significantly. The effect of chip peak temperature on final package warpage is very small, while the maximum low-k stress increases with increasing chip peak temperature. Based on the simulation results, lower substrate and chip temperature should be adopted. Finally, substrate temperature of 80°C, underfill

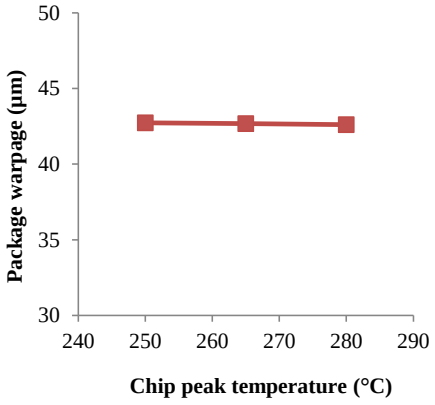
temporary curing temperature of 150°C and chip peak temperature of 250°C were applied in the TCB bonding process for Cu pillar interconnection assembly. A good bonding quality for Cu pillar interconnection as shown in Fig. 2 was achieved. All assembled packages passed time zero electrical continuity test and preliminary reliability test under moisture sensitivity level 3 (MSL3) conditions [13]. Temperature cycling (TC) reliability test with range from -40°C to 125°C was also conducted for Cu pillar jointed packages. The TC test results showed that all packages passed 1000 cycles.




(a)

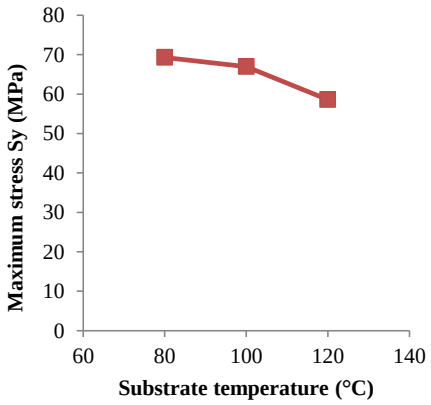



(b)

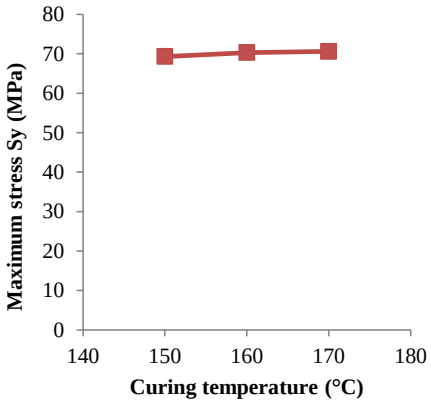



(c)

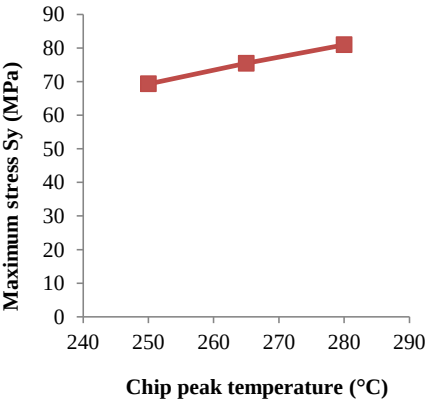
Fig. 29. Effect of bonding condition on package warpage (a) substrate temperature, (b) NCP curing temperature and (c) chip peak temperature.




(a)




(b)




(c)

Fig. 30. Effect of bonding condition on low-k stress (a) substrate temperature, (b) NCP curing temperature and (c) chip peak temperature.

## VI. Conclusion

TCB process modeling methodology was demonstrated and validated in this study. Comparison between TCB and reflow processes was also carried out. It is shown that TCB process is a desirable assembly method for low-k chip assembly with fine pitch Cu pillar interconnection. Parametric studies were conducted for TCB process using FEA simulation to optimize package design, material selection and process condition. The final packages were assembled with Cu pillar interconnection using TCB process and high package reliability was achieved. Some results and conclusions were summarized as below:

1) TCB process induced package warpage increases with increasing substrate core CTE and decreasing core thickness. Low-k stress increases significantly with increasing core CTE when using reflow process, but stress is not sensitive to core CTE when using TCB process. Therefore, thick and low CTE core is recommended to improve reliability of low-k chip assembly.

2) Shorter Cu pillar and smaller ratio of Cu pillar to solder height result in lower low-k stress.

3) Low-k stress and package warpage are less sensitive to die thickness when using TCB process for assembly compared to conventional reflow process. Thicker die leads to smaller warpage and lower low-k stress for TCB process. Package warpage decreases but low-k stress increases with increasing die thickness when using reflow process.

4) Photo dielectric opening shows different effects on low-k stress for TCB and reflow processes. Larger opening design is optimal when using TCB process for assembly.

5) NCP underfill material with lower CTE below Tg and lower modulus above Tg is recommended to reduce low-k stress induced by TCB assembly process.

6) In order to reduce package warpage and low-k stress, TCB bonding process using slightly lower substrate temperature is recommended.

## ACKNOWLEDGMENT

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