Failure Mechanism for fine pitch micro bump in Cu/Sn/Cu system during Current Stressing

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Abstract

Current-induced failures in fine pitch Sn micro bump with Cu pillar have been investigated under a current density of 3.2×10^4 A/cm^2 and temperature of 150°C. This process takes place in 2000 hours of electromigration test. From the FIB image and EDX analysis we observed the intermetallic compound formation, kirkendall effect, and crack contributed to this failure. There are two stages failure process for Cu pillar with micro-bump during current stressing. In first stage, the whole Sn solder was transformed into intermetallic compound and kirkendall voids were formed at the interface between the Cu pillar and Cu_3Sn intermetallic compound. In second stage, the Kirkendall voids coalesced into larger porosities then formed continual crack by current stressing, leading more bump resistance increase.

I. Introduction

The electromigration reliability of chip to package interconnects has become a major concern due to potential elimination of Pb from flip chip bumps, increased IO density resulting in smaller and finer pitch bumps, TSVs, RDL, and microvias.[1-6] At the same time, the increase in power density and higher power applications requires chip-to-package interconnects to carry more current per interconnect. With the bump size significantly smaller than C4 solder joints and the need to increase the current density, electromigration (EM) has emerged as a critical reliability concern and has drawn considerable interest.[7-11] Cu pillar bumps are known to be one of the most promising candidates for the interconnection materials.[12] Also, Cu pillar bump is widely adopted as chip-to-substrate interconnects in 3D integration as well as Flip chip package.[13] Only a few studies have reported regarding the EM for solder joint with Cu pillar.[14-16] However, it is not clear what is the EM failure mechanism of fine pitch micro-bump with Cu pillar. In this study, EM test of Cu pillar with Sn cap interconnection with a fine pitch of 40 μm was conducted. The micro-bump structure consisted of Sn solder with 20 μm Cu pillar. Four-point probe measurement was implemented to detect the small resistance changes of micro-bumps since the resistance changes were very small. We provide the failure mode of fine pitch micro-bump with Cu pillar.

II. Experimental set-up and procedure

The test structures comprised an 8 mm square silicon die flip chip mounted using Cu pillar technology on a 14 mm square, 250μm thick substrate. The die has one Al metal layer and SiO_2/Si_3N_4 passivation. The solder-capped Cu pillar micro-bumps are formed on Al pads around the peripher of the die. There are 664 bumps on a pitch of 40 μm. The chip with the solder-capping Cu pillar micro-bumps is aligned with the substrate after which the micro-bumps are all formed. The underfill material is then filled into the gap between the chip and the substrate. The top chip and bottom substrate were assembled using thermo-compressive bonding. After assembly, the structure of Cu pillar micro-bumps, as shown in Fig. 1, consisted of Cu pillar on UBM/ Sn solder/Cu trace on substrate. The UBM on die chip side and Cu pillar (diameter 20 μm), were deposited through electroplating. Aluminum traces, 20 μm wide and 2 μm thick, provide connection between micro-bumps. Before assembly the tin layer on top of the Cu pillar was about 12 μm thick. The contact opening at the base of the Cu pillar had a diameter of 10 μm. The dimension of Cu trace on the substrate side is 20 μm wide and 15 μm thick. We have designed and fabricated 4-wire measurements resistance for Cu pillar with Sn solder micro bump. Fig. 2 shows the schematic representation of EM test system during EM tests with current density of 3.2×10^4 A/cm^2 [17]. EM tests were performed by placing the samples in a furnace at 150 °C. Constant direct current of 100mA (DC) was applied, and the resistance change over time was recorded using a voltmeter connected to a switch matrix and computer for data acquisition. To minimize the noise of resistance variation from connecting wires, four-point probe measurement was employed on the test structure. The average current density was calculated based on the applied DC current divided by the area of the UBM opening of the micro-bump. The arrows depict the electron flow direction. After EM tests, the samples were ground with SiC papers down to 2500 grit and then polished progressively with 0.1 and 0.05 μm Al_2O_3 powders. The microstructural changes and phase identification of the cross-sectioned micro bumps were observed using focused ion beam (FIB) and energy dispersive x-ray analysis (EDX), and for materials characterization. Failure modes were identified by examining the resistance traces. The neighboring micro bumps subject only to thermal annealing, were also cross-sectioned to investigate intermetallic growth, interfacial reaction, and void formation.

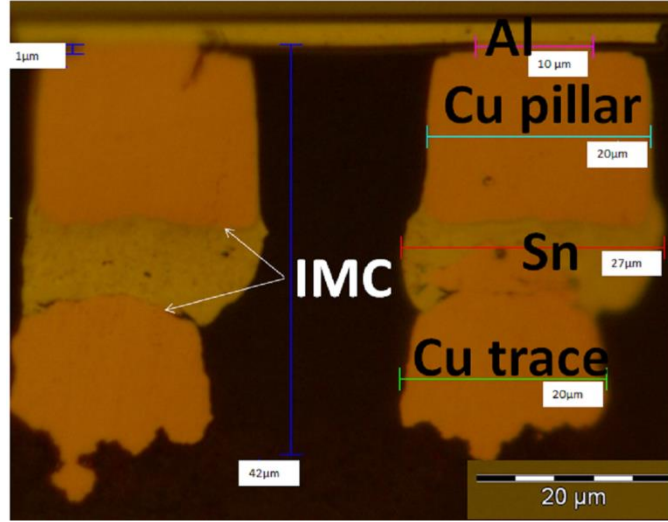


Fig.1. The cross section view of Cu pillar with micro-bumps.

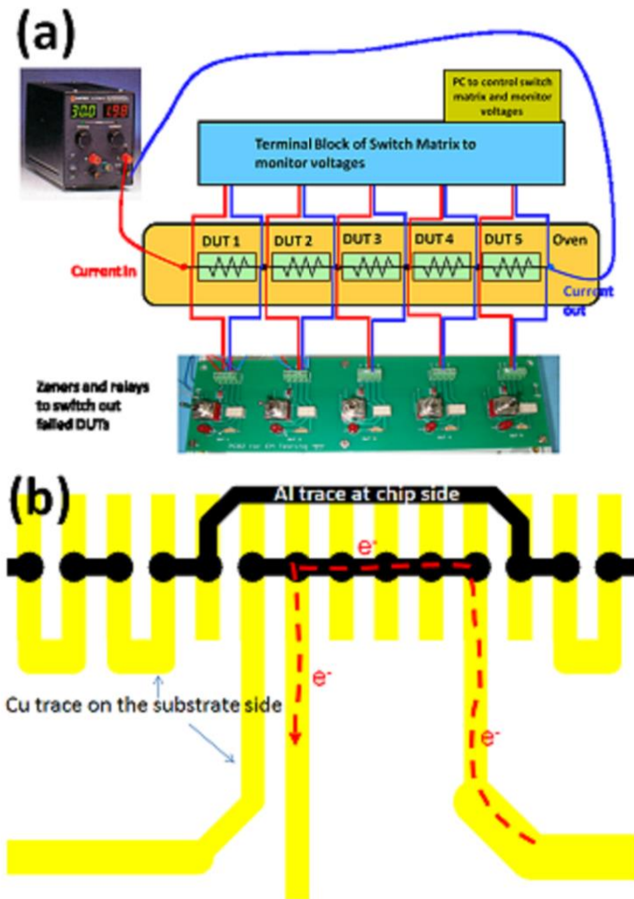
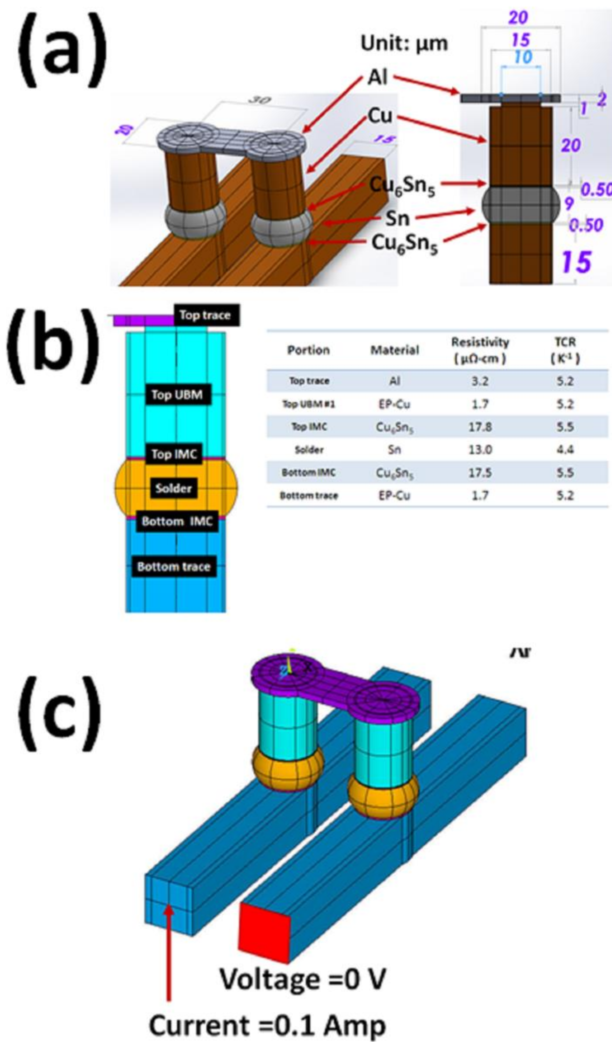


Fig.2. (a) Schematic representation of EM test system.

(b) The layer out of the single bump test structure.

A 3D finite element simulation using numerical analysis methods with the ANSYS finite element analysis software was conducted to determine the current density and temperature distribution in the Cu pillar micro-bumps. Results from these analyses were used to evaluate the EM reliability of the Cu pillar micro-bumps. The constructed model for the package is shown in Fig. 3. Constant electric current was applied on only two of the micro-bumps through the circuit shown in Fig. 3(a). The interfacial intermetallic compounds on the chip and on the substrate sides were omitted. The electrical resistivity for the materials used in this modeling is showed in Fig. 3(b). The effect of temperature coefficient (TCR) was considered in the simulation. The TCR values of the metals used in this simulation were assumed to be linear and the values were tabulated in Table. The 3-D electric solid element analysis using ANSYS was conducted to predict the steady-state current density distribution. The model used in this study was a SOLID69 eight-node hexahedral coupled field element. All the boundary conditions were followed the experiment setup, as shown in Fig. 3(c). For the electric boundary conditions, a constant current was applied through the Cu line in the substrate side and the Al or Cu trance in the chips side.



Portion	Material	Resistivity (μΩ-cm)	TCR (K^{-1})
Top trace	Al	3.2	5.2
Top UBM #1	EP-Cu	1.7	5.2
Top IMC	Cu_6Sn_5	17.8	5.5
Solder	Sn	13.0	4.4
Bottom IMC	Cu_6Sn_5	17.5	5.5
Bottom trace	EP-Cu	1.7	5.2

Fig.3. (a) Schematic drawing of the micro-bump with Cu pillar UBM used in this study. (b) Cross-sectional schematic of the micro-bump used in this study, showing the materials and the dimension of the micro-bump. (c) Three dimensional view of the constructed model and shows the boundary conditions.

III. Results

Electromigration test was performed to investigate the effect of current stressing. IMC were formed by Cu and Sn reaction. Kirkendall voids and continue cracks were observed at the interface of Cu pillar and Cu_3Sn IMC. Fig. 4 (a)-(f) shows the cross-sectional FIB images of the micro-bump after current stressing of 3.2×10^4 A/cm^2 at an oven temperature of 150°C with resistance increased by 141% compared to its original value. Fig. 4 (b),(d) and (e) present an enlarged images of Cu pillar with micro bump upon stressing, showing Kirkendall voids and continuous cracks were clearly observed on the chip side. Fig. 4 (a)-(b) display the micro-structure of the micro-bump with electron flow down after current stressing of 2000 h. The Cu pillar was consumed significantly on the chip side. The thickness of Cu pillar decreased from 20μm to 7μm.The whole micro-bump experienced phase transformation into Cu_3Sn IMC during EM tests. On the chip side, we found continuous crack between Cu pillar and Cu_3Sn IMC after electromigration test.

Fig. 4(c)-(d) shows the cross-sectional FIB image of the micro-bump with electron flow up after current stressing. Similar to the FIB image as shown in Fig. 4(a)-(b); the Sn inside the whole micro-bump was totally transformed to Cu_3Sn IMCs. We also found crack in the Cu_3Sn IMC and Cu/Cu_3Sn interfaces. These cracks will cause the micro bump to fail. Fig. 4(e)-(f) presents FIB images for micro-bumps without current stressing (no current at all). The interfacial reaction resulted in a fully converted Cu_3Sn IMC bump. Kirkendall voids were observed in thermal aging under EM test process. It is reasonable that the Cu_3Sn IMC and Kirkendall voids formation under longer isothermal aging time. Due to Kirkendall voids accumulation when stressing time increased, a number of small voids can be observed both at Cu_3Sn/Cu interface and inside the Cu pillar layer.

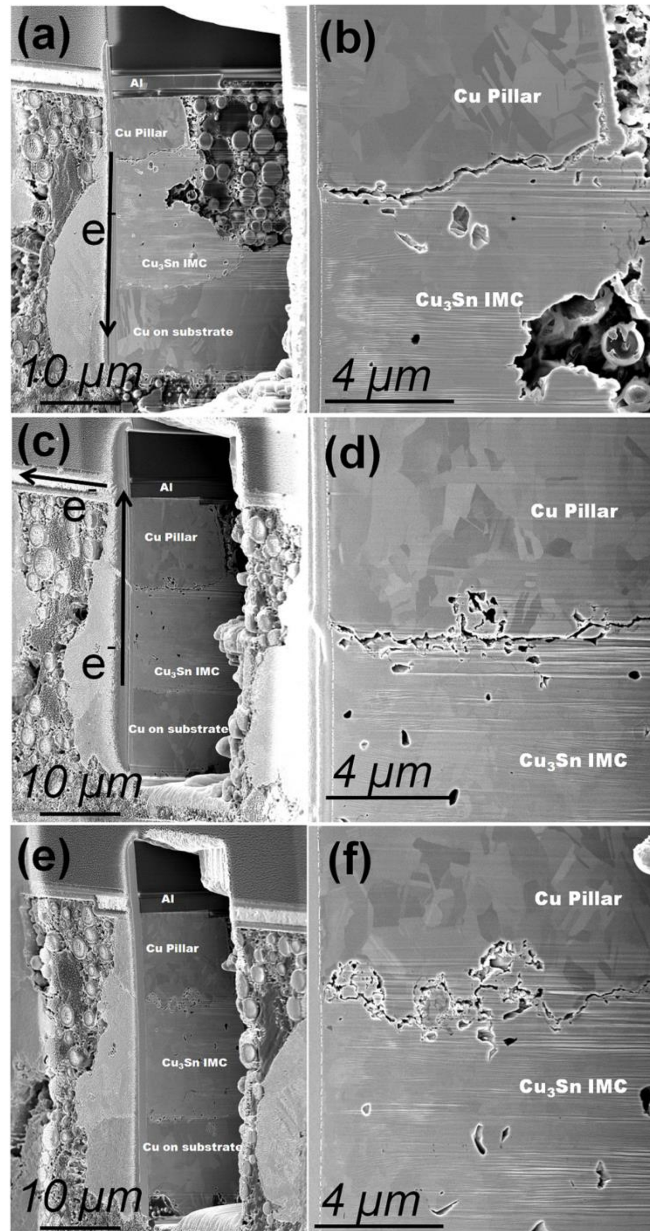


Fig.4. Cross-sectional SEM images of micro-bump after current stressing with 100 mA at 150°C with (a)-(b) downward electron flow (c)-(d) upward electron flow, and (e)-(f) thermal reference bump without stressing.

IV. Discussion

It has two stages bump resistance variations during electromigraiton test. Fig. 5 shows the bump resistances change with time for micro-bump with Cu pillar structure. For this case, the initial bump resistance was 38.0 mΩ. After 1000 h, the bump resistance slowly increased to 41.5 mΩ. There was a long time with little resistance change within 50% of the stressing time; this period is denoted as first stage. It has low resistance variation which was less than 10%. This stage is chemical force dominates and causes IMC grow so bump resistance slowly increased. By Pouillet's law ($R=\rho L/A$), the resistance of a given material will increase with the length, but decrease with increasing cross-sectional area. When the solder fully transform to IMC joint, the resistance change is about 10% by calculated. It matches the experimental result. Therefore, even the phase change of the IMC has little impact on the resistance change of the micro-bump. Furthermore, the Sn solder fully transformed to Cu_3Sn IMC as the bump resistance increased 10% by calculation. Therefore, the Sn was exhausted then Cu_3Sn IMC bump formed in this stage.

After first stage, the bump resistance began to rise with a greater rate in the secondary stage. This stage lasted for 1000 h, and bump resistance reached 91.6 mΩ at 2000 h. It has linearly increased in bump resistance; with resistance increased the value is about 141% at termination of the test at 2000 h. The total bump resistance increased about 50 mΩ at this stage. The stage is electromigration force dominates that drives void growth at this time so resistance increases linearly. During second stage, these vacancies attract each other and congregate, then form microvoids, which coalesce into continue crack. Therefore, it can be seen that continue crack in Fig. 4(a)-(b) after 2000 h. The maximum length of the crack is about 10 μm between Cu pillar and Cu_3Sn IMC interface in the chip side. The crack significantly decreases the contact area of micro-bump. As the contact area decreased, the available cross section for conducting current became smaller, resulting in the increased bump resistance.

Hence, the whole failure process during current stressing can be described as follows: Firstly, Cu-Sn IMC formed and grew with increasing stressing time. Then complete consumption of the Sn solder to form fully Cu_3Sn IMC bump. Kirkendall voids occurred at the interface between the Cu_3Sn IMCs layer and the Cu pillar as expected. Secondly, the Kirkendall voids coalesced into larger porosities and continue crack during current stressing. With the formation of cracks, the contact area was decreased, which led to more bump resistance increased.

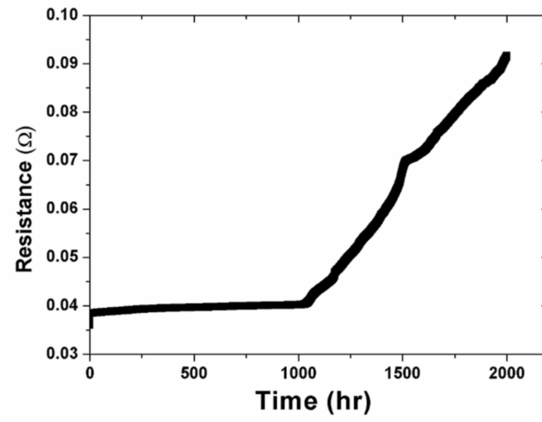


Fig.5.The bump resistance as a function of time when the micro-bump with Cu pillar was current stressed by 100 mA at 150 °C.

To investigate how void propagation influences bump resistances by simulation, a series of models with various sizes of voids were constructed. A three-dimension simulation model was created to analyze the current density distribution. Three-dimensional electrical simulation was carried out by finite element analysis to find out the current density redistributions in our test samples. In our samples, the diameters of the the Cu pillar UBM opening were 20 µm. Pancake-type voids were assumed to propagate along the interface between Cu pillar and Sn solder micro-bump. The shape of the void was assumed to be irregular. The depletion percentage of the Cu pillar opening is 10%, 50.0%, 60%, 75%, 90% and 94.3%, respectively, for the three models. As voids formed and propagated, more current was forced to drift longer to the right side along the Al pad and the Cu pillar UBM layer, causing the current density to redistribute. Fig. 6(a) shows the cross-sectional view of the current density distributions before void growth when 0.1 A was applied to the micro-bump. The numerical analysis results indicated that the maximum current density was generated at the corner of aluminum trace near copper pillar UBM, where the electron flow entered the corner and left. The maximum current density values in aluminum trace, Cu pillar UBM, and micro-bump, were $6.22x10^5$ A/cm^2, $7.33x10^5$ A/cm^2 and $1.27x10^5$ A/cm^2, respectively. The highest magnitude obtained was approximately 7.33×10^5A/cm^2, which is about six times higher than that in the solder. Fig. 6(b) shows the current density distribution in the full IMC bump without void formation when 0.1 A was applied. It is seen that the IMC thickness do not affects the current density distribution. The maximum current density value is the same. Due to the maximum current density occurs in the corner of Cu pillar UBM. Fig. 6(c) illustrates the current density distribution in the Cu pillar with micro-bump when a small void is formed near the entrance of the Al trace on the right-hand side. The void was then assumed to propagate to fill 10% of the Cu pillar UBM opening. The current redistributed due to void formation, however the maximum current density still occurred in the Cu pillar UBM near the upper right corner of the periphery of the Cu pillar UBM opening under the Al trace. Compared with that shown in Fig. 6(a), the maximum current density inside the solder has been increased to 2.14×10^5 A/cm^2 due to void formation. The void was then assumed to propagate to fill 50% of the UBM opening, as shown in Fig. 6(d). Since the Cu pillar/solder layers still serve as a current path, the void may be able to propagate to the edge of the solder bump. Therefore, we postulate that the growth of void in the low current density region under the periphery of the Cu pillar

opening is mainly attributed to current redistribution. The maximum current density inside the solder bump increased further to 5.10×10^5 A/cm^2 due to void formation. The void was then assumed to propagate to fill 60% and 75% of the UBM opening, as shown in Fig. 6(e)-(f). The current entered the solder joints through a smaller contact area, causing an increase in maximum current density. It raised to 5.33×10^5 A/cm^2 and 6.86×10^5 A/cm^2, respectively. However, the maximum current density still occurs in the Cu pillar UBM layer near the current into the Cu pillar UBM layer. The solder in the contact opening was completely depleted leaving a small amount of solder near the periphery of the Cu pillar UBM opening, as illustrated in Fig. 6(g)-(h). There were approximately 10% and 6.0% of contact area left for conducting the current. With further decrease in contact area, the maximum current density became 1.97×10^6 A/cm^2 and 2.53×10^6 A/cm^2, respectively. The maximum current density transfers to solder joint. The micro bump occurs seriously crowding in the current flows into the solder bump. The Cu pillar UBM/IMC layers served as a conducting path to direct the current to the remaining solder. Hence, the remaining solder near the periphery of the Cu pillar UBM opening could be completely depleted and failure followed.

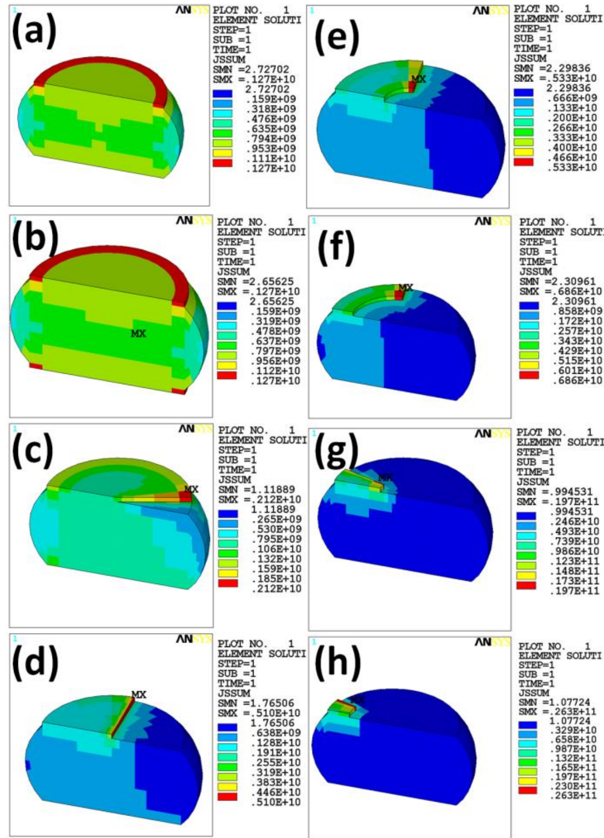


Fig.6. The cross-sectional view for five of the simulation models. The depletion percentage of the Cu pillar UBM opening is (a) 0%, (b) full IMC joint, (c) 10%, (d) 50%, (e) 60%, (f) 75%, (g) 90% and (h) 94%.

Our simulation shows that bump resistance increased slowly in the first stage, and then increased rapidly in the final stage which is close to the experimental values. Bump resistance was defined as the decrease in voltage between the entrance point of the Al trace into the Al pad and the junction point of the Cu line with the micro-bump. Fig. 7 shows the percentage increase in bump resistance vs depletion percentage of Cu pillar UBM opening. In initial stage, the solder joint transforms to full IMC joint. The bump resistance increased only 1.15 mΩ, which is about 10% increased of the initial value. The bump resistance increased from 13.4 to 16.0 mΩ. It increased to 20.2 and 31.3 mΩ in stages II and III, respectively. It rose to 40.0 mΩ in final stage. Nevertheless, the simulation value appears slightly lower than the experimental one, which may be attributed to that the void shape and area in the simulation models do not match the real ones perfectly. In addition, phase separation and IMC formation would affect bump resistance, but the simulation did not consider the two micro-structural changes. The bump resistance increased 141% of its original value after the stressing condition, as shown in Fig. 4(a). The depletion percentage of Cu pillar UBM opening was estimated to be 90% using the cross-sectional SEM image in Fig. 4(a). The simulated results in Fig. 6(g) indicate an approximate 90% of depletion percentage in length for the same increase in bump resistance.

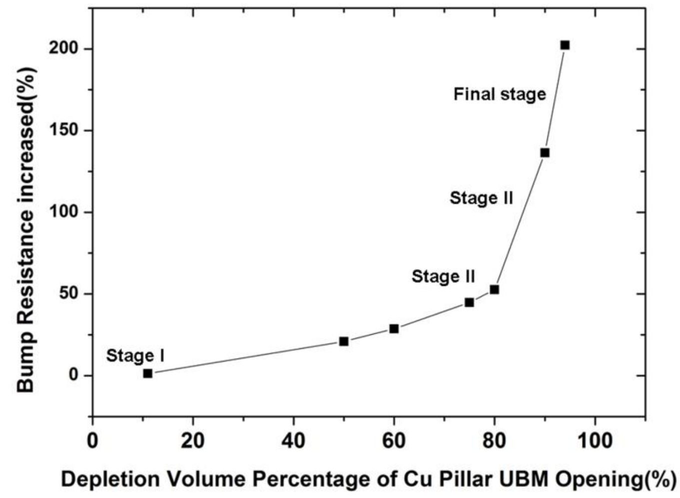


Fig.7. The percentage increased in bump resistance as a function of depletion percentage of Cu pillar UBM opening.

V. CONCLUSION

EM tests were performed on fine pitch Cu pillar with Sn micro-bumps for 3.2×10^4 A/cm^2 at 150°C. Results showed that the full conversion of the Sn micro-bump into Cu_3Sn intermetallic compound, Kirkendall voids and continue crack formed at the interface between the Cu pillar and Cu_3Sn intermetallic compound.

To conclude the results it can be found that there are two stages failure mechanism during the EM test process. The first stage is intermetallic compound formed and grew with increasing current stressing time. The time required for consumption of the Sn solder during the EM test process. This stage causes little impact on the electrical resistance during current stressing. In the second stage, the Kirkendall voids coalesced and continue crack by electron wind force. With the creation of crack, the effective contact area was decreased, which led to more bump resistance increased. The Kirkendall voids and crack that form during EM test degrade the mechanical and conductive properties for Cu pillar with micro-bump. Therefore, it can be considered a reliability issue for Cu pillar with micro-bump.

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