Structural Integrity of Three-dimensional Metal-insulator-metal (3-D MIM) Capacitor Embedded in Fully-filled Cu Through-silicon Via (TSV)

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***Abstract*—A novel way to implement integrated metal-insulator-metal (MIM) capacitor with ultra-high capacitance density of up to 5,621.8 nF/mm^2 has been proposed earlier. This technology embeds three-dimensional metal-insulator-metal (3-D MIM) capacitor into the existing trench of through-silicon via (TSV) prior to Cu filling to achieve > 90% planar surface area reduction. However, the previous study was on the early-stage test vehicles without Cu filling. In this work, the complete test vehicles with fully-filled Cu TSVs have been successfully fabricated whose trench diameters are 0 (D00), 10 (D10), 20 (D20), and 30 µm (D30), respectively. Firstly, the design layout and the process flow are disclosed in details. Then under scanning electron microscope (SEM) and transmission electron microscope (TEM), it is found that the peak of the Si scallop on the sidewall is deformed for the D30 test vehicle. For the first time, the damage is found in Si substrate, instead of TSV SiO_2 liner, due to the thermo-mechanical stress between the TSV Cu core and the surrounding structures. In addition, the Al_2O_3 dielectric layer is also impaired at the damaged Si peaks. Lastly, the leakage current density is measured and normalized at a bias of 1.5 V: 4.0 × 10^{-9} A/cm^2 for D00, 4.1 × 10^{-8} A/cm^2 for D10, 1.1 × 10^{-6} A/cm^2 for D20, and 7.4 × 10^{-1} A/cm^2 for D30, respectively. Therefore, the structural integrity of D10 and D20 test vehicles with fully-filled Cu TSVs is preserved, but the D30 test vehicle is not intact due to higher stress. Capacitance density of 6,547.1 and 7,091.7 nF/mm^2 is recorded for D10 and D20 test vehicles, respectively.**

***Index Terms*—integrated metal-insulator-metal (MIM) capacitor, through-silicon via (TSV), three-dimensional integrated circuit (3-D IC).**

I. Introduction

Researchers are actively exploring new approaches to integrate high density metal-insulator-metal (MIM) capacitors for the advanced integrated circuits (ICs) to realize smaller form factors, lower parasitics, and new on-chip functionalities. Trench MIM capacitor, also known as three-dimensional (3-D) MIM capacitor, is considered as one of the best technologies to boost the capacitance density of conventional planar capacitor, since it utilizes the third dimension of the substrate and therefore higher surface area can be utilized without planar area penalty [1]–[9].

The authors have proposed to embed the 3-D MIM capacitor in the trench of existing through-silicon via (TSV) to realize an ultra-high capacitance density of up to 5,621.8 nF/mm^2 [10]–[13]. The concept is shown in Fig. 1, in which the benefit of this technology is demonstrated by the area "freed-up" for other functionalities. However, the previous study was on the early-stage test vehicles without Cu TSV filling and therefore the effects of thermo-mechanical stress exerted by Cu core was not fully understood. Recently, Cu TSV filling has been completed and therefore making it a complete structure which contains both 3-D MIM capacitor and Cu TSV core.

In this study, firstly, the design layout of four different test vehicles and their process flow are disclosed in details. Then, the structure integrity of the test vehicles is inspected under scanning electron microscope (SEM) and transmission electron microscope (TEM). It is found that the periodic peaks of Si scallop on the sidewall are deformed in the trench with a diameter of 30 µm, whereas the peaks are intact in the trench with a diameter of 10 µm. The deformation is attributed to the residual thermo-mechanical stress between the TSV Cu core and the surrounding structures. In addition, the 10 nm Al_2O_3 dielectric layer is also impaired at the damaged Si peaks. Next, the results of *I-V* and *C-V* electrical characterizations are presented and discussed. The leakage current density at 1.5 V confirms that the structural integrity of the D10 and D20 test vehicles is preserved despite some thermo-mechanical stress, whereas the D30 test vehicle becomes very leaky. The values are 4.0 × 10^{-9} A/cm^2 for D00, 4.1 × 10^{-8} A/cm^2 for D10, 1.1 × 10^{-6} A/cm^2 for D20, and 7.4 × 10^{-1} A/cm^2 for D30, respectively. Additionally, record high capacitance densities of 6,547.1 and 7,091.7 nF/mm^2 are achieved for the D10 and D20 test vehicles, respectively.

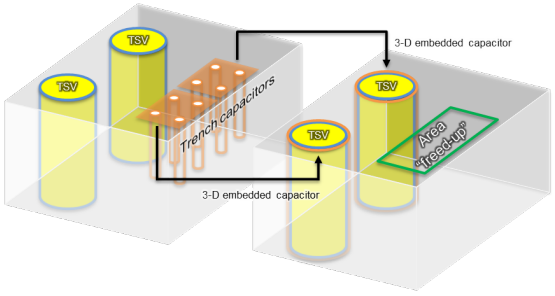

Fig. 1. The proposed 3-D MIM capacitor embedded in TSV. The top surface area is thus "freed-up" because the conventional trench capacitors are embedded in the trenches of existing TSVs.

II. Experiment

A. Design Layout

Four different layouts were designed for physical and electrical characterizations to assess the structural integrity of 3-D MIM capacitor embedded in fully-filled Cu TSV: (a) "D00" planar test vehicle is a de-embedded structure whose geometry is 180 µm × 400 µm; (b) "D10" embedded test vehicle contains one 3-D MIM capacitor in a TSV trench with a diameter of 10 µm; (c) "D20" embedded test vehicle contains a 3-D MIM capacitor in a TSV trench with a diameter of 20 µm; and (d) "D30" embedded test vehicle contains one 3-D MIM capacitor in a TSV trench with a diameter of 30 µm. The target depth of these trenches is 100 µm for all structures.

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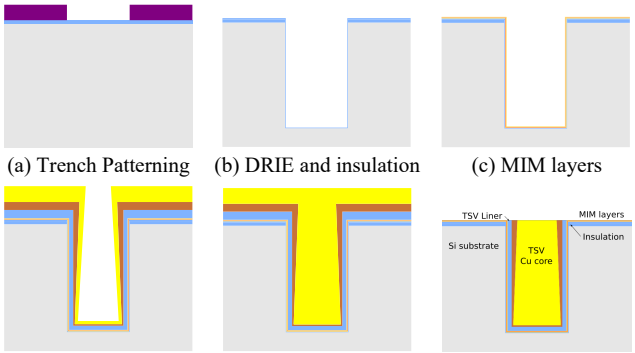
B. *Process Flow*

The process starts with a typical 1-10 Ω·cm 8-inch *p*-type Si wafer. Firstly, 200 nm SiO_2 was deposited on the wafer as hard mask, patterned by photoresist as shown in Fig. 2(a). Then deep reactive ion etching (DRIE) was done to form trenches and followed by 120 nm thick SiO_2 deposition as insulation layer between the bottom/outer electrode of MIM capacitor and the Si substrate as shown in Fig. 2(b). In Fig. 2(c), MIM layers (50 nm TiN/10 nm Al_2O_3/50 nm TiN) were deposited by atomic layer deposition (ALD) to ensure excellent step coverage and uniformity. Next, a stack of 200 nm SiO_2 TSV liner, 200 nm TiN diffusion barrier layer, and 1 µm Cu seed layer were deposited in sequence as shown in Fig. 2(d). Fig. 2(e) shows that Cu electroplating was done to fill up the TSV trench and the first round of chemical-mechanical polishing (CMP) was applied to remove the overburden until 1 µm Cu layer remained on top. After that, the wafer was annealed at 250°C and followed by the second round of CMP to remove the remaining Cu overburden expose the top/inner electrode. Lastly, the electrodes were patterned for electrical characterization as shown in Fig. 2(f). The summary of different layers is tabulated in Table I.



(a) Trench Patterning (b) DRIE and insulation (c) MIM layers

(d) Barrier and seed layer (e) Electroplating (f) CMP planarization

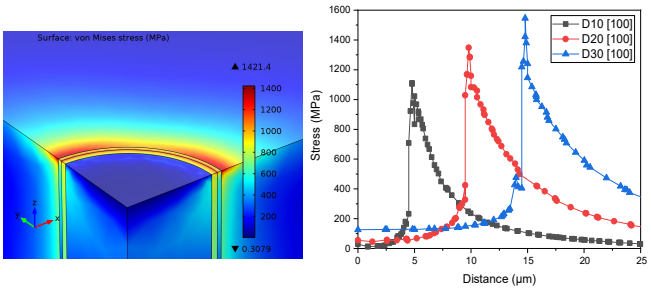
Fig. 2. The complete process flow of 3-D MIM capacitor embedded in fully-filled Cu TSV.

Table I Summary of different layers

Layer Name	**Thickness**
Hard mask SiO_2	120 nm
Insulator SiO_2	200 nm
Bottom electrode TiN	50 nm
Dielectric Al_2O_3	10 nm
Top electrode TiN	50 nm
TSV liner SiO_2	200 nm
Diffusion Barrier TiN	200 nm
Seed layer Cu	1 µm

C. *Thermo-mechanical modelling*

A simplified finite element model has been built in COMSOL to simulate the thermo-mechanical stress in the test vehicles as shown in Fig. 3(a), where the surface roughness of the Si substrate is not considered, and some thin layers are combined to reduce the complexity of meshing and computation. The x-axis points [100] direction; the y-axis points [010] direction; the z-axis points [001] direction. In Fig. 3(b), the peak stress level, along the Si [100] direction, increases from 1,110.6 to 1,285.6 to 1545.8 MPa as the TSV diameter increases from 10, 20 to 30 µm, respectively. It is worth noting that the peak stress resides in the neighboring Si substrate, which could potentially degrade its structural integrity for the test vehicle with larger TSVs.



(a) (b)

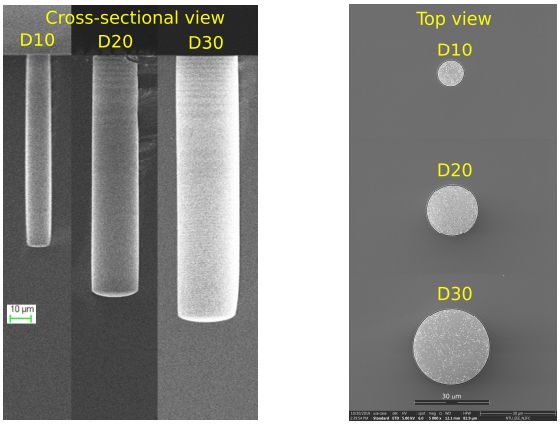
Fig. 3. COMSOL simulation: (a) a simplified finite element model was built to simulate the thermo-mechanical stress of all three test vehicles. (b). The stress level along Si [100] increases with larger TSV diameter.

III. Results and Discussion

The combination of physical and electrical characterizations are utilized to examine the structural integrity of 3-D MIM capacitors embedded in fully-filled Cu TSVs.

A. *Physical Characterization*

SEM and TEM were used to inspect the planar and cross-sectional views of the test vehicles. After the trench formation step, a wafer was cleaved to measure the geometries of all three trenches as shown in Fig. 4(a). The cross-sectional geometries of these trenches are 11.5 µm × 92.7 µm for D10, 21.8 µm × 114.4 µm for D20, and 30.2 µm × 128.1 µm for D30. The deviation in depth from the target 100 µm is caused by opening-dependent loading effect. Whereas in Fig. 4(b), the top view of D10, D20, D30 trenches after process is revealed from top to bottom in a row. This shows that all the trenches have been fully filled by Cu ECP and the Cu overburden have been completely removed by CMP successfully.



(a) (b)

Fig. 4. (a) The cross-sections of D10, D20, D30 trenches prior to filling. (b) The top view of D10, D20, D30 trenches after ECP and CMP.

Then, the cross-sections of D10 and D30 trenches (i.e., the smallest and the largest) were prepared using focus ion beam (FIB) for SEM/TEM inspection and comparison. In Fig. 5, the contrast is presented for D10 and D30 trenches before and after MIM and TSV filling. The white arrows in Fig. 5 (d) point to the locations are notably different in the D10 and D30. The numbers (1 to 6) labelled refer to the sidewall scallops induced by the Bosch process. The peaks in D10 are preserved, where the ones in D30 are deformed and form smaller scallops. To author's best knowledge, this is the first time that collapse of periodic Si peaks is observed. The collapse in D30 test vehicle is attributed to the high thermo-mechanical stress exerted by TSV Cu

core on the surrounding structures after the Cu annealing step. Previously, the impact of TSV thermo-mechanical stress only lies in the SiO_2 TSV liner and the surrounding strained devices (that necessitates keep-out zone), which have been reported in the literatures [14]–[18]. It is believed that the stacked 3-D MIM layers serve as the compliance layer and the stress is mostly concentrated on the scallops of the Si sidewall. In addition, the TEM zoom-in image in Fig. 6 shows that the Al_2O_3 dielectric layer is impaired at the location where the Si peak is damaged. The EDX results in Fig. 7 further confirms the separation of Al_2O_3 dielectric layer as two O peaks were detected distinctively. This observation is also in good agreement with the simulation results obtained earlier, suggesting that the 3-D MIM capacitor is compatible with the TSV whose diameter is below 30 µm to endure smaller residual thermo-mechanical stress.

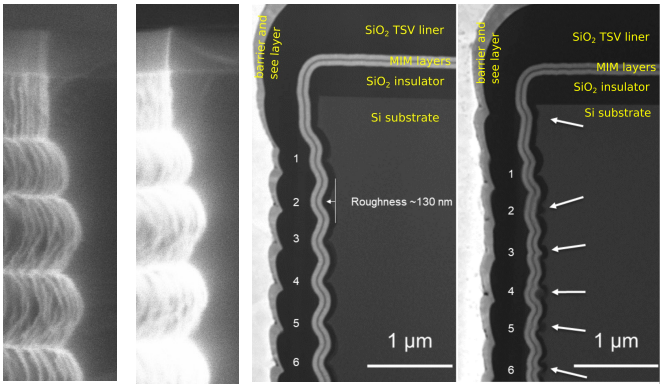


Fig. 5. The cross-sectional SEM images prior to MIM and TSV filling (a) D10 test vehicle, (b) D30 test vehicle; cross-sectional TEM images after MIM and TSV filling (c) D10 test vehicle and (d) D30 test vehicle.

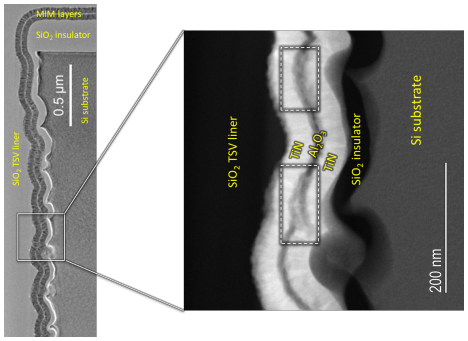


Fig. 6. The zoom-in TEM image of impaired parts of the Al_2O_3 dielectric layer located at the damaged Si peaks.

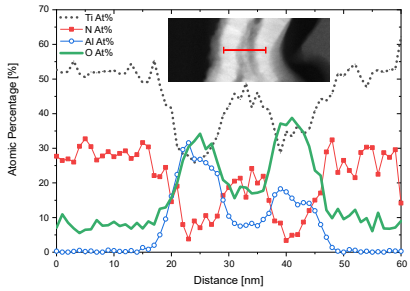


Fig. 7. Normalized *J-V* results with bias from 0 V to 3 V

B. *Electrical Characterization*

Current-Voltage (*I-V*) and Capacitance-Voltage (*C-V*) electrical characterizations were carried out in sequence to study the impact of the thermo-mechanical stress on their electrical performance.

Firstly, the results of *I-V* measurement are normalized to Current Density-Voltage (*J-V*) for fair comparison as shown in Fig. 8. It has been reported earlier by the authors that the D00, D10, D20, and D30 test vehicles without TSV Cu filling has negligible difference in leakage current density of ~1.0×10^{-9} A/cm^2 at 1.0 V [13]. In contrast, after TSV Cu filling, the leakage current density increases drastically as TSV diameter increases: at a bias of 1.5 V, the leakage current density is 4.0×10^{-9} A/cm^2 for D00, 4.1×10^{-8} A/cm^2 for D10, 1.1×10^{-6} A/cm^2 for D20, and 7.4×10^{-1} A/cm^2 for D30. This rapid increase is expected because the fully-filled TSV with larger diameter induces higher residual thermo-mechanical stress that affect the structural integrity of the MIM, and therefore leading to higher leakage current density. The D30 test vehicle is considered a failed device due to its extremely high leakage current density (eight orders more than that of the benchmark D00).

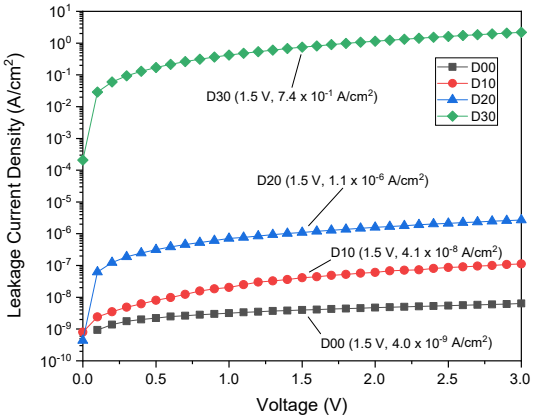


Fig. 8. Normalized *J-V* results with bias from 0 V to 3 V

Then the *C-V* measurement were taken for all four test vehicles with bias sweeping from -3 V to 3 V at 100 kHz. At the bias of 0 V, the capacitance is 592.7 pF for D00, 630.0 pF for D10, 669.8 pF for D20, and 721.8 pF for D30. The measurement results from D30 could be eliminated due to the extremely high leakage current density. The net capacitance contribution is 37.3 pF for a D10 trench and 77.1 pF for a D20 trench. It further translates to a record high capacitance density of 6,547.1 nF/mm^2 for D10 test vehicle, 7,091.7 nF/mm^2 for D20 test vehicle. Both *I-V* and *C-V* characterization results suggest the 3-D MIM capacitors work well with the integration of fully-filled Cu TSV in the 10 µm and 20 µm diameter trenches.

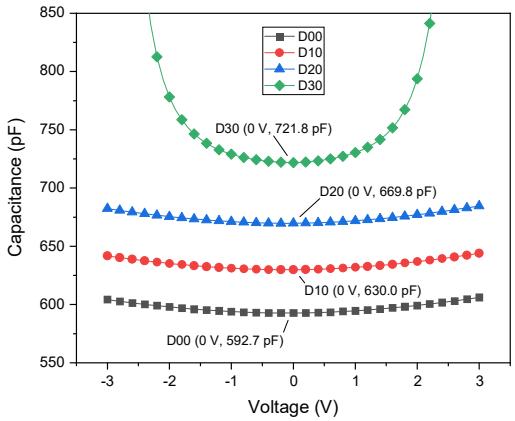


Fig. 9. *C-V* measurement results at 100 kHz with bias from -3 V to 3V.

IV. Conclusion

In conclusion, the 3-D MIM capacitors embedded in fully-filled Cu TSVs have been successfully demonstrated. For the first time, periodic peaks of Si scallop on the sidewall are deformed in the trench with a diameter of 30 μm, whereas the peaks are intact in the trench with a diameter of 10 μm. The 10 nm Al_2O_3 dielectric layer is also impaired at the damaged Si peaks. The leakage current density at 1.5 V is 4.0×10^{-9} A/cm^2 for D00, 4.1×10^{-8} A/cm^2 for D10, 1.1×10^{-6} A/cm^2 for D20, and 7.4×10^{-1} A/cm^2 for D30, respectively. The record high capacitance densities of 6,547.1 nF/mm^2 for D10 and 7,091.7 nF/mm^2 for D20 are achieved. The results suggest that the structural integrity is preserved for the D10 and the D20 test vehicles, but it is compromised for the D30 test vehicle due to larger thermo-mechanical stress that cannot be tolerated. In the future, a partially-filled TSV could potentially mitigate the stress, but it might suffer from higher DC resistance, worse reliability, and planar process compatibility issue. Apart from the structure integrity, many other aspects of this new device also need to be carefully assessed (e.g., its electrical performance and coupling effect at high frequency). Those topics will be further discussed extensively in the future publications.

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