Thermal Characterization and Management of GaN-on-SiC High Power Amplifier MMIC

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***Abstract*—Driven by the industry trends in radar applications, Gallium nitride (GaN) power amplifier (PA) has developed quite fast, targeting high performance needs, which in the meantime has posed critical challenge for device thermal management. Thermal design was started during the transistors and chip design. There are three stage transistors in the designed GaN PA chip. Thermal simulation correlated with IR camera experiment has been conducted for design, analysis and characterization of GaN-on-SiC Monolithic microwave integrated circuit (MMIC). Peak channel temperature and thermal resistance for DC and pulsed RF input operation have been investigated. The junction-to-case thermal resistance of the GaN chip under DC operation is 1.63°C/W, white thermal resistance is 1.05°C/W under pulsed operation. The validated model and results were used to guide the MMIC design, function test and reliability evaluation.**

Keywords—thermal characterization, GaN power amplifier, MMIC, peak channel temperature, multi-stage transistors

I. Introduction

Of higher break down field, high-efficiency power switching and large current handling capabilities, Gallium nitride (GaN) has the ability to offer many advantages over Si technologies to deliver higher output power from devices of smaller size and lighter weight [1-3]. Its unique features are responsible for its exponential growth and wide adoption to address amplification needs in extensive RF applications in the industry, especially for radar system and satellite communication. GaN-on-SiC power amplifier (PA) is of much better thermal performance, and can tolerate much higher temperature for high power operation [4,5].

Driven by the industry trends in radar applications, GaN PA has developed quite fast targeting high performance needs, which in the meantime has posed critical challenge for device thermal management. The self-heating inhibits the improvement of its potential electrical characteristics and causes issues for stable operation of the devices [6-9]. The highly concentrated heat and large temperature gradient may cause performance degradation for GaN MMIC, and then affect system operation. Accurate test techniques are quite essential to estimate the chip junction temperature under DC and RF operation, and to determine active degradation mechanisms of the devices [10-12]. In this work, thermal design was started at the transistors and chip design stage. Detailed simulation model has been constructed for thermal analysis, and experimental test using IR camera have been performed and correlated for performance investigation. The peak channel temperature of GaN transistor has been estimated using the validated simulation model. Thermal performance for both DC operation and pulsed operation have been analyzed. The scheme and results were used to guide the chip design, function test and reliability evaluation.

II. GaN MMIC Description

Thermal design and analyses have been performed on a GaN-on-SiC MMIC power amplifier for X-band radar platforms. The PA chip includes three stages: 1st stage has two 150μm × 120 μm devices, 2nd stage has four 250μm × 180 μm devices, and 3rd stage as the final has eight 280μm × 180 μm devices, as is illustrated in Fig.1.

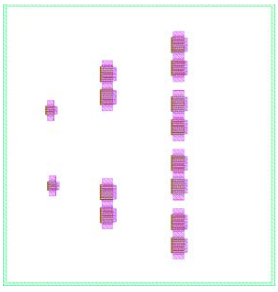


Fig. 1. Schematic image of MMIC layout with three stage amplifiers

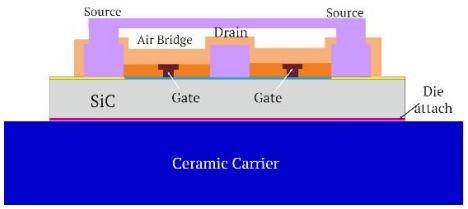


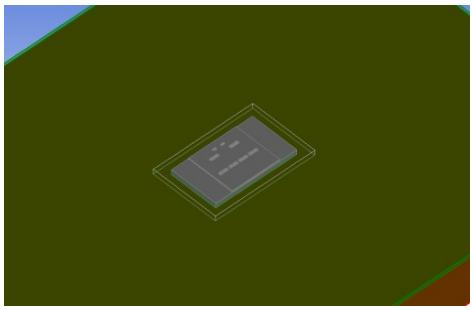
Fig. 2. Cross-section view of structures of GaN-on-SiC PA MMIC

The chip size is 5mm × 5mm, with transistors of gate length 0.4um and 10 gate channels in each transistor for 2nd and 3rd stage. The air bridge, spanning between source metals, only covers a small part of the gate finger, of length 20μm, compared with 180μm gate channel width. The High Electron Mobility Transistors (HEMT) with sub-micrometer T-shaped gates, were fabricated on the frond side, the SiC substrate was thinned to 100μm, as is illustrated in Fig.2. It is mounted on a ceramic carrier of high heat conductivity, through Epoxy die attach. The chip is designed to enable output power >48dbm and PAE >40% for frequency range 8~12 GHz. In the test vehicle module, there is a through opening in the evaluation board for ceramic carrier to be directly attached to the bottom Cu plate for better heat dissipation to the outside environment. During chip fabrication and module assembly, optical microscope and X-ray check were conducted, and no voids were observed for each step. Low interface thermal resistance is quite significant for high power GaN thermal management, especially the layers close to gate fingers ofs highly concentrated heat.

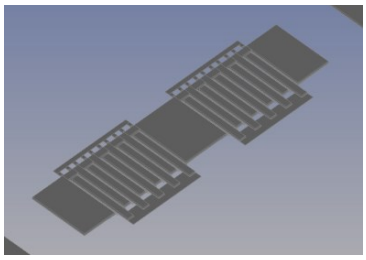
III. THERMAL SIMULATION AND EXPERIMENTAL CHARACTERIZATION

A. Simulation

3D thermal simulation models have been constructed using commercial software ICEPAK, including all key parts of the test vehicle module from transistor gate finger to bottom Cu plate, as is shown in Fig.3. All the detailed layers and structures of the transistors have been built in the model, and the temperature dependent material properties have been used.



(a) whole model of test vehicle



(b) Zoom-in model of the transistor at 3rd stage

Fig. 3. Thermal simulation model of the GaN-on-SiC MMIC

Thermal conditions are set the same as the experimental test, with Cu plate of constant temperature at bottom surface, which will be adjusted by the temperature controller in thermal test platform. The environment is open space of ambient temperature 25°C under natural convection. The heating power is directly provided to the T-shaped gate channel at the bottom surface. The steady-state thermal simulation was first performed, focusing on chip top exposed surface temperature near gates.

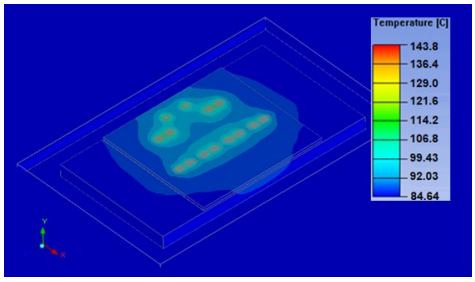


Fig. 4. Temperature distribution of the whole MMIC model

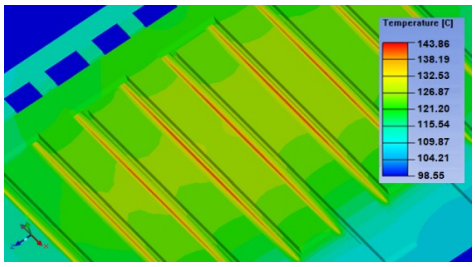


Fig. 5. Temperature distribution of the gate channel

The results in Fig.4. show that there is thermal cross-talk between transistors, even between transistors at different stages. The peak channel temperature occurs at the center location of the gate finger as is shown in Fig.5. The model and setting will be modified and validated by the experiment with IR camera.

B. Experiment

The test vehicle has been fabricated as is illustrated in Fig .6, with GaN MMIC located at the center of evaluation board. The top exposed surface of the GaN chip was painted in matt black for IR camera test, to obtain temperature distribution of devices.

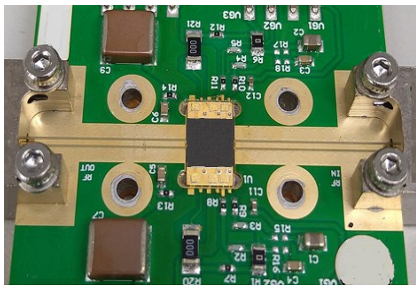


Fig. 6. Photo of the fabricated test vehicle module with GaN MMIC

Experimental tests have been conducted using an IR camera of pixel size 5μm, as is illustrated Fig.7. The top exposed surface temperature of the chip will be measured using IR camera, mainly focusing on the areas of transistors at different stages, as is shown in Fig.7. There will have a temperature difference between the measured temperature with the actual peak channel temperature, due to test setup and chip structure issue. The chip top surface temperature has been calculated and collected from simulation for performance validation.

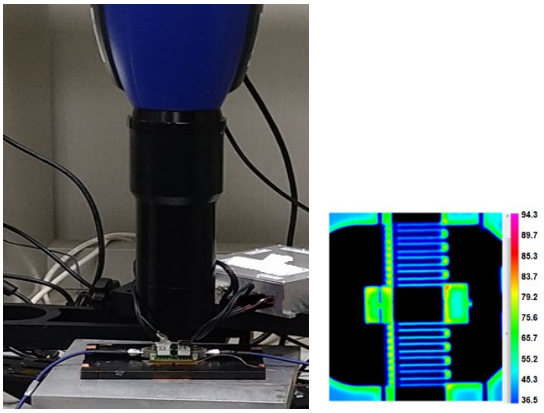


Fig. 7. Photo of IR camera test setup and Temperature distribution

IV. Results Correlation and Model Validation

The Cu plate bottom surface temperature has been changed by temperature controller during DC operation, while same heating power is dissipated for the whole MMIC. The max temperature of three stage transistors have been recorded and compared, as is illustrated in Fig.8.

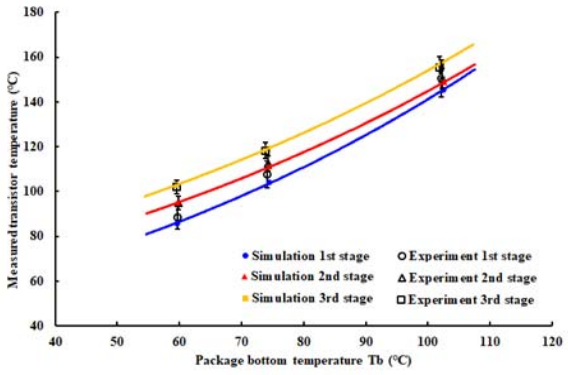
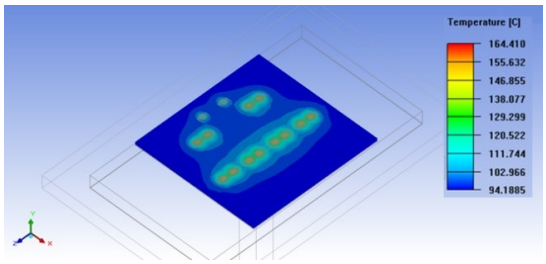


Fig. 8. Simulation results correlated with test results under DC operation

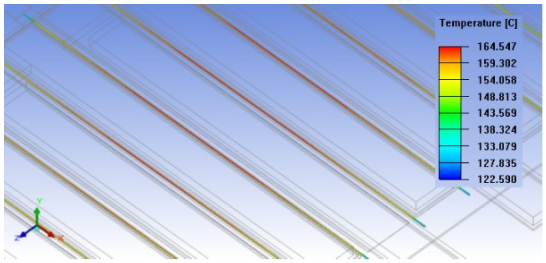
The simulation results show great agreement with the experimental results, and the error is within ±5%. Not only the max temperature, but the temperature profile surrounding each transistor and the package temperature are matched between simulation and experiment, suggesting well validated simulation scheme and model for GaN chip. As to 3rd stage transistor, with package bottom temperature 102°C, the maximum measured temperature is 157.5°C, which occurs at the transistors located at chip center. However, the peak channel temperature of the gate is higher than this based on simulation. There is a temperature difference of around 7°C between the top surface and inside gate, which means the peak gate channel temperature is 164.5°C for 3rd stage transistor. As to 2nd stage transistor, the maximum measured temperature is 150.8°C, while the peak gate channel temperature is 157.6°C. As to 1st stage transistor of lower heating power, the maximum measured temperature is 135.1°C, while the peak gate channel temperature is 139.8°C. For 3rd stage devices, the peak channel temperature of transistor located near chip edge is ~2°C lower than the center ones.

V. Thermal Analysis Under DC Operation

Based on simulation and experiment results, the junction-to-case thermal resistance of the GaN chip under DC operation is 1.63°C/W, where the junction temperature is the peak channel temperature from validated simulation, as is illustrated in Fig. 9.



(a) chip top surface



(b) Transistor gate fingers

Fig. 9. Temperature distribution from simulation results with 38.2W heating power and 102°C package bottom temperature

To study the thermal cross-talk on chip between transistors at different stages, the self-heating and interactive thermal resistances are calculated. The self-heating resistance of 3rd stage transistor is 4.71°C/W. The interactive resistance of 2nd stage to 3rd stage is 0.21°C/W, while the 1st stage to 3rd stage is 0.16°C/W. With the highly concentrated heat in the transistors, the interactive heating from 1st and 2nd stage to 3rd stage is not strong. Since 1st stage and 2nd stage transistors are more close to each other, their interactive resistances are 0.49°C/W from 2nd to 1st stage, and 0.77°C/W from 1st to 2nd stage. With fewer gate fingers in 1st and 2nd stage devices, their self-heating resistances

are much higher than 3rd stage devices. To further mitigate the cross-talk effect, the distance between 1st and 2nd stage transistor is increased by 200μm, and between 2nd stage and 3rd stage by 300μm. Simulation results show that the maximum temperature drop is within 1℃. The following analysis will mainly focus on the 3rd stage transistors performance.

Further simulation has been performed with heat dissipation power 51.1W and package case temperature 55℃, in this case the transistor heat density is 2.3W/mm for 3rd stage. Transient simulation is conducted to monitor gate channel temperature variation during heating time until steady state. Since low thermal impact from 1st and 2nd stage transistors, and to save computing time and resources, this model only includes 3rd stage transistors. Simulation results are shown in Fig.10. and Fig.11.

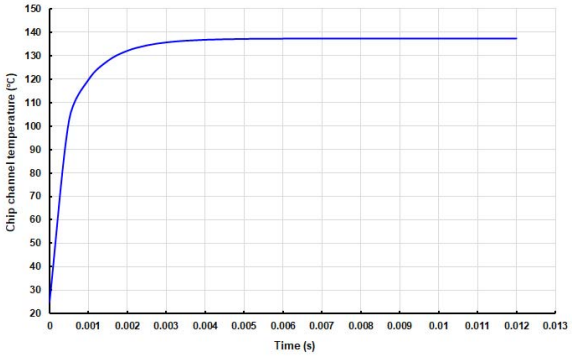


Fig. 10. Temperature variation vs operation time under DC operation

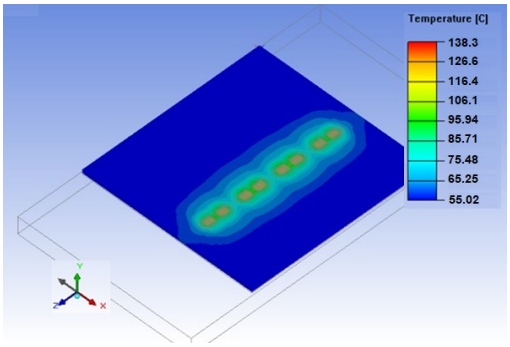


Fig. 11. Chip top surface temperature distribution at steady state

As shown in the results, it takes around 1ms to reach stable state. The peak channel temperature is 138.3℃. With MMIC bottom temperature 85℃, to reach peak channel temperature 200℃ for the final stage transistors, the GaN heating power density of 3.1W/mm, total chip heat power of 70.6W, can be dissipated under DC operation.

VI. Performance under Pulsed Operation

The validated model has been used to estimate the thermal performance under pulse condition with RF input. The same simulation scheme is used to conduct transient thermal analysis under pulsed operation. Experiments have been performed at 10GHz frequency with 10% duty cycle, and input power 25dBm, test platform temperature is set to be 85℃.

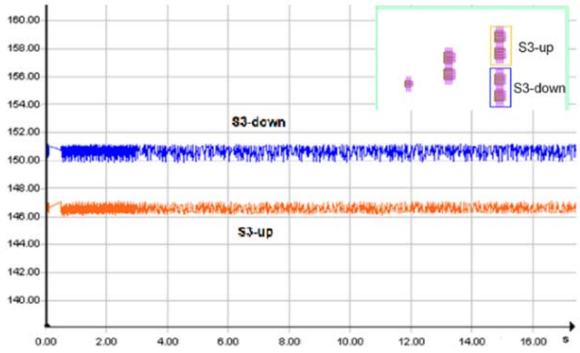


Fig. 12. Temperature measurement results under pulsed operation

As the results shown in Fig.12, there is a temperature difference for 3rd stage transistors located at different locations. S3-up is the transistors located near the chip edge, while S3-down locates near the chip center. The temperature of S3-down is higher than S3-up. According to simulation, the max top surface temperature at S3-up is 146.7℃, while the max top surface temperature at S3-down is 151.6℃. Great agreement has been obtained under pulsed thermal test with RF turned on. According to simulation, the peak gate channel temperature is higher than the measured top surface temperature. As to S3-up, the peak gate channel temperature is 153.5℃, while the peak gate channel temperature of S3-down is 158.4℃.

Further simulations have been performed, using this validated model, to show the transient thermal performance of 3rd stage transistors under pulsed operation, with 51.1W heat dissipation power and package bottom temperature 55℃, as is shown in Fig.13 and Fig.14.

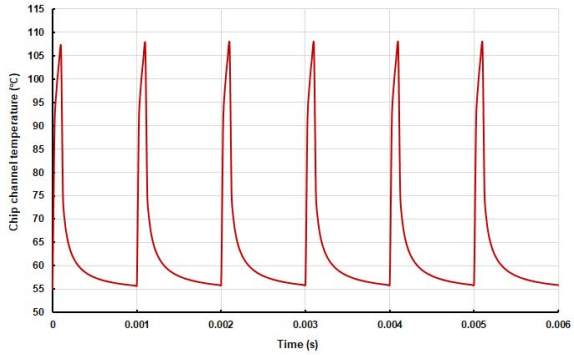


Fig. 13. Temperature variation vs operation time under pulsed operation

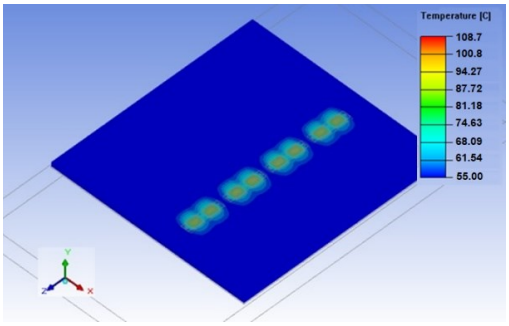


Fig. 14. Chip top surface temperature distribution at peak T during cycle

The peak gate channel temperature is 108.7℃, and junction-to-case thermal resistance is 1.05℃/W under pulsed operation. With MMIC bottom temperature 85℃, to maintain the peak channel temperature of the transistor under 200℃, the GaN power density of 4.92W/mm, chip total heating power of 109.5W, can be dissipated under pulsed operation. To maintain saturation output power for 8~12GHz, the power dissipation for each stage transistors are varied for different frequency, as well as the PAE. The validated thermal simulation scheme and models have been used to estimate the peak channel temperature of GaN transistor to guide MMIC design, and to assist further reliability test under high temperature condition.

VII. SUMMARY

Detailed simulation models have been constructed for thermal analysis, and experimental test using IR camera have been performed and correlated for performance investigation under both DC and pulsed operation. The peak gate channel temperature of transistor has been estimated using the validated simulation model. Thermal performance for both DC operation and pulsed operation have been analyzed. The junction-to-case thermal resistance of the GaN chip under DC operation is 1.63℃/W. With MMIC bottom temperature 85℃, to reach peak channel temperature 200℃, the GaN heating power density of 3.1W/mm can be dissipated under DC operation. The junction-to-case thermal resistance is 1.05℃/W under pulsed operation. With MMIC bottom temperature 85℃, to maintain the peak channel temperature of the transistor under 200℃, the GaN power density of 4.92W/mm can be dissipated under pulsed operation. Based on the scheme and results obtained in this work, the GaN MMIC has been developed and characterized for X-band radar application

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