Nano Porous Gold as a Capping Layer for Thin Film Encapsulation

Jae-Wung Lee, Wei-Shan Wang, Jaibir Sharma, Yu-Ching Lin, Chen Bangtao, and Navab Singh

***Abstract*—This paper reports Nano Porous Gold (NPG) structure as a cap layer for encapsulating MicroElectroMechanical System (MEMS) devices. The NPG solves two main issues in thin film encapsulation (TFE) i.e. (1) longer release time, and (2) mass loading. The uniformly distributed etch channels in the NPG cap structure helps in reduction of release time as well as protection of MEMS devices from mass loading during the sealing as the etch channels form a zig-zag path. This NPG was used as a cap layer for the demonstration of TFE with 400 µm x 400 µm in size. This size of encapsulation was released within 10 min which is 16 times less than that of sidewall located channel scheme. The effectiveness of our scheme is shown experimentally by reducing the release time for 400 µm x 400 µm size encapsulation by a factor 16 in comparison of sidewall located channel. In addition, NPG provides possibility of easy and rapid sealing without contamination of devices inside the cavity.**

***Index Terms*— Thin film encapsulation, packaging, MEMS, release time, Nano Porous Gold**

I. INTRODUCTION

Thin film encapsulation (TFE) techniques have attracted a great attention as a vacuum sealing technique due to the possibility of thickness reduction of overall package device and low cost from elimination of a capping wafer as well as area saving of seal ring in comparison to wafer bonding technique. In order to realize the encapsulation for the MEMS devices, a simple surface micromachining techniques e. g. deposition, etching and release steps are used. The location of the etch holes for releasing TFE and device plays an important roles in this scheme as these etch holes decides the release time of TFE as shown in fig 1 (a, b) and protection of MEMS device during sealing of TFE as shown in Fig 1 (b, c). In one of the approach, the etch channel are distributed all over the cap layer helps in reducing the release time as shown in Figure 1(a) but fail in protecting MEMS device during sealing as shown in Fig 1(c). In another approach, the etch channels are accommodated at the edge of TFE as shown in Figure 1(d) helps in protecting MEMS device during sealing but fail in reduction of release time as sacrificial material to be removed through these side etch channels deep inside near MEMS device as shown in Fig 1(b) [7-8]. The mass loading is very critical issue as it can be cause a electrical shortage, damage or/and can change the operating frequency of many devices like FBAR, SAW etc. This issue on long release time further aggravates when an encapsulation to be done for a large size MEMS device. This also results in a various issues like selection of cap layer and sacrificial layer material because a longer release time may results in attacking the cap layer as well as MEMS devices inside the encapsulation during release. It is also preferred to reduce the release time of encapsulation to increase the throughput of the release process. In view of above, there is a need of encapsulation method which has short release time and safe sealing.

From the above discussion, it shows clearly that all above methods which depend on the location of etch channels suffer from either mass loading or longer release time. Moreover, none of them solve both these issues, simultaneously. To solve above all issues simultaneously, a porous capping layer can be used with micro-or nano-cavities [8-9]. In these approaches, the nano- or micron-sized pores play the role of etch channel which can help in rapidly releasing the structures and sealing without contamination of devices. However, few of these techniques for the fabrication of porous structures suffer from various issues e.g. high temperature, complexity, and difficulty in controlling the etch hole size which make them unsuitable for using as cap layer in commercial product.

To solve the above issues, we propose a simple process for the fabrication of 3-dimensional etch holes in gold cap layer on the sacrificial material. These 3-dimensional etch holes with several tens nanometer in size can be formed by selectively etching of Sn from electroplated AuSn alloy and form Nano Porous Gold (NPG).

In this paper, NPG is used as a cap layer for the demonstration of TFE for MEMS device application. The NPG was performed on oxide sacrificial layer and Vapor HF (VHF) was used as release process. The cavities of the 3µm in height and 400 µm x 400 µm in size can be released in 10 min which is 16 times less than that of sidewall located channel scheme. Further, this process can be used with other sacrificial materials and removal method.

II. DESIGN AND FABRICATION

Figure 2 shows the cross-section view of the proposed TFE scheme where NPG is used as cap layer. The cavity for TFE can be realized by the removing the SiO_2 sacrificial layer through etch holes in NPG. The high porosity in NPG can be obtained by optimizing the electroplating condition of AuSn alloy and selective etching of Sn in the alloy. The NPG consists large number of zig-zag etch channel path which are uniformly distributed all over the capping layer. These large numbers of nano-etch holes

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(pores) helps in reduction of release time of sacrificial layer and zig-zag path of etch holes helps in protection of MEMS devices from mass loading during sealing as shown in Fig. 2. In order to use NPG as cap layer for TFE application and prevent the peeling-off of the cap layer due to seed layer etching during the NPG formation by selective etching of Sn, the anchor areas of TFE is protected by gold mask.

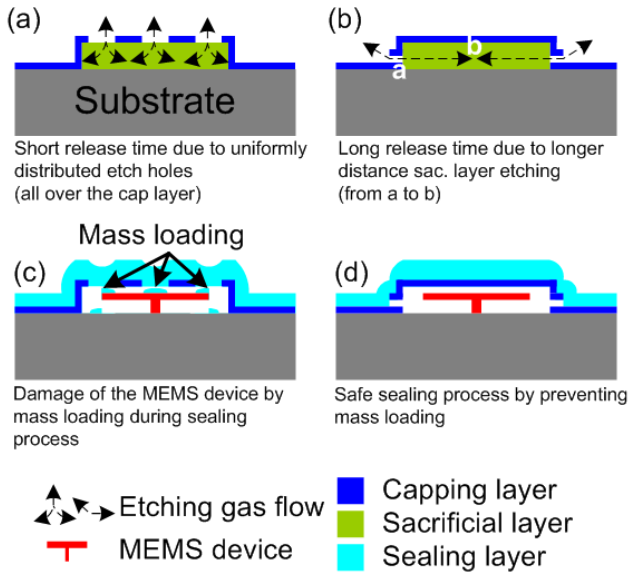

Fig. 1. Schematic diagrams of TFE with (a) uniformly distributed etch hole on the cap layer, (b) sidewall located etch channels and (c),(d) mass loading issue on MEMS device during sealing for TFE realized using a approach as shown in Fig 1(a) and (b), respectively

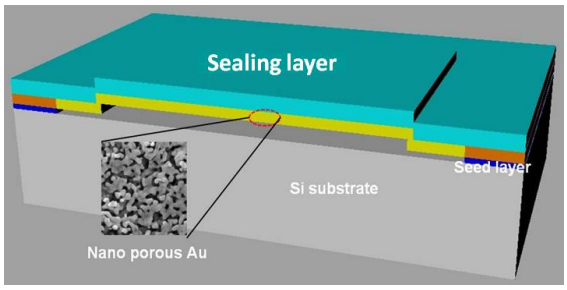

Fig. 2. Cross-section view of proposed encapsulation scheme

The fabrication process flow for proposed TFE is shown in Fig. 3. The encapsulation comprises four parts which are substrate, cavity, capping layer and sealing layer. At first, the cavity for the MEMS device was defined by deposition and patterning of 3µm thick SiO_2 sacrificial layer as shown in Fig. 3(a).

Next, 20 nm Cu seed layer was deposited for electroplating of AuSn alloy. This was followed by the electroplating of AuSn alloy. Fig. 3(b) shows the cross-section view of the sample after AuSn electroplating on Cu seed layer with the optimized current density of 1.25 mA/cm^2. Then gold mask was deposited was patterned to protect the post area of TFE. This was followed by the patterning cap area for selective NPG formation. Gold hard mask was used to protect the region where etching of seed layer and NPG formation is not required.

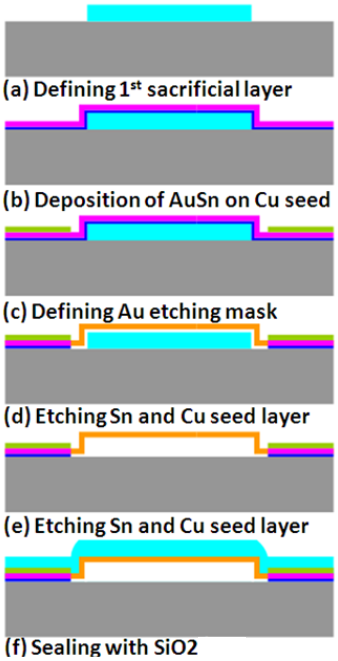

Fig. 3. Process flow diagram for the fabrication of encapsulation

Figure 3 (c) shows the cross-sectional view of the sample after gold hard mask patterning. This was followed by selective etching of Sn from AuSn alloy for the formation of NPG and Cu seed layer. Figure 3(d) shows the cross-section view of the sample after this process step. The cross-section diagram shows the zig-zag through nano-etch holes which can be used to remove SiO_2 sacrificial layer and can be sealed without any mass loading. The nano-etch channels defined in the above step are large enough to etch SiO_2 using VHF [9] and small enough to seal the channels without mass loading. Next SiO_2 sacrificial layer was removed with the help of VHF. This result in free standing cap membrane encapsulating free released MEMS device as shown in Fig. 2(e). After sacrificial removal, TFE was sealed with help of Plasma Enhanced Chemical Vapor Deposition (PECVD) SiO_2. The final encapsulated structure is shown in Fig. 2(f).

III. Results and Discussion

Figure 4 shows the SEM images of the 400 µm x 400 µm size encapsulation after NPG formation by selective etching of Sn and Cu seed layer to facilitate sacrificial SiO_2 removal by through nano-etch channels for releasing TFE. Fig. 4 (a) shows three different regions of the encapsulation which are NPG on SiO_2 sacrificial layer, NPG on Si and Au mask on AuSn alloy. Figure 4 (b) shows pores of several tens of nanometer in size uniformly distributed on SiO_2.

The NPG has zig-zag (torturous) path of the pores (etch channels) which are similar to sponge the structure. This structure helps in protection MEMS device from mass loading during sealing process in comparison to straight etch hole fabricated by Al anodization. Figure 4(c) shows uniform and well developed NPG at the edge of the sacrificial layer without any defects. As explained above, to prevent the peeling-off of the capping layer due to seed layer removal near the post of TFE during selective etching of Sn, gold hard mask was used as protection layer.

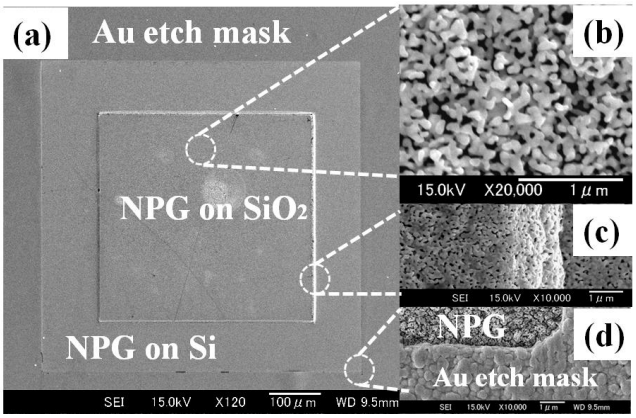

Fig. 4: SEM image of 400 µm x 400 µm size encapsulation with NPG after selective etching of Sn

Figure 4 (d) shows gold protected and un-protected region after selective etching of Sn. from the figure it is clear that gold protected region does not shows any pores.

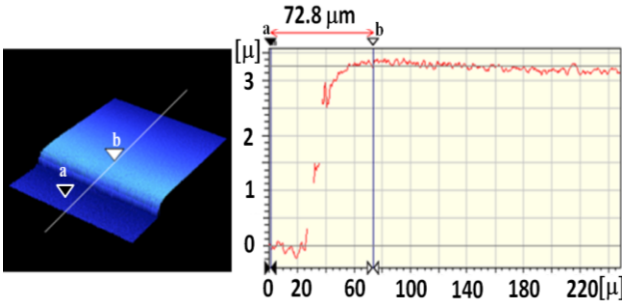

Fig.5. Surface profiling images of 400 µm x 400 µm size encapsulation before sealing

Fig. 5 shows the surface profiler image of the 400 µm x 400 µm size encapsulation after 10 mins sacrificial layer release. The image shows higher height that the 3 um thick SiO_2 sacrificial layer. This means that TFE is released. This release time is 16 times less than in the release time of sidewall located of same size.

Fig. 6 shows SEM images of 400 µm x 400 µm size release TFE with FIB cutting after sealing process. The image shows sealing process was performed successfully without downward deformation of the encapsulation. To investigate cavity inside the encapsulation, FIB cutting was performed on edge of the encapsulation as shown in Fig. 5 (b).

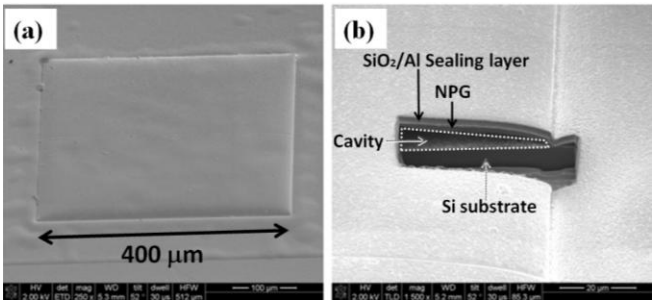

Fig. 6: SEM image of 400 µm x 400 µm size encapsulation (a) full encapsulation with 9 etch holes after sealing and (b) FIB cut at the edge

From the SEM image, it shows that cavity is well released and encapsulation is sealed successfully. A large upward deformation was observed at the center of the encapsulation after sealing. There may be two main reasons for this deformation. One is pressure difference between inside and outside cavity which normally results in down side movement of the encapsulation. The other is stress of the encapsulation layer due to integration by bi- or multilayer of the capping and sealing layer. Our results show positive effect on deformation of the encapsulation layer for formation of deep cavity by stress control.

IV. Conclusion

In this paper, we realized a NPG cap layer for the TFE which is very effective in reducing the release time of the encapsulation as well as in preventing the mass loading during sealing. The experimental results show 16 times reduction in release time for encapsulation of 400 µm X 400 µm size in comparison to sidewall located etch channel. This reduction of release time can solve many complication of TFE like attacking of cap, device, and isolation material during the release process.

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References

[1] G. H. Mohamed, *The MEMS handbook*, 2nd ed., New York, USA: Taylor & Francis, 2002.

[2] R. R. Tummala and E. J. Rymaszewski, *Microelectronics Packaging Handbook*, 2nd ed., Massachustts, USA: Kluwer Academic Publishers, 1989.

[3] K. Najafi, "Micropackaging Technologies for Integrated Microsystems: Applications to MEMS and MOEMS", *Micromaching and Microfabrication process Technology VII, Proc. Of SPIE* Vol. 4979, pp.1-19, 2003.

[4] A. Partridge, M. Lutz, B. Kim, M. Hopcroft, R.N. Candler, T.W. Kenny, et al., MEMS resonators: getting the packaging right, in: SEMICON-Japan, 2005.

[5] B. H. Stark and K. Najafi, "A low-temperature thin-film electroplated metal vacuum package," *J. Microelectromech. Syst.*, vol. 13, pp. 147–157, 2004.

[6] J. L. Pornin, C. Gillot, G. Parat, F. Jacquet, E. Lagoutte, N.Sillon, G. Poupon, F. Dumont, "Wafer Level Thin Film Encapsulation for BAW RF MEMS," *Electronic Components and Technology Conference*, pp. 605-609, 2007.

[7] C. Gillot, J.L. Pornin, A. Arnaud, E. Lagoutte, N. Sillon, J.C. Souriau, "Wafer Level Thin Film Encapsulation for MEMS," *Electronic Components and Technology Conference* ,pp. 243-247, 2005.

[8] C. O'Mahony, M. Hill, Z. Olszewski, A. Blake, "Wafer-level thin-film encapsulation for MEMS" *Microelectronic Engineering* vol. 86, pp. 1311–1313 , 2009.

[9] J. Zekey, D. S. Tezcan1, J.-P. Celis, R. Puers, C. Van Hoof , and H.A.C. Tilmans, "Wafer-Level Thin Film Vacuum Packages for MEMS using Nanoporous Anodic Alumina Membrane," *Transducers conference*, pp. 975-977, 2011.