Electrical Characterization and Reliability Studies of Nano-TSV

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***Abstract*—Nano-TSV formation using Silicon (Si)-On-Insulator (SOI) wafer was demonstrated previously. In which, Si thickness can be precisely controlled using the proposed wafer thinning method. The developed platform is targeted for use as backside power delivery network (BS-PDN). In this work, we had designed and fabricated 180 x 500nm nano-TSV chain and leakage test structures. The Si layer is 75nm thick. In the nano-TSV, the liner and barrier/seed materials are Al_2O_3 and Ta/Cu, respectively. Thereafter, the nano-TSV is filled by Cu eletro plating (ECP) as filling metal. Finally, the wafer frontside and backside are metallized with aluminum for electrical characterization and reliability studies. We first collected nano-TSV chain resistance and leakage electrical data directly after fabrication. These electrical tests were then repeated after subjecting the samples to reliability test conditions, including (1): Thermal Cycling (TC) (2): High Temperature Storage (HTS) and (3): uHAST. The result shows that the nano-TSV process is robust to survive through reliability stress conditions.**

Keywords—nano-TSV, backside power delivery network, electrical characterization, reliability study

I. Introduction

Backside power delivery network (BS-PDN) is a proven application for nano-TSV as shown in Fig.1. In a typical topside power and signal routing, the density of active devices is limited by the number of interconnects. With the advent of backside nano-TSV, power lines can access devices from the backside. This architecture allows the topside to be dedicated to signal lines. As a result, it enables higher packing density of devices [1], [2], [3], [4]. Thus, it is expected that nano-TSV can also increase data bandwidth significantly between two directly bonded wafers through enabling higher density of interconnects [5], [6], [7], [8]. Although Nano-TSV fabrication is matured in CMOS back-end-of line (BEOL) processes, the method of achieving thin Si thickness (<500nm) with repeatable and precise thinning control remains a challenge [9], [10], [11].

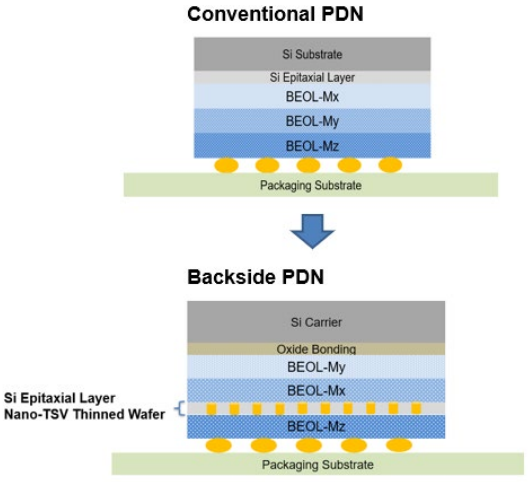

Fig 1. Schematic of Conventional-PDN v.s. Backside-PDN

A novel wafer thinning integration process for nano-TSV formation by SOI precise wafer thinning process was previously demonstrated [12]. In this work, we had designed and fabricated nano-TSV chain and leakage test structures with Aluminum metallization on wafer frontside and backside as electrical connections with silicon thickness of 75nm. We first collected the nano-TSV chain resistance and leakage electrical data directly after fabrication. These electrical tests were then repeated after subjecting the samples to reliability test conditions, including (1): Thermal cycling at -40C to 125C for 60 cycles; (3): High Temperature Storage (HTS) for 60hrs and (4): uHAST (130C, 85% RH, 48hrs). Subsequently, we compared the electrical measurement data before and after reliability stress conditions to verify the robustness of our nano-TSV fabrication process.

II. FABRICATION

12" SOI wafers with SOI Si thickness of 75nm on 2000A buried oxide (BOX) are used. Al is first deposited using physical vapor deposition (PVD) and patterned to form the front side metal connection. Then an oxide layer is deposited using low temperature chemical vapor deposition (CVD) method. Thereafter, the oxide layer is planarized. Subsequently, the wafer is fusion-bonded to a Si wafer, pre-deposited a layer of oxide. Thereafter, the thick top Si substrate is thinned down by edge trimming and mechanical grinding process. The SOI wafers BOX layer is then exposed by plasma dry etching to remove the top Si remaining layer and HF-nitric-acetic acid was used to remove the BOX layer. After the precise thinning process, nano-TSV was then fabricated using immersion lithography and plasma dry etching processes. Subsequently, Al_2O_3 passivating dielectric was deposited using atomic layer deposition (ALD) process. This is followed by Ta/Cu PVD as barrier/seed, and Cu electro plating (ECP) as filling metal.

Then the wafer is subjected to chemical mechanical polish (CMP) to planarize the Cu surface. Finally, backside Al metal is formed. Fig. 2 illustrates the process flow. Fig. 3 shows the SEM/TEM images of the 180 x 500nm nano-TSV fabricated with Al frontside and backside metal by precisely thinning process on SOI 75nm Si wafer.

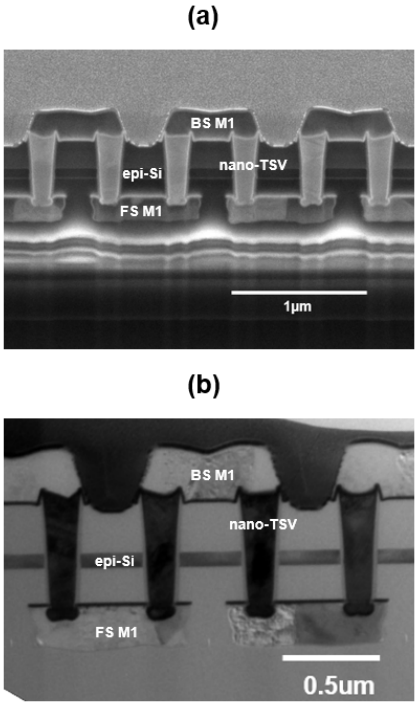

Fig 3. (a) SEM; (b) TEM images post the nano-TSV process

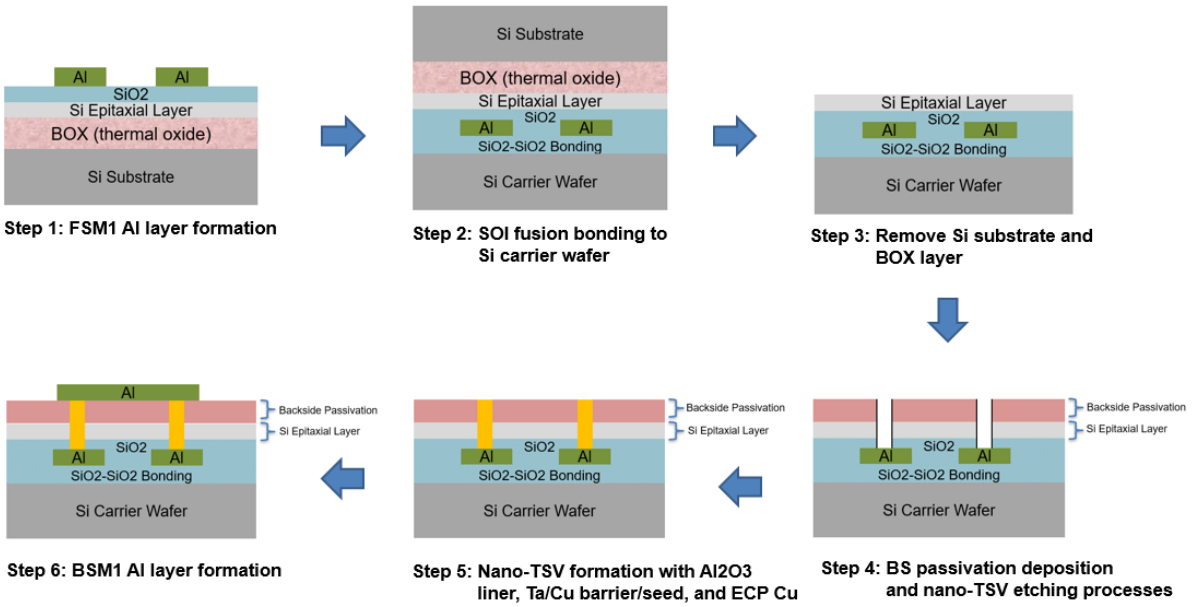

Fig 2. Process flow of nano-TSV with Al metallization on wafer frontside and backside

III. WARPAGE CONTROL

Since nano-TSV fabrication used the immersion scanner for lithography, the wafer warpage control was a concern due to strict alignment constrains. In addition, high warpage will also impact the yield results during different processes. To control wafer warpage, SOI wafer with a thin 2000A BOX layer was selected to use in this process since the BOX layer thickness contributes to significantly compressive stress during the wafer thinning process and limits the thinning process options. For fusion bonding and passivation oxide deposition, CVD with optimized film stress was used for warpage control purposes. had been optimized for warpage control purpose. Fig. 4 shows that wafer warpage is well controlled (< -100µm) during different fabrication process steps of the nano-TSV wafer.

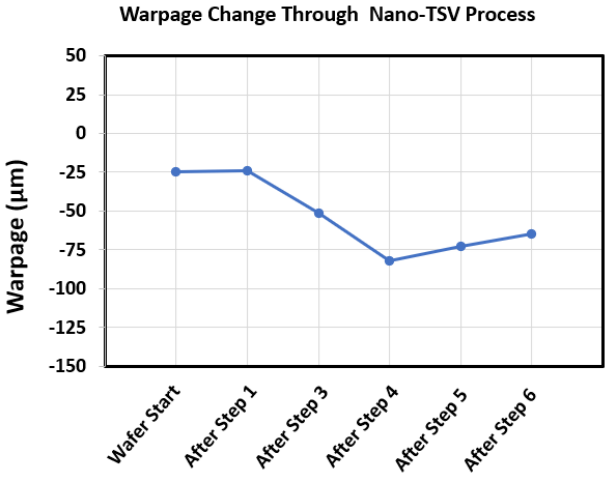

Fig 4. Wafer warpage change during different fabrication process steps of the nano-TSV wafer

IV. ELECTRICAL CHARACTERIZATION

To characterize electrical performance of the nano-TSV wafers, we have designed and fabricated nano-TSV daisy chain connecting Al metallization on the wafer frontside and backside as electrical connections. Fig. 5 shows GDS design and schematic for nano-TSV daisy chain. Electrical I-V curve for a single TSV is shown as Fig 6.

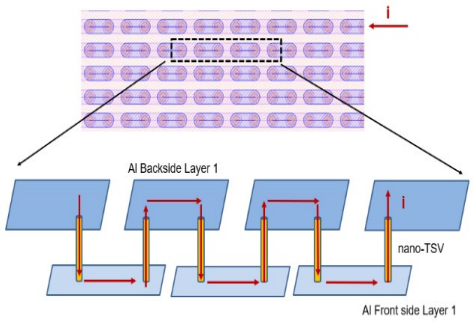

Fig 5. GDS design and schematic for nano-TSV daisy chain pattern

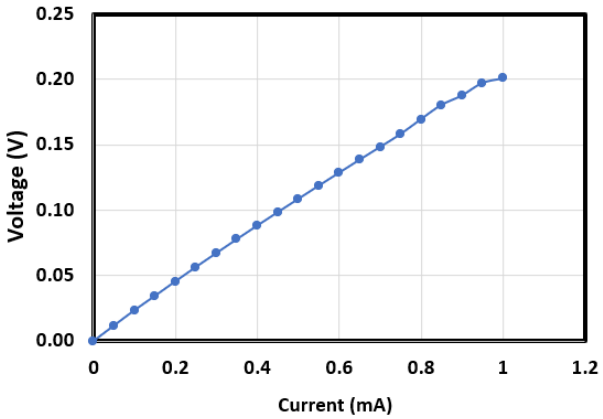

Fig 7. Single nano-TSV I-V curve

For nano-TSV chain with parallel TSV connection between Al frontside/backside metal layers, Fig. 8 shows the GDS design and the schematic. Fig. 9 shows I-V curve of the pattern.

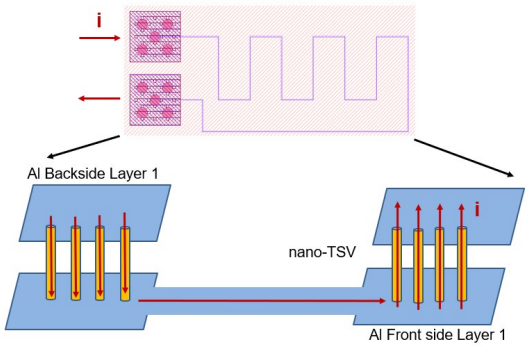

Fig 8. GDS design and schematic for nano-TSV chain with parallel TSV connection

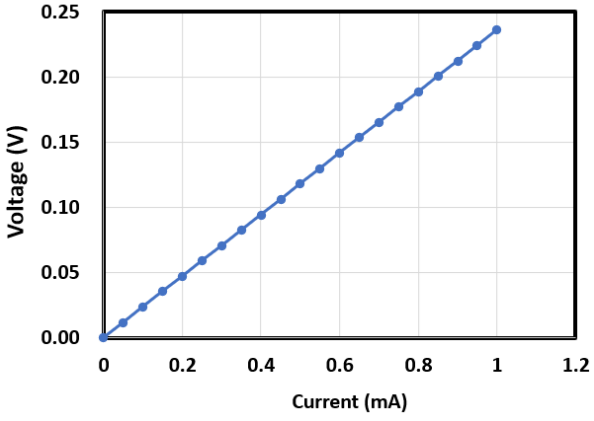

Fig 9. Parallel nano-TSV chain I-V curve

For nano-TSV leakage pattern, Fig. 10 illustrates the GDS design and the schematic. Fig. 11 shows electrical leakage data of the pattern.

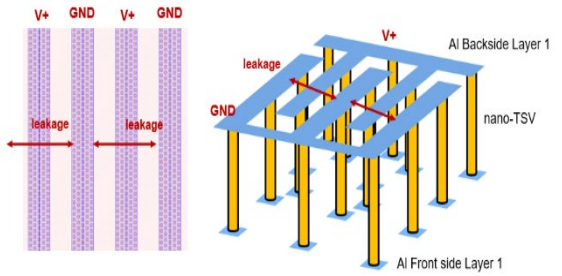

Fig 10. GDS design and schematic for nano-TSV leakage pattern

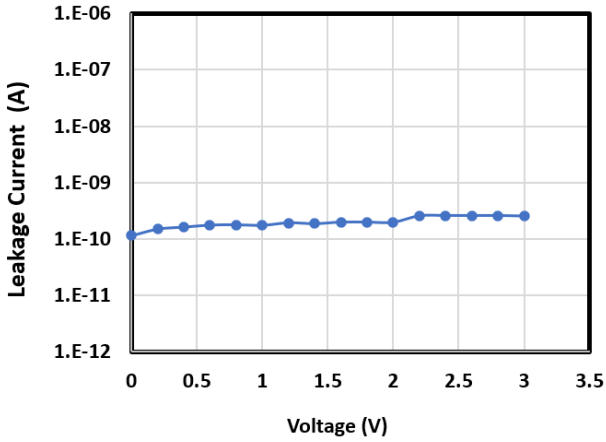

Fig 11. Nano-TSV leakage data

V. Reliability Data

We first collected nano-TSV chain resistance and leakage data directly after fabrication (T0). These electrical tests were then repeated after subjecting the samples to reliability test conditions (T1), including (1): thermal cycling at -40C to 125C for 60 cycles; (2): High Temperature Storage (HTS) for 60hrs and (3): uHAST (130C, 85% RH, 48hrs). Table 1 shows the summary of reliability test condition.

Table 1. Summary of reliability test condition

Item	Reliability Test Condition
a	Thermal cycling at -40C to 125C for 60 cycles
b	High Temperature Storage (HTS) for 60hrs
c	uHAST (130C, 85% RH, 48hrs)

For the thermal cycling results, Fig. 12 and Fig. 13 show the T1 data is comparable to the T0 data post reliability testing for both parallel nano-TSV chain resistance and leakage patterns.

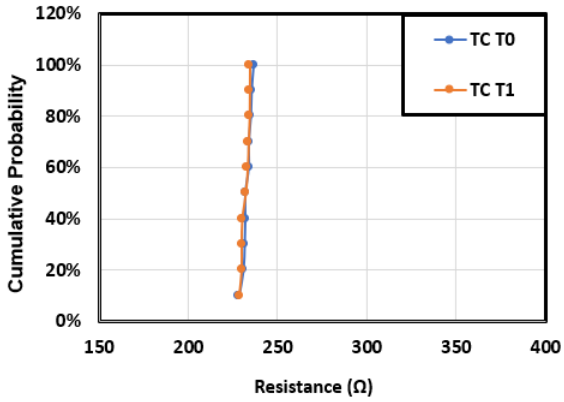

Fig 12. Thermal cycling reliability data for parallel nano-TSV chain resistance

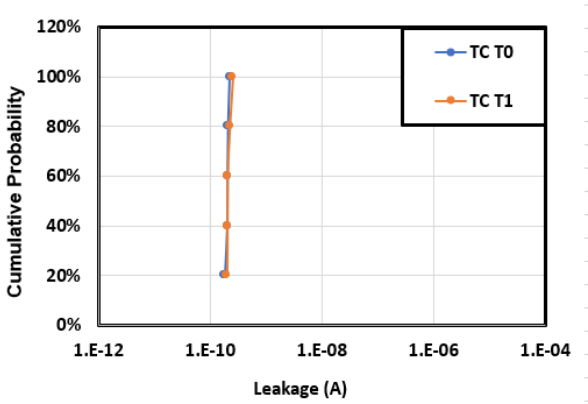

Fig 13. Thermal cycling reliability data for nano-TSV leakage pattern

For the HTS results, Fig. 14 shows ~90% of the T1 data is comparable to the T0 data for parallel nano-TSV pattern. Besides, Fig. 15 shows the nano-TSV leakage data is comparable between T0 and T1. For the uHAST result, Fig. 16 shows T1 data is comparable to T0 data post reliability testing for parallel nano-TSV chain resistance. For the leakage pattern, T1 data is slightly larger than T0 data post the testing.

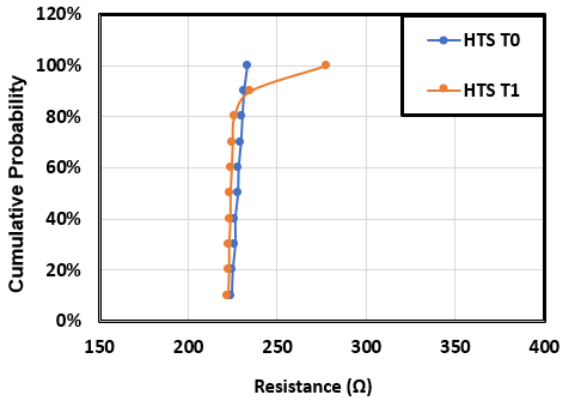

Fig 14. HTS reliability data for parallel nano-TSV chain resistance

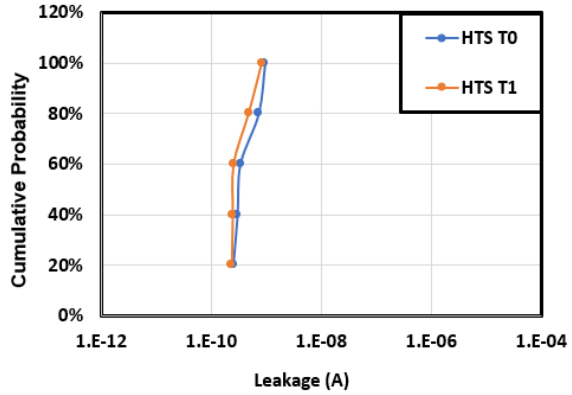

Fig 15. HTS reliability data for nano-TSV leakage pattern

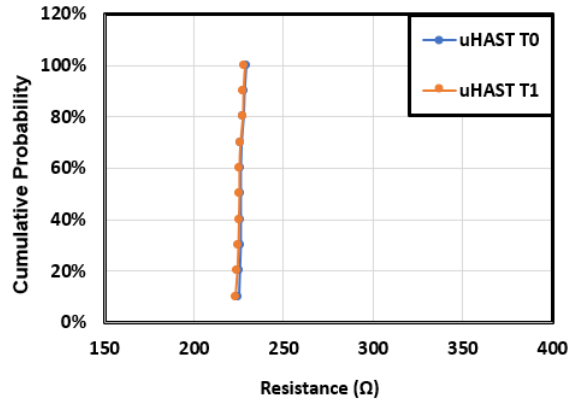

Fig 16. uHAST reliability data for parallel nano-TSV chain resistance

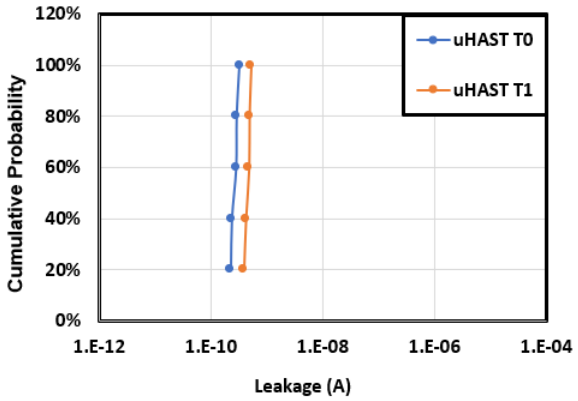

Fig 17. uHAST reliability data for nano-TSV leakage pattern

The above reliability results show that the nano-TSV chain resistance and leakage test structures can survive through the reliability stress conditions. Although the reliability testing conditions are not as complete as JEDEC standard. But the robustness the nano-TSV had been verified.

VI. Conclusion

A robust 180 x 500nm nano-TSV chain formation with precise wafer thinning method using SOI wafer is demonstrated. The study conducted the electrical characterization and the reliability stress testing to verify the performance of the nano-TSV chain and leakage test structures. The reliability result shows the nano-TSV chain is still robust post the stress testing. This provides possibility of application in backside power delivery network and high-performance computing.

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