Wafer Level Fabrication of Embedded Silicon Microcooler on Heating Devices

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Abstract

The demand for cooling performance on microelectronics package is in increasing trend due to the complexity of multi-chips packaging design and enhanced chips performances. This paper demonstrated the wafer level fabrication of embedded silicon heat sink and silicon-based liquid microchannel on metallic heating and sensing device. This thermal management solutions was designed to achieve high heat dissipation. 3.6um thick of metallic heater and sensor was used to deliver high power flow and direct embedded liquid cooling channel was fabricated at the opposite site of heating devices. Wafer level fabrication process integration flow was established. Process feasibility challenges issues and defectivities incurred were addressed. The respective solutions or process parameters optimization were discussed in this paper.

Introduction

The advancement of microelectronic processing allows miniaturization design into more complex and enhanced chip performance. Packaging technologies were involved into heterogenous multi-chips packaging such as 3D chip stacked packages, chiplet packaging and fan-out wafer level packaging which require high demand of thermal management. Microchannel liquid cooling become one the most effective thermal management solutions. M. Bergendahl. [1],[2] developed stack silicon micro-cooler with miniaturized fins and channel width, attached to functional chip with separable metal lid or with direct TIM laminated respectively. In this paper, direct embedding of liquid cooling channels and pin fins within silicon substrate give numerous advantages over functional chip thermal management. Wafer level silicon cooling channels fabrication allows miniaturized channels width, thinner pin fins and conductive walls which increase the thermal heat transfer efficiency. On the other hand, embedded channel allows direct cooling contact with the heating device which leads to higher heat transfer coefficient which could widely applied in semiconductor power devices and radar communications. Silicon channels enhance the flexibility of chip cooling to multiple chip stacking and cross flow to meet higher heat dissipation.

As shown in Fig.1, three main components were comprised in this thermal solution package, such as: as (i) Silicon Cap at 300um thick; (ii) Silicon substrate at thickness 300um, with 250um depth microchannel cavity on top surface; (iii) Metal heaters and sensors built on bottom surface of silicon substrate. 3.6um thick of metal heater and sensor, with line width at 200um and 20um respectively was fabricated on co-planar layer to meet the high accuracy of thermal sensing.

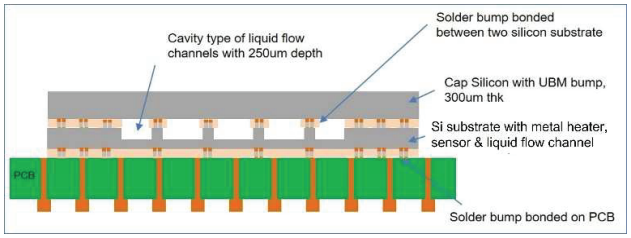


Fig. 1. Schematic of Package Metal Heaters and Sensors with Embedded Cooling Solution Structures

Methodology

Fig. 2 and Fig. 3 show the full fabrication process flows of this metal heaters and sensors with embedded silicon microchannels at the opposite side. 3.6um thick of metallization process was deposited on silicon substrate via plasma vapour deposition with enhanced cooling and deposition loop controlled. Subsequently, photo-lithography patterning process was performed to build the heater and sensor structures via series of processes such as photoresist coating, UV-exposure and chemical developing. Chemical wet-etching was processed to remove the exposed metal surface selectively while the heaters and sensors structures which protected by layer of photoresist, were hindered from chemical etch will be built completely after stripping of photoresist and unused seed layer. Due to unusual thickness of metallization layer, chemicals wet etch timing and in sequence of oxygen plasma processes was optimized to ensure effective removal of undesired metal layer without residue and over-etching of metal sidewall. Dielectric layer and via opening were processed in parallel with series of polyimide coating, litho-patterning, developing, and curing processes. Photosensitive dielectric layer was selected instead of CVD dielectric due to shorter process throughput and lower process cost to fabricate a thick layer of dielectric and via opening to ensure better insulation performance without cross-talk issues between heaters and sensors during high current input. CuNiAu UBM was fabricated on via openings to connect heater and sensor metals towards PCB via solder bond. UBM fabrication started with PVD Ti/Cu seed layer deposition, followed by photoresist coat, expose and develop to pattern UBM opening at 200um diameter. CuNiAu bump electroplating process was performed on via opening at desired thickness. After photoresist and seed layer stripped, frontside fabrication processes completed.

As shown in Fig.3, a substrate carrier was temporarily bonded on metalized surface and to proceed fabrication of microchannels and pin fins on the opposite of wafer. Temporarily materials such as release, and adhesive glue layers were spin coated on substrate carrier first. Subsequently, wafer front-side surface was thermal-pressurised bonded with coated substrate carrier. Wafer backside will be sent for backgrind

thinning to desired thickness at 300um. CVD oxide deposition and was performed as dielectric layer between opened TSV and next UBM layer. Photoresist and oxide hardmask were patterned with the microchannel and pin fins structures to act as protective layer during subsequent silicon dry etch process. Deep reactive ion-etch process was performed to etch silicon layer selectively at more than 200um depth. CuNiAu bumping process was performed again via PVD seed metallization, lithography patterning and CuNiAu electroplating process. All plasma oxide/metal deposition and reactive gas etching processed parameters were optimized to manage thermal budget from overheating the bonded carrier, which could lead to delamination issue. Temporarily bonded carrier was debonded and cleaned afterwards. Full wafer level fabrication process completed.

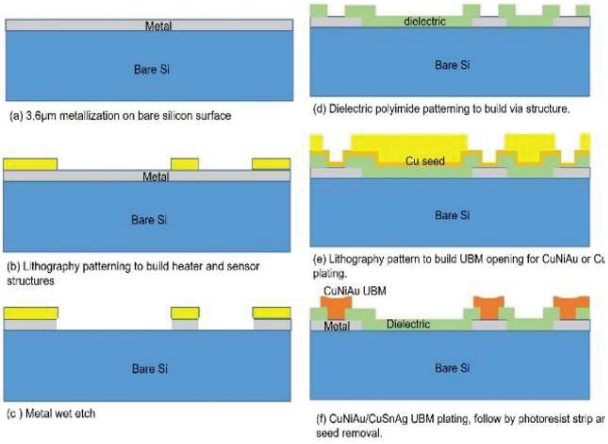


Fig. 2. Schematic Fabrication Process Flow of Front-side Heaters and Sensors

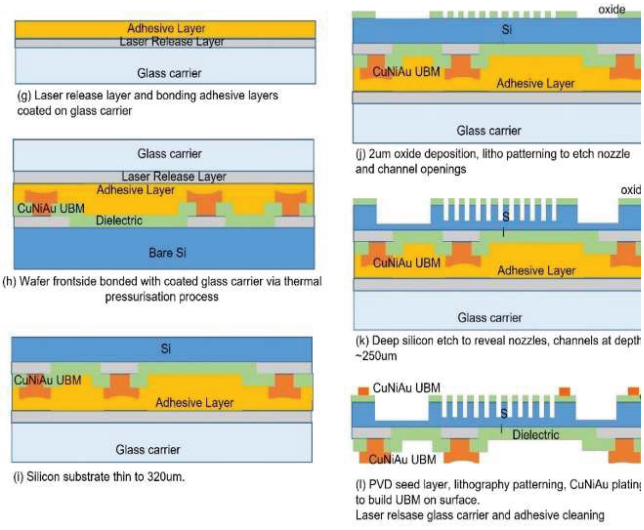


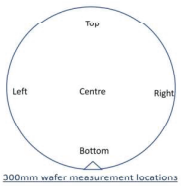
Fig. 3. Schematic Fabrication Process Flow of Back-side Microchannels

Results and Discussion

Critical process parameters and conditions was evaluated and developed to meet the product specifications as well as process feasibilities, without defects. Key measurements and inspections were performed and tabulated, to discuss the process issues and defectivity which incurred at specific process steps. The solutions and optimized parameters were developed and elaborated in this paper.

I. Development of thick metalization process at good thickness and uniformity control.

Fabrication of metal sensors and heaters were processed through PVD deposition process on silicon oxide surface. This thick metallization, 3.6µm requirement compared with standard deposition process at <5000A aroused several key challenges. They are such as thick deposited metal at good uniformity, metal etch without serious undercut and residues issues. This thick metal required long deposition process time which could lead to metal-arching defects, build-up stress to cause wafer warpage and metal peeling issue. Hence, deposition process parameters such as process power, time, intercepting cooling steps and cycle loop deposition rate were optimized to manage the thermal budget accumulation, sufficient time-relaxation of stress build-up and as well as enhanced plasma control to prevent arching defect and good deposition uniformity. Subsequently, chemical etching process was performed selectively on photolithography patterned metal surface to carve the sensors and heaters structures. Table.1 shows the measurement results of the sensor and heater width and thickness. The average results were obtained from five locations measurement across wafer, good uniformity achieved. The width measurement results show 7-8µm of sidewall loss for sensor and heater respectively due to long etching process time. The sensor and heater thickness are at 3.5µm and 3.6µm respectively, within specification of 0.1µm variation. Chemical etching process time and mechanism was optimized here. Extra longs etch process time was carried out due to 7 times thicker of metallization. However, this will lead to severe metal undercut and thickness over-etched until 1.8µm remained at shown in Fig.4. Consequently, high resistance or metal discontinuity issues aroused. Investigation noticed that due to high concentrated metal-etch, etched metal will be redeposited and adhere to photoresist at metal sidewall as shown in Fig.5. This hindered and slowing down the metal etching rate. Thus, optimized process parameters spin speed, etch-time and etch mechanism was developed. Process mechanism was remodified into multi-steps etching. 60% of standard etch was performed first, followed by photoresist stripping and last step of metal residue cleaning. Comprehensive results have been achieved with targeted thickness, sensor metal width at acceptable resistance measured at 650ohm. Fig. 6 show the sensor resistance response (range from 650ohm to 1000ohm) with variation of temperature from 25degC to 150degC. Linear correlation achieved and showed good metallization properties. This justified the metal dimensions as tabulated are within specifications and the metallization processes were optimized.



Measurement	Width (um)		Thickness (nm)	
Wafer Location	Sensor	Heater	Sensor	Heater
Centre	13.2	192.2	3337.7	3551.1
Top	12.4	191.8	3809.0	3683.1
Right	13.1	189.4	3883.7	3675.2
Left	13.8	191.5	3300.8	3581.3
Bottom	13.9	193.9	3267.0	3630.2
Average	**13.3**	**191.8**	**3519.6**	**3624.2**

Tab. 1. Metalized Heater and Sensor Measurement Results

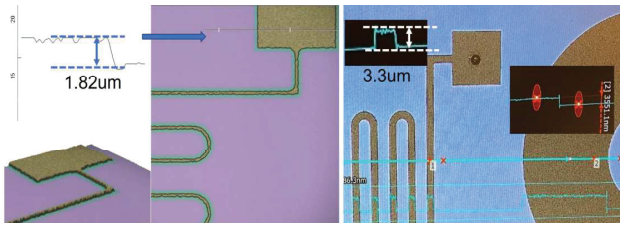


Fig. 4. Metal Thickness and Width Comparison at Different Chemical Etch Process Time (left) 50% Excessive Etch Show (right) Optimized Etch Time.

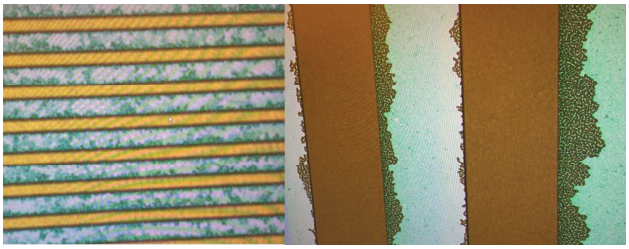
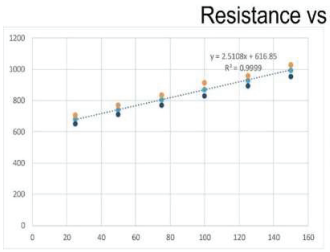


Fig. 5. Microscopic Images on Metal Residue Observed at Sensor Lines (left) and Heater Lines (right)



Temp	Resistance1	Resistance2	Resistance3
25	680.9	706.7	651.8
50	742.0	770.7	710.5
75	804.5	834.6	770.7
100	866.8	912.1	831.4
125	929.6	960.3	892.5
150	995.2	1029.8	955.4

Fig. 6. Metal Sensors Resistance Response to Variation of Temperature Measurement Results

II. Temporarily Carrier Bonding Method Selection and Evaluation.

After frontside processes completed with dielectric and UBM layers on top of heater/sensor metal, wafer has to be temporarily bonded to a carrier in order to perform backside microchannel trench and pin-fins processes. Glass carrier bonding was in favorable due to its debonding mechanism is at less destructive and less mechanical friction with device surface. Glass debonding via laser removal of release layer on glass to separate both substrates, helps to minimize the contact force applied on channel-etched (thin-wall) wafers which could cause crack or breakage of wafer. However, as shown in Fig. 7. the warpage induced due to CTE mismatched with different substrate was demonstrated. Glass bonded substrate shows larger warpage condition at 500µm and failed to vacuum chuck during dry etching process. Silicon carrier bonded gave a better warpage control at less than 200µm. This allow process feasibility in vacuum chuck as well as better process stability in subsequent etch, lithography and metallization processes. In order to improve the process allowance for mechanical shim-cutting debonding method from silicon carrier, pattern density for microchannel trenches was reduced to half to enhance the wafer stiffness.

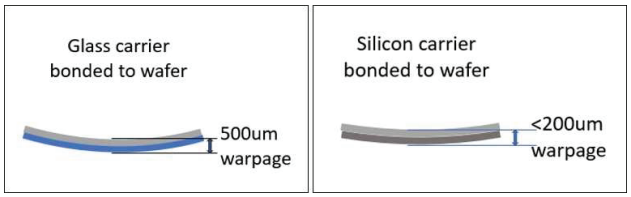


Fig. 7. Schematic of Glass or Silicon Carrier Temporarily Bonded with Wafer Frontside

III. Optimized Oxide and Metal Deposition Process Parameters to Prevent Bonded Carrier Delamination Due to Overheating

Oxide and metal plasma deposition process are required on opposite sides of bonded wafers. Specific thermal budget management is required to ensure bonded carrier does not delaminate and separate due to overheating at temperature higher than 200degC at long process time. CVD thick oxide deposition process parameters, mechanism and surface pre-treatment conditions were optimized to ensure appropriate thermal budget build-up, with good layer stress control and as well as no oxide layer delamination issue. This thick oxide layer was used as hardmask for deep trench reactive gas dry etching process and act as adhesive layer to build UBM layer on top. Hence, PVD seed layer deposition process was applied as seed layer for CuNiAu UBM plating. In-situ PVD processes integrated high temperature degas, argon plasma native oxide cleaning and argon plasma metal deposition processes which could induced accumulation of thermal budget. Similar to CVD plasma process, this could lead to weakened the silicon adhesive bonding and create potential risk of bonded-carrier separation. Additional cooling steps and PVD process parameters was optimized to ensure sufficient cooling during these plasma steps.

IV. Microchannel Trenches and Pin-fins Dry Etch Process Optimization

Silicon microchannel trenches and pin-fins were fabricated via silicon DRIE (deep reactive ion etch) process with oxide hardmask and photoresist as hindering layers. Fig.8 shows the SEM images of the silicon etch profile on pin-fins and trenches structures. This optimized cycle loop of etching mechanism achieved straight via profile with maintaining top and bottom pin-fins opening at 52+/-1µm, with depth at 200µm. Smooth sidewall and bottom corner without undercut observed as well. Furthermore, Fig.9 shows etch dimension measurement results at centre and edge across wafers. Good process uniformity was achieved with trench depth at around 200µm, pin-fins depth at around 210µm from centre to edge of wafer. Trench at larger

opening show slight faster etch rate compared to high density pin-fins area. Fig.10 shows the overall image of this cooling chip design which embedded with heaters and sensors. Cooling liquid will flow horizontally via the side openings across the pin-fins resided at middle area. Thin bottom wall at 80µm was remained to ensure structure stiffness after bonded to cap silicon chip and withstand liquid flow pressure. Due to high density openings, extra long process time required to meet this deep etching. This will lead to insufficient masking protection, burnt mark observed, as well as etch rate uniformity concern. Thus, alternate etch-patterning was developed to reduce 50% of opening as shown in Fig.11. This xray figure also demonstrated good alignment between opposite sides heaters/sensors and trenches features.

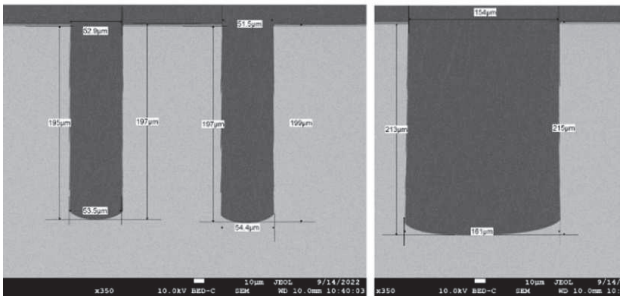


Fig. 8. SEM Images of Silicon Pin-Fins and Trenches Etch Profile Measurement Results

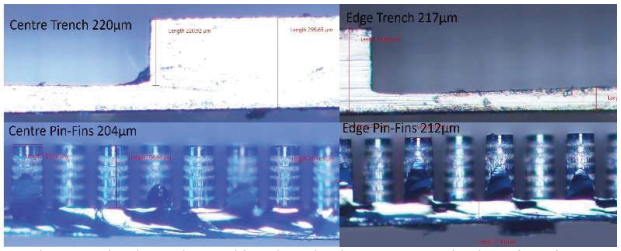


Fig. 9. Etch Dimension Uniformity Check at Centre and Edge of Wafer

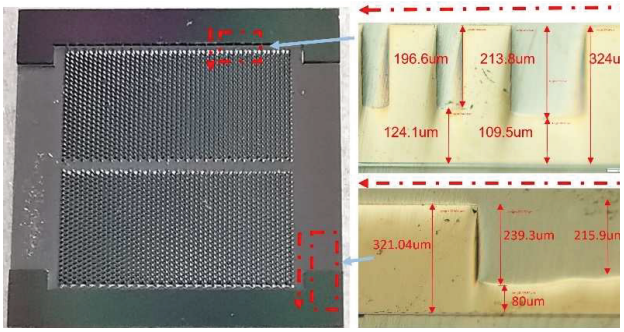


Fig. 10. Overall Silicon Cooler Scope Images and Etch Dimension

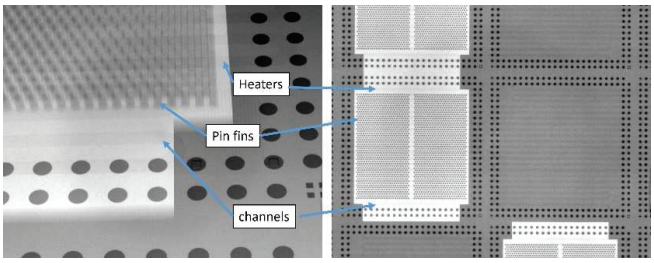


Fig. 11 Xray Images of Frontside Heaters with Embedded Pin-Fins and Channel Trenches on Opposite sides of Wafer

Conclusions

The wafer level fabrication of embedded cooling microchannels and pin-fins onto chip with heating and sensing devices was established successfully. The key achievements in this paper are such as: (i) The wafer level integration process flow and process parameters optimization were developed, (ii) Frontside metallization heaters and sensors critical dimensions measurement results were within specifications and good uniformity. This validated good process quality and consistency. Metal wet etch process conditions was optimized to ensure uniform line width coverage at wider range from 15µm to 200µm across full wafer. (iii) Linear correlation of metal sensor resistance reading over temperature range from 25degC to 160degC show fabricated metal thickness and properties are within specifications without defects. (iv) Microchannel depth and pin fins height was measured to validate DRIE etch process uniformity control. (v) Good alignment accuracy between opposite sides heaters and channels features.

Acknowledgments

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