

Study of Cu Pad Expansion with Surrounding Dielectrics for Hybrid Bonding

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Abstract

Copper/dielectric hybrid bonding technology is a key enabler for advanced chip-level (chip-to-chip, chip-to-wafer) or wafer-level (wafer-to-wafer) heterogeneous integration. In hybrid bonding, the initial room temperature bonding among the activated dielectrics is followed by Cu-to-Cu bonding at high-temperature anneal. The new dielectric materials are in the pathway toward lowering the thermal budget of the bonding process. In such an aspect, the Cu dishing could be controlled based on Cu thermal expansion. The annealing temperature is defined at which the thermal expansion of Cu should be greater than the dishing, that resulted from the damascene process. In this regard, the effect of the surrounding dielectric material around the Cu and the expansion of Cu over the applied thermal cycle need to be understood. This study focuses on the dependency of the Cu expansion with various surrounded dielectric, metal pad pitch, and its shapes, using the Finite Element Analysis (FEA) method with Ansys mechanical.

Introduction

Advanced packaging with vertical integration is a key enabling technology for high performance and low power system applications [1] and wafer bonding is a key enabler for the vertical stacking of multi-functionalities. High interconnect densities required for high functional integration demands fine-pitch interconnection. Hybrid bonding technology helps facilitate improvement in interconnect density [2]. In addition, applications like chip-stacked high bandwidth memory (HBM) require low thermal-budget hybrid bonding to mitigate memory losses due to high process temperature. In such a scenario, the industry is looking for an alternative dielectric for lowering the thermal budgets during dielectric bonding [3]. Even though we reduce the thermal budget of dielectric, the reduction in the thermal budget also necessary for overall reliable hybrid bonding

However, good metal interconnection at fine pitches depends on the dishing of Cu resulting from the damascene process. Dishing is unavoidable and achieving zero dishing in the CMP process is challenging. If the expansion of Cu is less than the dishing at the annealing temperatures, the formation of voids at the Cu-Cu bonding interface is unavoidable. Thus, Cu pad expansion during the hybrid bonding of fine-pitch structures is a major consideration. In addition, the effect of the surrounding dielectric matrix in Cu pad expansion still needs to be understood. This study will help understand Cu expansion in the presence of a surrounding dielectric matrix. This will be helpful for the integration of new dielectrics for better Cu interconnections at fine pitches for future advanced packages.

Finite Element Analysis (FEA) Methodology

For understanding Cu expansion with surrounding dielectric, we use Ansys mechanical FEA simulation method.

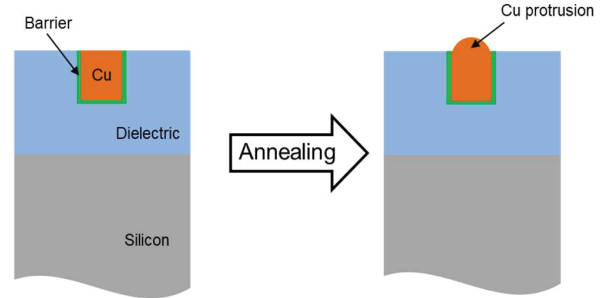


Fig. 1. Schematic of Cu protrusion after annealing

The following Cu pad structure, as shown in Fig.1, is considered in the present study. The schematic shows one Cu pad and the materials surrounding it, namely the barrier, dielectric, and silicon under the dielectric layer. As illustrated in Fig.1, before annealing, the Cu surface is assumed to be flush to the dielectric surface. After annealing at elevated temperature, Cu protrusion takes place due to thermal expansion and creep deformation.

Two Cu pad designs are considered in the present study, namely a square-shaped Cu pad and a round shape Cu pad. Both designs are shown in Fig. 2. The FEA model consists of 2x2 sets of Cu pads. Fig. 3 gives the boundary conditions applied in the FEA mode. Symmetric conditions are applied on the two side faces of the FEA model, while coupled constraint is applied on the other two side faces. With such boundary conditions, the FEA model is extended to a 4x4 Cu pad geometry.

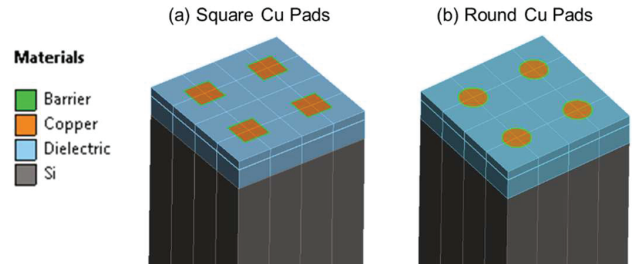


Fig. 2. Schematic of Cu protrusion after annealing

The thermomechanical material properties applied in the present FEA simulations are listed in Table 1. Three dielectric material candidates that are CMOS compatible are considered, i.e., silicon nitride, TEOS oxide, and silicon carbon nitride. As Cu creep plays a very important role for Cu to Cu bonding, its creep properties are included in the simulation [4].

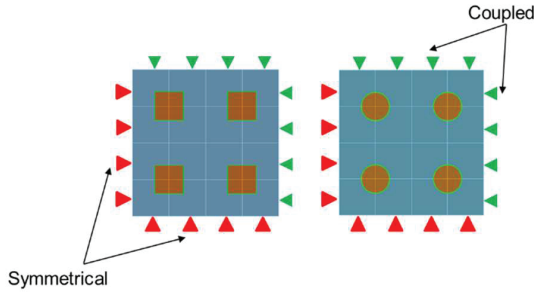


Fig. 3. Boundary condition set-up in FEA model

Materials	Young's modulus (GPa)	Poisson's ratio	CTE (ppm/°C)
Copper	117	0.34	17
Si	131	0.28	2.6
Ti	120	0.36	8.41
SiO ₂	73	0.17	0.5
SiCN	70	0.20	5.17
SiN	156	0.27	3.27

The annealing profile shown in Fig. 4 is applied as thermal loading in the FEA simulations. It can be divided into three stages, i.e., ramp-up stage, holding stage and cool-down stage.

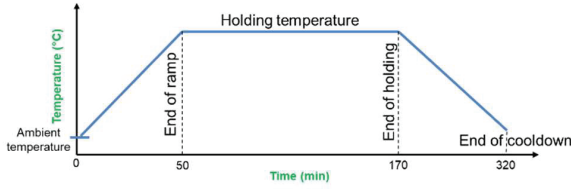


Fig. 4. Annealing profile showing the temperature vs time

In order to study the Cu protrusion behavior during annealing and how it is affected by the design and process conditions, several variables are considered in the FEA analysis. The design variables are defined in Fig. 5, whereas the ranges considered for these variables are shown in Table 2.

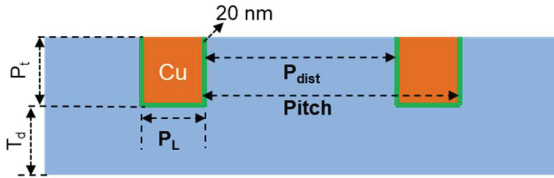


Fig. 5. Definition of design variables considered

Variables	Unit	Values
Annealing temperature	°C	250, 350, 400
Pad to Pad distance P_{dist}	μm	0.25, 0.4, 0.5, 1.5, 3
Cu size P_L	μm	0.25, 0.4, 0.5, 1.5, 3
Cu diameter P_L	μm	1, 3
Cu thickness P_t	μm	0.35, 0.5, 0.7, 1
Dielectric thickness T_d	μm	0.75, 1, 1.5, 2

Results and Discussion

The FEA results for Cu protrusion during the annealing temperature cycle are shown in Fig.6. The Cu pad considered in this case is square shaped and the dielectric is SiO₂. Cu pad size P_L is 1 μm , pad to pad distance P_{dist} is 1.5 μm , and the pad thickness P_t and dielectric thickness T_d are 0.35 μm and 0.75 μm , respectively.

From Fig.1, it is observed that Cu protrusion takes place once the temperature increases. In the low temperature range, i.e., approximately below 150°C, Cu protrudes mainly due to pure thermal expansion, which is reversible. When the annealing temperature goes beyond 200°C, Cu creep deformation becomes noticeable. Therefore, the Cu protrudes more rapidly. When the annealing temperature is held at its maximum value of 350°C, Cu protrusion continues purely due to creep deformation. At the end of the holding stage, Cu protrusion reaches its maximum value. Once the cool-down stage starts, the Cu protrusion reduces due to thermal contraction. However, the irreversible creep deformation remains at the end of cool-down. Therefore, the total Cu protrusion incurred after annealing is 2.4 nm, in this case.

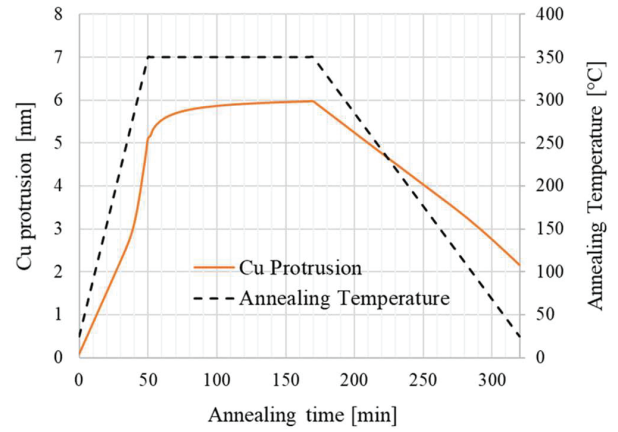


Fig. 6. Cu protrusion during annealing (square Cu pad, SiO₂ dielectric, $P_L=1 \mu\text{m}$, $P_{dist}=1.5 \mu\text{m}$, $P_t=0.35 \mu\text{m}$, $T_d=0.75 \mu\text{m}$)

In the subsequent section, the effect of some design variables and annealing temperature on Cu protrusion are examined.

Effect of Cu Pad Design, Dielectric material and Annealing Temperature on Cu Protrusion

The effect of three annealing temperature on Cu protrusion is studied next, with the other variables remaining the same. Cu protrusion at the end of the ramp-up stage, end of holding and end of cool-down are plotted in Fig. 7.

It shows that at low annealing temperature of 250°C, Cu creep deformation is insignificant. By the end of cool-down, Cu protrusion is merely 0.2 μm , which may be insufficient to establish proper Cu-to-Cu bonding. However, the Cu protrusion after annealing could be increased to 2.4 μm and 3 μm by raising the annealing temperature to 350°C and 400°C, respectively. Therefore, to achieve sufficient Cu protrusion for Cu-to-Cu bonding, a high annealing temperature is desirable.

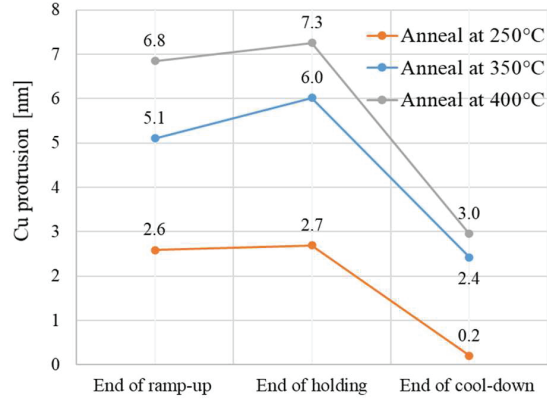


Fig. 7. Cu protrusion at end of different annealing stages for different annealing temperature (square Cu pad, SiO₂ dielectric, $P_L = 1 \mu\text{m}$, $P_{dist} = 1.5 \mu\text{m}$, $P_t = 0.35 \mu\text{m}$, $T_d = 0.75 \mu\text{m}$)

In this study, square and round pad shapes are modelled. Cu protrusions at the end of different stages for square and round pads are compared in Fig.8. It indicates clearly that comparable Cu protrusion is achieved with annealing for both Cu pad designs. With round shape, Cu protrusion is slightly higher by 15% in this case. The final Cu protrusion is 2.8 μm and 2.4 μm for round Cu pad and square Cu pads, respectively. A possible reason is that at the same size/diameter of 1 μm , the round Cu pad has smaller cross-sectional area than that of the square pad. Therefore, the side surface that can resist the constraint from the surrounding dielectric is smaller for round pad. Thus, the Cu pad tends to expand more in the vertical direction than in the lateral direction. However, this influence is not significant.

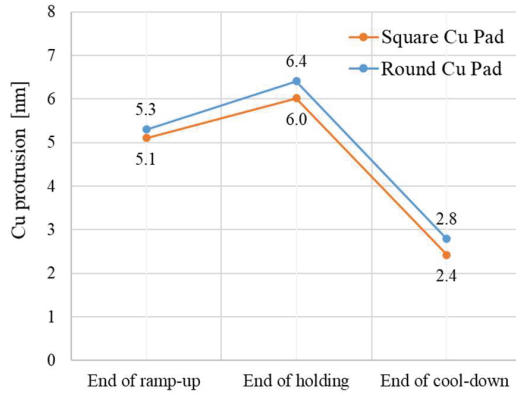


Fig. 8. Cu protrusion at end of different annealing stages for different Cu pad shape (SiO₂ dielectric, $P_L = 1 \mu\text{m}$, $P_{dist} = 1.5 \mu\text{m}$, $P_t = 0.35 \mu\text{m}$, $T_d = 0.75 \mu\text{m}$, annealing temperature = 350°C)

To assess the effect of pad size, two scenarios are considered, i.e., with the same Cu pad pitch over pad size ratio and with different Cu pad pitch over pad size ratio. Fig. 9 shows the Cu protrusion at different stages for different Cu pad size P_L . In this case, the pad pitch over pad size ratio is fixed at 2. It is noticed that for the same pad pitch over pad size ratio, Cu protrusion increases with the pad size. This is due to the larger Cu volume in the large Cu pad compared to the small pad.

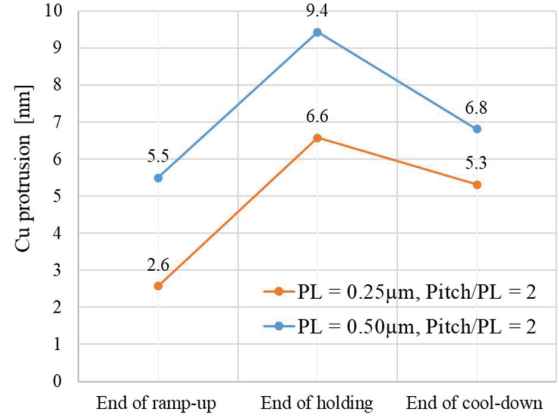


Fig. 9. Cu protrusion at end of different annealing stages for different Cu pad size and same pitch over pad size ratio (square Cu pad, SiO₂ dielectric, Pitch/ $P_L = 2$, $P_t = 0.5 \mu\text{m}$, $T_d = 1 \mu\text{m}$, annealing temperature = 350°C)

On the other hand, for different pitch over pad size ratios, the observation obtained from Fig. 9 does not apply. Fig.10 compares two cases with both different pad size and different pitch over pad size ratio, where the small pad has large pitch over pad size ratio, and the large pad has smaller pitch over pad size ratio. The results in Fig.10 indicate that the Cu protrusion is affected simultaneously by both variables. The difference between the two cases is small. The increment in the Cu protrusion for the large pad is offset by the reduction for small pitch over pad ratio. This also suggests that the Cu protrusion increases with the pitch over pad ratio. However, the effect may be expected to diminish when the pitch over pad ratio reaches a certain threshold.

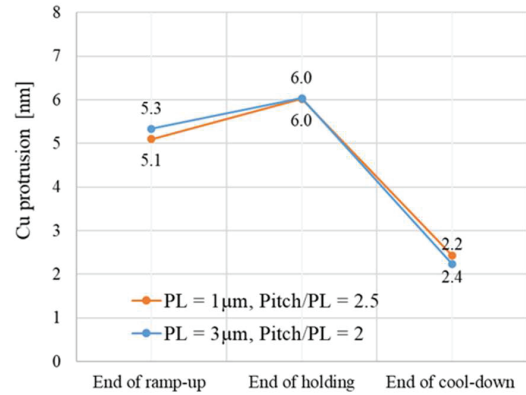


Fig. 10. Cu protrusion at end of different annealing stages for different Cu pad size and pitch over pad size ratio (square Cu pad, SiO₂ dielectric, $P_t = 0.35 \mu\text{m}$, $T_d = 0.75 \mu\text{m}$, annealing temperature = 350°C).

Similarly, the effect of pad thickness is studied, and the results could be found in Fig.11. The observation indicates that larger pad thickness leads to larger Cu protrusion for a given pad size. This is expected as larger Cu protrusion is expected from a larger Cu volume.

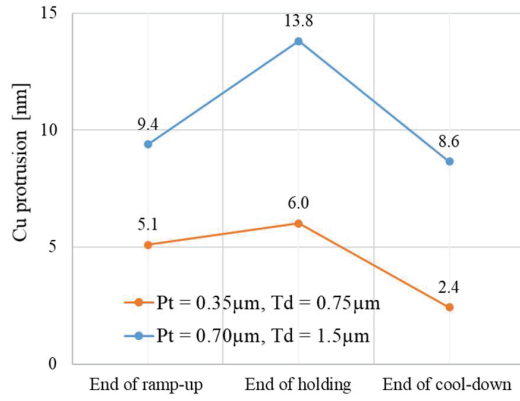


Fig. 11. Cu protrusion at end of different annealing stages for different pad thickness and dielectric thickness (square Cu pad, SiO₂ dielectric, $P_L = 1 \mu\text{m}$, $P_{dist} = 1.5 \mu\text{m}$, annealing temperature = 350°C)

It is also important to study the effect of different dielectric material candidates on Cu protrusion during the annealing process. However, the FEA results for Cu protrusion shown in Fig.12 suggest that the effect is not significant for the three dielectric material candidates considered in this study, i.e., SiO₂, SiCN and SiN. This applies to both small pads (Fig.12) and large pads (Fig.13). However, based on the small differences in Cu protrusion among these three dielectric materials, SiO₂ yields the smallest Cu protrusion while SiCN and SiN allow for similar, but slightly higher Cu protrusion over SiO₂. This observation is in line with the material properties of these materials. SiO₂ has a smallest CTE compared to SiCN and SiN.

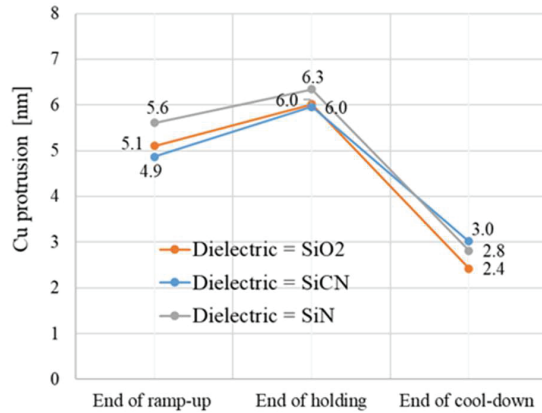


Fig. 12. Cu protrusion at the end of different annealing stages for different dielectric material (square Cu pad, $P_L = 1 \mu\text{m}$, $P_{dist} = 1.5 \mu\text{m}$, $P_t = 0.35 \mu\text{m}$, $T_d = 0.75 \mu\text{m}$, annealing temperature = 350°C)

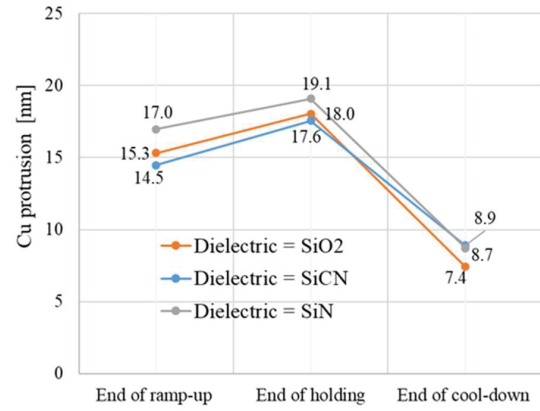


Fig. 13. Cu protrusion at end of different annealing stages for different dielectric material (square Cu pad, $P_L = 3 \mu\text{m}$, $P_{dist} = 3 \mu\text{m}$, $P_t = 1 \mu\text{m}$, $T_d = 2 \mu\text{m}$, annealing temperature = 350°C)

Conclusions

Cu protrusion during the annealing process is investigated using FEA methodology. Several design, process and material variables are studied to delineate their effect on Cu protrusion. The following are some of the major findings:

- For all the parameters considered, Cu protrusion varies from the sub-nanometer level to a maximum of 20 nm.
- Annealing temperature of 350°C and above is required to achieve reasonable Cu protrusion.
- With the same pitch over pad size ratio, Cu protrusion increases with the pad size.
- Large pad pitch over pad size ratio leads to larger Cu protrusion. This effect diminishes if the pad pitch over pad size ratio reaches a certain characteristic value.
- Large pad thickness leads to large Cu protrusion for a constant pad size.
- Round Cu pad has slightly larger Cu protrusion over square Cu pad. However, the difference is relatively small.
- Among the three dielectric materials considered, SiCN and SiN allow for similar Cu protrusion. On the other hand, SiO₂ results in a smaller Cu protrusion.

Acknowledgments

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