Cu and barrier CMP process development with fine 1µm Cu bond pad and 2.5 µm pitch for Wafer-to-wafer Hybrid Bonding

Sangita Chaki Roy, Chen Gim Guan, Nandini Venkataraman, Wen Lee and Navab Singh
Institute of Microelectronics, Agency for Science, Technology and Research (A*STAR), Singapore
chakiroys@ime.a-star.edu.sg

Abstract

Fine pitch hybrid bonding is evolving as a vital advanced permanent bonding in 3D IC technology for its low cost and providing shorter global interconnect length. Chemical mechanical planarization (CMP) is a critical process step for realizing uniform Cu dishing control all over the wafer for successful W2W hybrid bonding. In this paper, we have investigated the effect of various CMP conditions using a three-step CMP process, on Cu dishing, intra-die oxide planarity, and surface roughness and have attempted to understand the dishing control mechanism for our developed CMP process. Atomic force microscopy has been used to characterize the dishing and non-uniformity of the wafers. We have demonstrated controlled dishing <3 nm, intra-die oxide planarity <0.6 nm, and Cu/oxide surface roughness <0.3 nm for 1 µm Cu bond pad size and fine pitch ~2.5µm. Our analysis indicates that the balanced combination of HPP and LPP with polish time control for Cu and barrier polishing helps to control the Cu pad dishing and achieve high uniformity all over the wafer. Our study outlines a way for the optimization of Cu and barrier CMP processes for fine-pitch Cu pads for hybrid bonding applications.

Introduction

Hybrid bonding has garnered significant attention in recent years with exciting potential product applications in 3D integration. As well as being used in the high-volume manufacturing of CMOS image sensors, hybrid bonding (HB) is also a key enabling technology in 3D integration, allowing multiple dies to be stacked via dense interconnects at the wafer-to-wafer (W2W) or chip-to-wafer (C2W) level. In the case of W2W hybrid bonding, hybrid bonding at fine interconnect pitches down to 500 nm with adequate overlay has been demonstrated recently by various groups [1-2]. Hybrid bonding involves bonding between wafer surfaces having damascene-like structures with copper pads embedded in a dielectric. While spontaneous dielectric-to-dielectric bonding occurs upon contact at room temperature via van der Waals bonds, during further thermal annealing, Cu-to-Cu bonding occurs by Cu expansion and diffusion across the bonding interface. To achieve a void-free bonding interface, surface preparation through chemical mechanical polishing (CMP) is key, with excellent global and local planarity, low surface roughness, and controlled Cu dishing (typically <5 nm) required. It is well-known that Cu dishing depends on the pattern density and linewidth, while pattern density differences across the die may lead to intra-die non-planarity. In addition, recipe parameters (e.g., applied pressure, polishing duration), consumable configuration (e.g., choices of pad and slurry composition), and tool hardware configuration also contribute to Cu dishing variations.

Fig. 1 exhibits the schematic cross-section of Cu dishing in the Cu bond pads and the intra-die oxide planarity (referred to as "global oxide protrusion", heretofore). Last few years, Cu dishing control by CMP process development at a fine pitch in Cu/SiO_2 hybrid bonding has been explored in various directions such as utilizing a multi-step CMP approach using an extra deposition layer followed by a CMP polish methodology, the Cu dishing control by adding an extra CMP step alongwith investigating various CMP slurries for fine-pitch W2W hybrid bonding [3-4]. However, very little focus has been put on understanding a balanced optimization of process parameters such as polishing pressure and time for dishing control for fine pitch bond pads. In this paper, we investigate the CMP process development for 2.5µm pitch/1µm Cu pad structures with the goal of achieving dishing <3 nm and minimizing "global oxide protrusion" (<0.6 nm) for W2W HB.

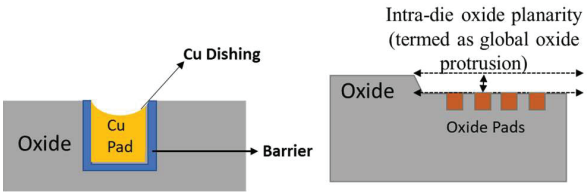

Fig. 1. Schematic illustration of Cu dishing and intra-die planarity in fine pitch Cu pad device.

Experimental

300 mm patterned silicon wafers with 1 µm Cu pads and 2.5 µm pitch were prepared using a standard single Cu damascene process sequence involving lithography patterning, dielectric (silicon dioxide) etching, PVD Ti barrier/Cu seed layer deposition, and Cu electroplating. A three-step CMP process was then developed to planarize these wafers, with the goal of meeting the key hybrid bonding requirements. Commercially available Cu and barrier slurries have been used for the CMP process development. The planarized bonding surfaces were then evaluated for Cu dishing, global oxide protrusion, and surface roughness using atomic force microscopy (AFM) at the wafer center and edge. The scan area used for Cu roughness measurement is 0.5µmx0.5µm, for oxide roughness is 2µmx2µm, the dishing measurement for Cu pads is 10µmx10µm and global oxide protrusion is 80µmx80µm, respectively. Wafers were then bonded and annealed using standard processes and evaluated for bonding void defects using IR imaging.

Results

As the Cu pad size and the bonding pitch become ultra-fine, achieving highly controlled and uniform Cu dishing across the die with various pattern densities and across the

wafer becomes highly complex. The failure in proper control of the crucial parameters can lead to poor bonding quality and consequently to electrical connectivity failure between the connecting pads.

In this paper, to achieve good dishing control for fine pitch and smaller Cu pads, we have tried to achieve the required key parameters by recipe parameter optimization (applied pressure and polishing duration) with a fixed CMP slurry composition, oxidizer ratio, and CMP pad. Three-step CMP processes with different combinations of polishing pressures along with fixed time polishing (FTP) have been set up for the Cu and barrier polishing experiments. Table 1 shows the details of the three process recipes i.e., Process 1, Process 2, and Process 3 with different applied pressure and fixed time at various recipe sub-steps.

Table 1. CMP Process parameters.

No	CMP Step	Process 1	Process 2	Process 3
1	**Step 1**-Cu Bulk Planarization	HPP (High-Pressure Polish)	HPP	HPP
2	**Step 2**- Barrier Polish	HPP	HPP	LPP (Low-Pressure Polish)
3	**Step 3**- Barrier Overpolish (By Fixed Time Polish FTP)	HPP (50s)	LPP (50s)	LPP (10s)
	Cu Touch up Polish (by FTP)	-	LPP (5s)	HPP (25s)

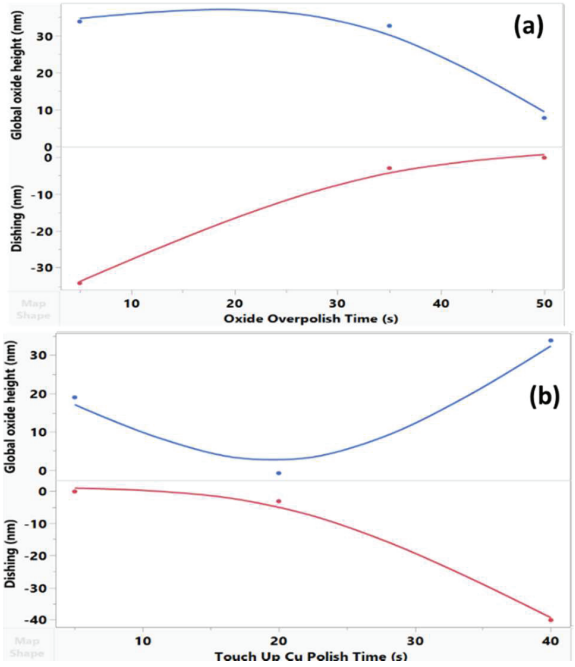

Fig.2. Cu dishing and global oxide variation with (a) barrier overpolish time and (b) touch-up Cu Polish time.

As can be seen from Table 1, the copper overburden after the damascene process is planarized in step 1, while in step 2, the barrier is planarized exposing the oxide. In step 3, we first

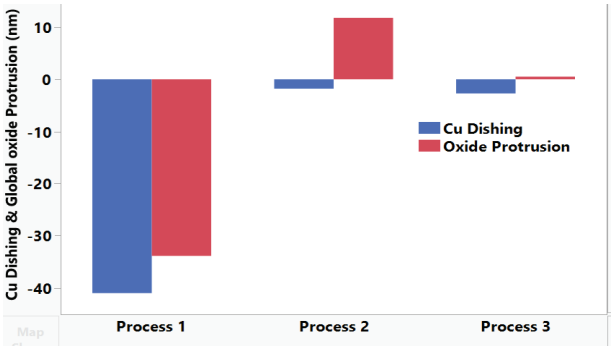

Fig. 3. shows the (a) Cu dishing and global oxide protrusion variation with three Process recipes, optimized Process 3, respectively.

overpolish the barrier, reducing the oxide height, and then introduce a Cu touch-up polish step for creating controlled dishing. Next, we tried to understand the effect of single barrier overpolish (with standard barrier slurry) or touch-up Cu polish (with standard Cu slurry) on Cu dishing and global oxide protrusion. Fig. 2(a) shows the effect of barrier overpolish time in LPP on Cu dishing and global oxide protrusion as overpolish time increases from 5s to 50s. As can be seen, the Cu dishing reduces rapidly from -34.23 nm to -0.06 nm while the global oxide protrusion reduces from +33.86 nm to +7.81 nm, where the positive sign convention shows protrusion, and the negative sign convention shows dishing. The global oxide protrusion value was too large even with 50s barrier overpolish.

Furthermore, we explored the introduction of touch-up Cu overpolish only [with no barrier overpolish, HPP] after step 2, to evaluate its effect on Cu dishing and global oxide protrusion. Fig. 2(b) shows that as the touch-up Cu overpolish time increases from 5s to 40s, the dishing increases rapidly from -0.082 nm to -40.1 nm, while global oxide protrusion increases from +19 nm to +33.86 nm. The observed trend in dishing and global oxide protrusion may be explained by the material removal rate (MRR) difference between the Cu and barrier/oxide layers in the Cu slurry used for this step.

From the above systematic experiments, we understand that for obtaining required Cu dishing and global oxide protrusion with good uniformity all over the wafer, it is imperative to explore optimal process conditions at both the barrier overpolish and Cu touch-up polish steps. After undergoing many optimization experiments, we have finalized the combination of HPP and LPP barrier overpolish followed by a touch-up Cu polish after our set steps 1 and 2.

Fig. 3 shows that with CMP Process 1, where Cu touch-up polish step was not introduced, very high values of Cu dishing and global oxide protrusion were obtained. However, with the introduction of step 3 in Process 2 [Cu Touch up Polish for dishing (by Fixed Time Polish FTP)], the achieved Cu dishing was -1.8 nm (low) and global oxide protrusion was 11.8 nm (medium) as depicted in Fig.3. Finally, in Process 3, we used a more controlled and optimized combination of HPP, LPP and FTP to attain the required Cu dishing of -2.69 nm (medium) < 3 nm and global oxide protrusion of 0.503 nm (low) < 0.6 nm.

Atomic force microscopy (AFM) has been utilized for characterizing Cu dishing and sub-nanometer global oxide protrusion with respect to the CMP process optimization parameters. Fig. 4 shows the effect of polishing pressures on the Cu bonding pad and global oxide protrusion for the three processes. As can be seen, for process 1, with HPP polishing for Cu and barrier polishing, very high dishing and global oxide protrusion are obtained (Cu dishing 40.1 nm & global oxide protrusion ~33.86 nm). As the polishing is done with LPP in process 2 with the barrier (longer time) & and touch-up Cu polishing (shorter time), there is a gradual reduction of Cu dishing (-1.8 nm and global oxide protrusion 11.8 nm). The 3D image shows that the global oxide protrusion is still quite high even though the Cu pad dishing is well in the range < 3nm. Finally, in Process 3, when we overpolish the barrier with LPP for a shorter time (10s) and then touch-up Cu polishing is done with HPP for a longer time (25s), the dishing obtained is -2.69 nm and global oxide protrusion is 0.503 nm. Moreover, the Cu roughness of the bonding pad area is very high ~ 2.36 nm in Process 1, but as we use the combination of LPP and HPP in Process 2 and 3, respectively,

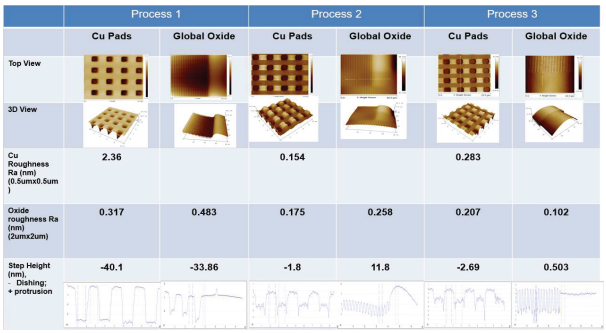

Fig. 4. The AFM scan results for Process 1, 2, and 3.

the Cu roughness is well below 0.5 nm. Additionally, the oxide roughness is well controlled from 0.483 nm in Process 1 to 0.258 nm for Process 2 and 0.102 nm for Process 3. Thus, we obtain the required hybrid bonding dishing < 5 nm and global oxide protrusion <0.6 nm along with the surface Cu and oxide roughness <0.5nm.

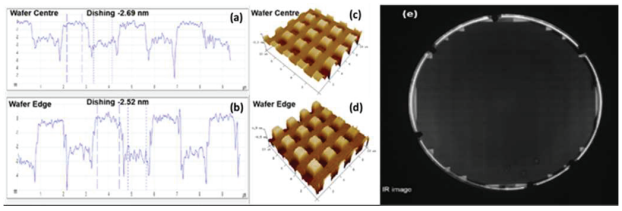

Fig. 5. Comparison of (a & b) Cu pad dishing for wafer center and edge, (c & d) AFM scan images, (e) IR image of hybrid bonded for optimized process 3.

Figure 5 (a) & (b) displays Cu dishing in the wafer center and edge of the wafer using optimized Process 3. The Cu dishing attained is consistent between the center and edge. Similarly, Fig. 5(c) and (d) show the three-dimensional AFM view of the

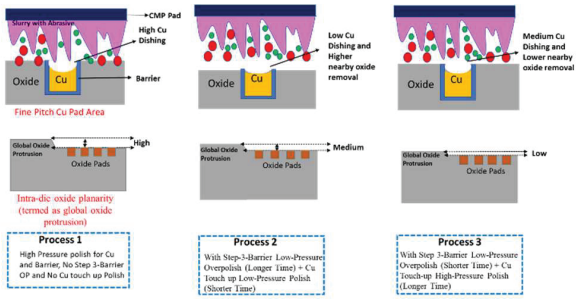

Fig. 6. Schematic illustration of the fine pitch Cu bond pad device under different conditions of CMP.

Cu dishing achieved in the wafer center and edge with high uniformity which is the balanced effect of the material removal rate optimization and improved topography effect. Meanwhile, Fig. 5(e) shows the IR image of the wafer-to-wafer hybrid bonded pair of wafers. The bonded wafers show good uniformity with more than 90% bonded area with no visible voids or defects.

CMP is a critical step in HB with key challenges of optimal dishing control for achieving good Cu-Cu bonding during post-bonding anneal. The optimized CMP process can be understood by a simple schematic diagram as shown in Fig. 6., showing the fine pitch Cu pad structure, global oxide protrusion, CMP polishing pad, and CMP slurry with abrasive and additives. Polishing with HPP differs from LPP in the landing mechanism, i.e., the contact force on the Cu pad surface and the surrounding oxide area. As discussed previously, in step 1, the copper overburden after the damascene process is planarized by HPP where the surface is approached with a larger contact force ("hard landing"), leading to more Cu removal due to higher material removal rate. Similar to step 1, in step 2, the barrier region is also polished by HPP for clearing the barrier material with high contact force and thus higher material removal rate. In our process, step 3 is the most critical step. In this step, we first overpolish the barrier, reduce the dielectric/global oxide protrusion, and then introduce a Cu touch-up polishing for creating dishing. HPP is crucial for a high material removal rate while low-pressure polishing is essential for a uniform removal rate across the wafer, thus attaining good surface topography for various pattern densities. Thus, it is essential to optimize the fine-pitch Cu CMP using HPP and LPP with fixed-time polishing to achieve low Cu dishing, smoother surface, and global flatness. As depicted in Fig. 6, it shows the final polish stage of process 1, and step 3 of Process 2 and 3. The conditions for Process 2-Barrier Low-Pressure Overpolish (Longer Time) + Cu Touch-up Low-Pressure Polish (Shorter Time) and Process 3-Barrier Low-Pressure Overpolish (Shorter Time) + Cu Touch-up High-Pressure Polish (Longer Time). Barrier polishing removes the barrier material Ta and exposes TEOS where barrier slurry has high selectivity for barrier material Ta/TEOS and a very low Cu removal rate compared to Ta/TEOS. In general, low-pressure polishing creates low dishing while high-pressure polishing produces high dishing due to their respective material removal rate. However, with a short polishing time of the barrier layer, the barrier material Ta/TEOS is removed, and low Cu dishing is produced due to different removal rates of barrier slurry for barrier and Cu. Thus, when a synergistic step 3 is explored, the

barrier overpolish in HPP for a longer polishing time and an immediate Cu touch-up polishing in LPP for a shorter time creates low Cu dishing and higher nearby oxide removal. However, with a shorter barrier overpolishing in LPP and a following Cu touch-up polishing in HPP for a longer time creates medium Cu dishing and lower nearby oxide removal. Our analysis indicates fine (2.5µm) pitch and smaller (1µm) Cu pad structures need sufficiently balanced HPP and LPP with fixed time CMP to achieve the required Cu dishing alongwith intra-die oxide planarity and surface roughness for void-free hybrid bonding.

Conclusions

In this paper, we have explored the CMP process development for 2.5 µm pitch/1 µm Cu pad structures with the goal of achieving Cu dishing <5 nm for W2W HB. The collaborative impact of using the combination of high pressure, and low pressure, with fixed-time control steps for planarizing hybrid bonding pad layers has been assessed. Due to the high material removal rate, the Cu bulk is planarized with HPP. The barrier slurry has high selectivity and removal rate for the barrier; thus, the barrier thinning can be planarized with HPP. Meanwhile, for barrier overpolish with low-pressure polishing for a shorter time followed by high-pressure polishing of Cu touch-up using a longer time is effective in creating the controlled dishing < 3 nm, global oxide protrusion < 0.6 nm, and Cu/oxide surface roughness < 0.3 nm with high uniformity across the wafer. Our work paves a new approach for designing high-performance Cu and barrier CMP for controlling via dishing and intra-die oxide planarity with high uniformity for very small Cu bond pads for hybrid bonding.

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