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Citation: Applied Physics Letters **105**, 152104 (2014); doi: 10.1063/1.4898577
View online: http://dx.doi.org/10.1063/1.4898577
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/105/15?ver=pdfcov
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Influence of post-deposition annealing on interfacial properties between GaN and ZrO_2 grown by atomic layer deposition

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(Received 9 September 2014; accepted 6 October 2014; published online 16 October 2014)

Influence of post-deposition annealing on interfacial properties related to the formation/annihilation of interfacial GaO_x layer of ZrO_2 grown by atomic layer deposition (ALD) on GaN is studied. ZrO_2 films were annealed in N_2 atmospheres in temperature range of 300 °C to 700 °C and analyzed by X-ray photoelectron spectroscopy and high-resolution transmission electron microscopy. It has been found that Ga-O bond to Ga-N bond area ratio decreases in the samples annealed at temperatures lower than 500 °C, which could be attributed to the thinning of GaO_x layer associated with low surface defect states due to "clean up" effect of ALD-ZrO_2 on GaN. However, further increase in annealing temperature results in deterioration of interface quality, which is evidenced by increase in Ga-O bond to Ga-N bond area ratio and the reduction of Ga-N binding energy. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4898577]

GaN-based heterostructure devices such as high electron mobility transistors (HEMTs) have been used extensively for high frequency,[1] high power,[2] and low noise applications.[3] However, a layer of gallium sub-oxide (GaO_x) layer can be formed on GaN surface by reaction with oxygen even at room temperature.[4] Surface-related defect states associated with the GaO_x layer result in large current leakage[5] and severe current collapse at high frequency,[6] which may inhibit the further enhancement of device performance of GaN-based HEMTs. Recently, the insertion of a dielectric layer as the gate insulator and surface passivation layer in GaN-based metal-insulator-semiconductor HEMTs (MISHEMTs) is reported to mitigate the above issues.[7,8] By virtue of its high dielectric constant along with reasonably high conductance band offset (CBO) and valance band offset (VBO) aligned to GaN substrate,[9] ZrO_2 is a promising dielectric material candidate for GaN MISHEMTs. Excellent electrical characteristics of GaN MISHEMTs utilizing ZrO_2 as gate dielectrics are reported recently.[10–15] Nevertheless, several material issues should be considered for further improvement of the electrical properties for GaN MISHEMTs using ZrO_2 as gate insulators. Above all, the interface between dielectric layer and underlying GaN substrate is critical, and thermal stability of the dielectric layer at the interface is one of the most challenging requirements for application of ZrO_2 as a gate dielectric. However, so far, few studies have been carried out on the ZrO_2 dielectric layers on GaN, especially in regard with the interfacial properties between ZrO_2 and GaN. On the other hand, from device fabrication point of view, post-deposition annealing (PDA) could serve as an effective way to improve interfacial properties between high-k dielectric layer and semiconductor substrate for semiconductor devices. In this paper, a detailed investigation of the impact of post-deposition annealing on interfacial properties related to the formation/annihilation of interfacial GaO_x sub-oxide layer of atomic layer deposited (ALD) ZrO_2 on GaN is carried out by using X-ray photoelectron spectroscopy (XPS) and high-resolution transmission electron microscopy (HR-TEM).

ZrO_2 dielectric layers were deposited on GaN-on-sapphire substrates by using ALD method. The un-doped GaN-on-sapphire wafers were grown by Metal Organic Chemical Vapor Deposition (MOCVD) using a commercial reactor. For the investigation of ZrO_2/GaN interface, samples with 2 nm thick ZrO_2 on GaN surface were utilized for XPS measurements while ZrO_2 dielectric layers with a thickness of 10 nm were deposited for HR-TEM characterization. To deposit the ZrO_2 on GaN, the GaN-on-sapphire wafers were initially degreased for 10 min in acetone and subsequently in isopropyl alcohol (IPA). Before loaded into the ALD chamber, samples were treated by buffered oxide etchant (BOE) solution to remove surface native oxide and then followed by a rinse in flowing de-ionized (DI) water. ZrO_2 dielectric layers were deposited by a Cambridge Nanotech Savannah ALD system. The tetrakis-(diethylamino)-zirconium and H_2O were used as the precursors. Chamber pressure and substrate temperature were set at 0.6 Torr and 250 °C, respectively. During the deposition, sequential 400 ms and 40 ms pulse of H_2O and Zr sources were introduced into the chamber separately. After each pulse of precursor, the chamber was purged with N_2 for 6 s to remove excess precursors and by-product gases. High purity N_2 was used as the precursor carrier and purging gas. The growth rate for ZrO_2 was ~0.09 nm per ALD cycle. After dielectric layer deposition, different post-deposition anneals (PDAs) using rapid thermal annealing (RTA) in N_2 atmospheres for 30 s were performed under five different temperatures (300 °C, 400 °C, 500 °C, 600 °C, and 700 °C). The XPS measurements were carried

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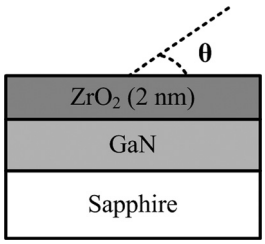

FIG. 1. A schematic cross-sectional diagram for GaN with 2 nm ALD-ZrO_2 dielectric layer for XPS measurements. The definition of take-off angle θ is also shown.

out using a monochromatic Al Kα X-ray source of energy 1486.7 eV. The spectra are curve-fitted with a combination of Gaussian and Lorentzian line shapes using a Shirley-type background subtraction. All peaks were referenced to the C 1*s* peak at 284.6 eV to compensate for any variations in the peak core-level positions due to binding energy (BE) shift caused by surface charging. The schematic structure of the sample used for investigating the ZrO_2/GaN interface by XPS measurements is shown in Fig. 1, where the photoelectron take-off angle is defined as θ. Here, the take-off angle θ was set at 15°, which enabled sensitivity analysis of chemical states at interface between ZrO_2 layer and GaN substrate.[9]

Ga 3*d* core-level XPS spectra obtained under different post-deposition annealing temperatures are depicted in Fig. 2. It can be seen from Fig. 2 that each Ga 3*d* spectrum could be deconvolved into two components, corresponding to the Ga-N and Ga-O bonds. The existence of the Ga-O spectrum for the as-deposited sample (indicated by N.A in Fig. 2) may be attributed to the parasitic oxidation of the GaN surface after cleaning during ALD deposition process.[16,17] Apparently, the Ga-N bonds show an obvious increase in binding energies (BEs) with the increase of annealing temperatures when the annealing temperatures are lower than 500 °C. Further increase in annealing temperature shows a reduction of the BEs. As a polar semiconductor, GaN surface is sensitive to fabrication process. Sharp upward band bending at GaN surface due to large polarization combined with possible surface Fermi-level pinning caused by surface defects and contaminations may occur.[18,19] In our previous report for ALD ZrO_2 on GaN, such strong upward band bending was observed through XPS measurements.[9] Meanwhile, as can be obtained from Fig. 2, the integrated XPS intensity of Ga-O bond to Ga-N bond ratio also shows variations related to annealing temperatures. For clarity, the dependence of Ga-N bond binding energies and ratio of the Ga-O to Ga-N XPS peak area on annealing temperatures are plotted in Fig. 3. It can be seen that the Ga-N bond binding energies are strongly coincident with the ratio of Ga-O to Ga-N peak area. In general, the decrease in the ratio of Ga-O to Ga-N peak area leads to the increase of Ga-N bond binding energy. This suggests that the Fermi-level position at GaN surface is affected by surface-related defect states associated with GaO_x layer. The surface states contribute to upward band bending at GaN surface. A higher defect density at ZrO_2/GaN interface could cause stronger upward band bending thus lower Ga-N bond binding energy. The annihilation or formation of the gallium sub-oxide layer at the interface is highly related to annealing temperatures. Under annealing temperature of 500 °C, the Ga-N bond binding energy shows the highest value along with the smallest Ga-O to Ga-N peak area ratio. The decrease in Ga-O bond concentration may suggest a "clean up" effect, which is most likely due to the formation of a Ga-O-Zr environment to passivate Ga-O bond. Such clean up effect is widely reported on ALD deposited high-k dielectrics on III-V semiconductor interfaces such as Al_2O_3/III-As[20,21] and Al_2O_3/III-N.[22,23]

HR-TEM is used to further characterize the interfacial properties between ALD ZrO_2 and GaN. Cross sectional TEM micrograph for as-deposited sample (N.A) and samples annealed at 500 °C and 700 °C are shown in Fig. 4. Obviously, compared with the as-deposited sample, ZrO_2 thin films get further crystallized with the increasing of the annealing temperatures, which is consistent with the report in literature.[24] For the as-deposited film shown in Fig. 4(a),

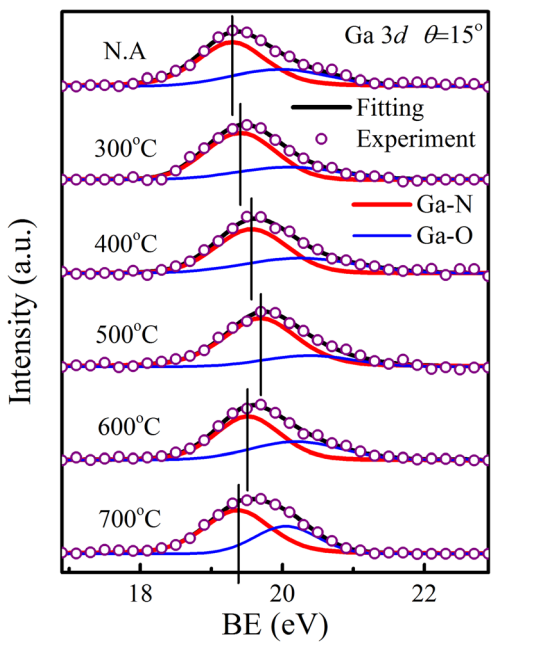

FIG. 2. The measured (open circles) and fitted (lines) XPS Ga 3*d* core-level spectra for ALD ZrO_2 on GaN samples measured at take-off angle θ of 15° under different PDA temperatures. The as-deposited sample is indicated as N.A.

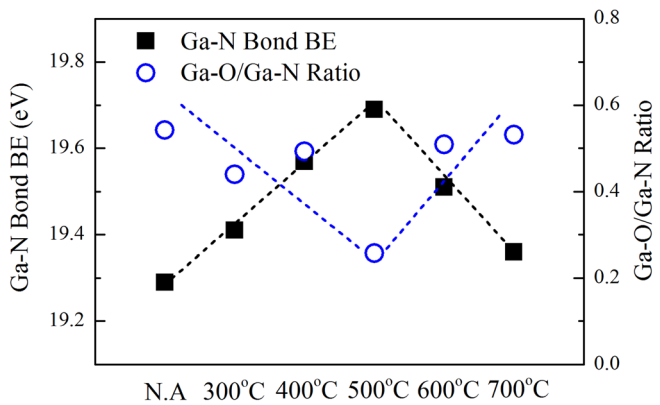

FIG. 3. Change of Ga-N bond BE and integrated XPS intensity ratio of Ga-O bond to Ga-N bond for ZrO_2/GaN samples under different PDA temperatures. The as-deposited sample is indicated as N.A, and the dashed lines are a guide for the eye to show the change trend.

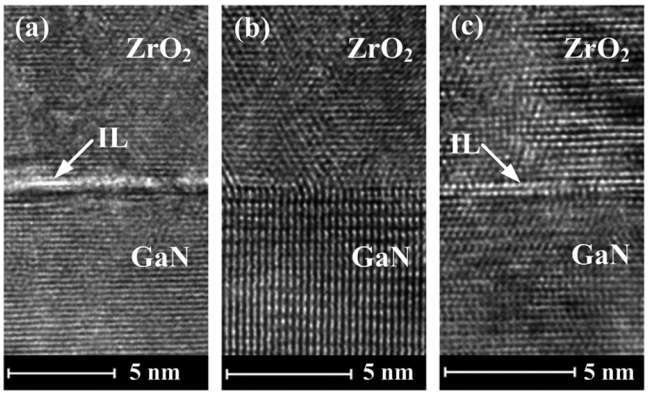

FIG. 4. Cross-sectional TEM images of the ZrO_2 dielectric layers on GaN: (a) as-deposited (N.A) and (b) with a 500 °C post-deposition annealing in N_2 for 30 s and (c) with a 700 °C post-deposition annealing in N_2 for 30 s. The interfacial layer is indicates as IL.

an obvious interfacial layer could be found. While, an abrupt interface without any interfacial layers is observed for sample annealed under 500 °C. This may further indicate the clean up effect for ALD ZrO_2 on GaN at annealing temperature of 500 °C. For the sample annealed at 700 °C in Fig. 4(c), re-formation of interfacial layer was observed. This could be attributed to the oxidation at the ZrO_2/GaN interface due to oxygen segregation at higher annealing temperatures.[25,26] The observation of regrowth of interfacial layer at higher annealing temperatures is in consistence with the reduction of Ga-N binding energy. The annihilation or formation of the gallium sub-oxide GaO_x interfacial layer at the interface between ZrO_2 and GaN during the post ALD annealing is dependent on annealing temperatures. The decrease in Ga-O to Ga-N peak area ratio in the samples annealed at the temperatures below 500 °C can be attributed to the reduction of Ga-O bonds due to the passivation of Ga-O bond through the clean up effect. While oxidation at the ZrO_2/GaN interface due to oxygen segregation at higher annealing temperatures may lead to the increase of Ga-O to Ga-N peak area ratio.

In conclusion, the effect of post-deposition annealing in N_2 atmospheres under different annealing temperatures on interfacial properties of ALD ZrO_2 on GaN is studied by XPS and HR-TEM analysis. The experimental results reveal that the ZrO_2/GaN interface quality can be effectively improved by post-deposition annealing in N_2 ambient at a temperature below 500 °C. This could be attributed to the thinning of interfacial GaO_x layer associated with low surface defect states due to the clean up effect of ALD-ZrO_2 on GaN. Deterioration of the interface quality due to re-formation of interfacial layer at higher annealing temperatures is observed. The above results provide important process guidelines for the use of ALD ZrO_2 as the high-k dielectrics and passivation layers for GaN-based HEMTs.

This work was partially supported by A*Star SERC Grant 1021690130 and NTU-A*Star Silicon Technologies, Centre of Excellence Grant 1123510003.

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