Package-Level Microjet-Based Hotspot Cooling Solution for Microelectronic Devices

Yong Han, Boon Long Lau, and Xiaowu Zhang

***Abstract*— A package-level hotspot cooling solution using Si hybrid heat sink and diamond heat spreader has been developed. The hybrid heat sink combines the merits of both microchannel flow and microjet array impingement, and can enable high spatially average heat transfer coefficient of 18.9 × 10^4 W/m^2 K with low pumping power of 0.17 W. The liquid jet is designed to directly impinge on the surface of the diamond heat spreader. The eight hotspot heaters, each of size 450 × 300 μm^2, were fabricated on the Si thermal test chip. The solid-fluid coupling simulation has been conducted using heaters model for microfluid cooling capability investigation. A gates model in conjunction with the heaters model is used to predict the thermal performance of the GaN transistors with the developed cooling solution. Hotspot cooling capability as high as 10 kW/cm^2 was demonstrated and validated. The heating power density of 3.9 W/mm can be dissipated in GaN device, while maintaining the peak gate temperature under 200 °C.**

***Index Terms*— Hotspot cooling, micro-jet array impingement, micro-channel, diamond heat spreader.**

I. Introduction

HIGH heat flux removal is a major consideration in the design of a number of microelectronic devices, such as power amplifier [1]. The presence of hotspots will post huge challenge to the thermal management, as the heat dissipation concentrates on tiny areas, which could lead to highly non-uniform temperature distribution, thus diminishing the device performance and adversely impacting reliability [2]. The effective thermal management of the hotspots will be a key to enable the technology to reach its full potential.

Micro-Jet array impingement can achieve large heat transfer coefficient, especially in the stagnation zones [3], [4]. Multiple micro-channels enable more effective energy exchange for the coolant with a larger surface area of multiple walls. Calame conducted an experimental study on the heat dissipation of the SiC micro-channel cooler [5]. A hotspot heat flux of 4kW/cm^2 was dissipated on a 1.2×5 mm^2 heat source. The numerical studies performed by Chen showed that micro-channel cooling system could improve the transistor-level power density [6]. Brunschwiler created micro-jet arrays with parallel fluid delivery and return architectures, and measured the heat transfer rate of 8.7×10^4W/m^2K [7]. Mizuno demonstrated a Si micro-channel cooler integrated with bump structure for GaN high power amplifiers (HPAs), and 0.3°C/W thermal resistance decrease was achieved [8].

In this letter, a package-level cooling solution integrating Si hybrid heat sink and diamond heat spreader has been developed for hotspot thermal management of microelectronic devices. The hybrid heat sink combines both micro-channel flow and micro-jet array impingement, can enable much higher heat transfer rates. To reduce the high concentrated heat flux for the heat sink to handle, a diamond heat spreader is adopted, and directly attached between the chip and the heat sink. The liquid jet is designed to directly impinge on the surface of the diamond heat spreader, and is constrained to flow along the micro-channel, then exit in two directions, as is shown in Fig.1. Thin bonding layer enabled reliable assembly and low thermal resistance. High hotspot cooling capability has been achieved and verified, suggesting the developed cooling solution can be applied to the GaN-on-Si devices. Large heating power density of the GaN transistors can be dissipated, while maintaining the peak gate temperature under operation limit.

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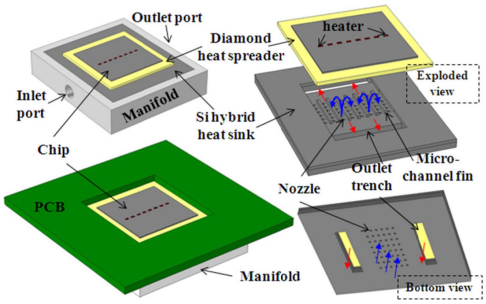

Fig. 1. Schematic images of the cooling structure with the exploded view and the bottom side view, and the flow arrow of the coolant in the Si heat sink.

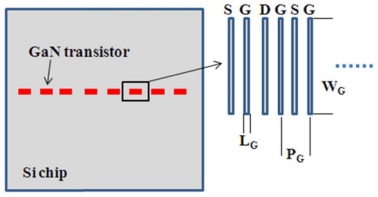

Fig. 2. Simplified layout of the GaN-on-Si power amplifier.

II. Fabrication and Experiment

For hotspot cooling capability evaluation, the experiments have been implemented on the customized Si thermal test chip of size 7×7mm^2 and thickness 100μm, with 8 hotspot heaters to mimic 8 GaN transistors. A top view of the typical GaN-on-Si power amplifier (PA) is shown schematically in Fig.2. Each transistor is composed of 10 gate fingers of gate width W_G, length L_G and gate-to-gate pitch P_G. The HEMT structure, which is magnified in the insert of the Fig.2, consists of source (S), drain (D) and gate (G).

During operation, the vast majority of the waste heat in the GaN PA is generated in the portion of each conductive channel that lies directly beneath the gate finger. The size of each hotspot heater is 450×300μm^2, which is a good

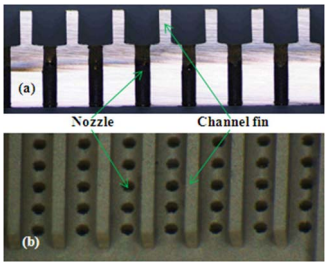

Fig. 3. Cross-section image (a) and micro-scope photo (b) of the fabricated Si micro-jet/micro-channel hybrid heat sink.

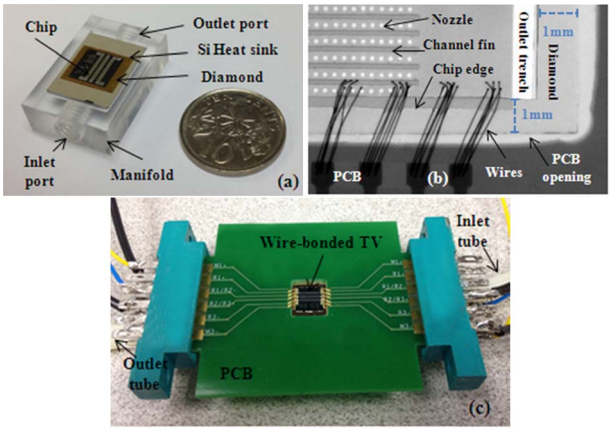

Fig. 4. Photo of assembled cooling structure (a), X-ray image of the test vehicle (TV) (b), and photo of the assembled TV (c).

approximation of an area of 10 gate fingers of 300μm W_G, 0.3μm L_G and 45μm P_G. The hotspot pitch is 690μm. The highly doped N-type resistors are built on Si test chip as the hotspot heaters [9].

A 300μm thick diamond heat spreader, which also works as the cover for the water-cooled heat sink, is fabricated by MPCVD, and is metalized with 1μm Ti/Pt/Au layer for bonding. The Si hybrid heat sink is fabricated using double-side DRIE process (Fig.3). On one side, there are 18 micro-channels of pitch 350μm, size 250×250μm^2, and length 3mm; On the other side, there is a 14×18 nozzle array of diameter 100μm, height 450μm, and pitch 250μm (along channel)/350μm (across channel). The Si heat sink is metalized with 4μm Au/Sn layer for chip-level thermal compression bonding (TCB) process.

The chip, heat spreader and heat sink are bonded together in one TCB step, in which the 280°C chuck holding time is 2 minutes and the compressive force is 49N. The size of the diamond heat spreader is 8.5×10mm^2. The minimum critical sealing dimension between the heat spreader and the heat sink is 1mm, as shown in Fig. 4(b). The bonding quality is checked, and no void is detected at the bonding layers. The test chip is wire bonded to the PCB, and DC power is supplied to the heaters. The inlet water temperature is 25°C. A micro-gear pump forces the water through a 15μm filter before entering the hybrid heat sink. The test chip temperature is measured using an IR camera at steady state (temperature variation ±0.1°C), which is reached within 30 minutes.

III. Simulation

The simulation models are constructed using COMSOL Multi-physics, as is illustrated in Fig.5. A solid-fluid coupling analysis is performed using the heaters model. The heat flux is loaded on each heater of area 300×450μm^2. The combined

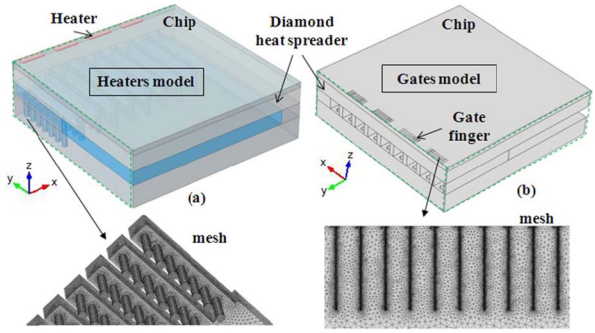

Fig. 5. Images of (a) 1/4 heaters model (fluid part in blue) and bottom view of fluid part mesh, and (b) 1/4 gates model and top view of gate heating region mesh. The symmetry boundary surfaces are outlined with dashed line.

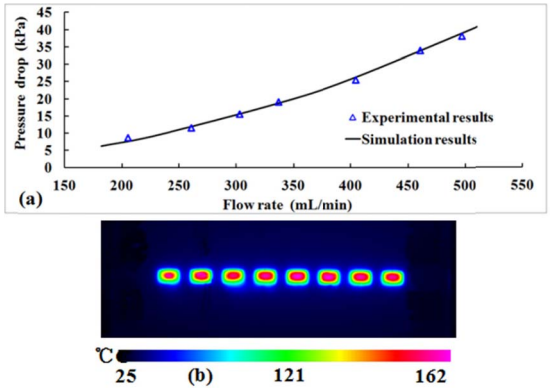

Fig. 6. Results of (a) pressure drop as a function of flow rate from the test and simulation, and (b) IR thermography image for 110W power dissipation.

effect of the heat convection and conduction is investigated to determine the optimized dimensions of the hybrid heat sink. The thermal performance of the GaN transistors is predicted using the gates model, which only include the solid part. The heat transfer coefficient distribution obtained from the heaters model is applied as the convective boundaries on the channel walls of this gates model. The thermal boundary resistance (TBR) is included between the GaN layer (2μm thick) and the Si substrate [2]. The heat flux is loaded on gate finger of area 300×0.3μm^2 in the gates model.

The solution was tested for mesh independency by refining the mesh size. Velocities and temperatures matched within 0.1% for both mesh sizes. The heaters model consists of around 2 million tetrahedral elements, while the gates model of 1.4 million. Based on the estimated low Reynolds number in the heat sink with flow rate 200∼500mL/min, it is considered to be operated in laminar regime. The no slip boundary condition is applied for the stationary wall. The temperature dependent material properties are considered in both simulation models.

IV. Results and Discussion

The results in Fig.6 illustrate the hydraulic and thermal performance of the test vehicle.

A stable flow motion inside the heat sink can be obtained. In order to maintain 400mL/min flow rate, the required pressure drop is around 25kPa. The hydraulic tests have been performed before and after 1000 cycles Thermal Cycling reliability test (−40°C ∼125°C). Consistent results have been obtained, and no leakage was observed. The flow stream line distribution is shown in Fig.7, based on the heaters model simulation results. When completely filled with moving water,

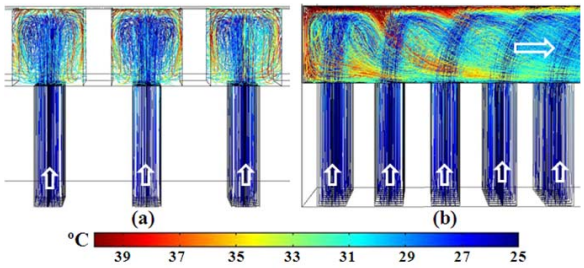

Fig. 7. Stream line distributions (the color represents the fluid temperature) (a) across channels, and (b) along channel, with 100W heating power.

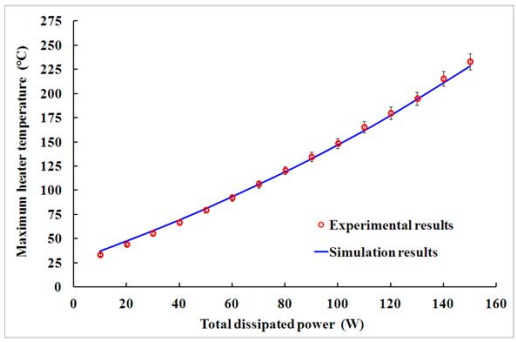

Fig. 8. Maximum heater temperatures as a function of the heating power from the test and simulation.

the pressure in the top micro-channel creates the flow to the confined micro-jets, impinging on the bottom surface of the diamond heat spreader.

The cooling capability is shown in Fig.8. The simulation results show excellent agreement with the experimental results. The maximum temperature occurs at the heaters located near the Si test chip center. The flow rate is set at 400mL/min, and the pumping power is 0.17W. The whole structure can dissipate 10kW/cm^2 (total heating power 110W) and 12kW/cm^2 (130W), while maintaining the maximum heater temperature under 165°C and 195°C, respectively.

The heat transfer coefficient in the heat sink is calculated using the equation $h = Q_W/(T_W - T_{in})$, in which Q_W is the heat flux, T_W is the channel wall temperature and T_{in} is the inlet water temperature. The overall spatially average heat transfer coefficient at the impingement wall in the channel is as high as 18.9×10^4W/m^{2}K. The local coefficient can be larger than 90×10^4W/m^{2}K in the stagnation zone. The cooling performance decreases rapidly away from the impingement zone. The maximum temperature rise caused by the bonding layer is less than 3%. The high concentrated heat flux from heater is effectively decreased by the direct-die-attached diamond heat spreader. For 110W power (10kW/cm^2), without diamond, the maximum heater temperature will reach as high as 220°C.

The gates model simulation is conducted to predict the performance of the GaN transistors with the developed cooling solution. The steady-state thermal analysis is performed, and the results are shown in Fig.9. The cooling capability of the Cu micro-channel heat sink (MCHS) designed in reference [10] is evaluated for comparison. With 0.2W pumping power for the Cu MCHS, the heating power density of 2.8W/mm can be dissipated, while maintaining the maximum gate temperature under 200°C. With 0.17W pumping power for the developed cooling solution, the heating power density of 3.9W/mm can be dissipated, which is 39.2% more than the Cu MCHS.

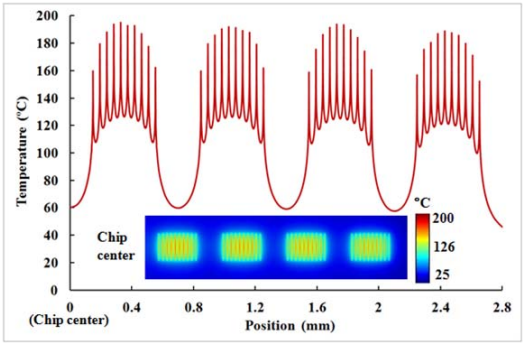

Fig. 9. Simulation results of temperature profile in longitudinal direction across 4 transistors and temperature distribution for 3.9W/mm power density.

With the hybrid heat sink, by increasing the pumping power to 0.35W, around 5.5% more power density can be accommodated.

V. Conclusion

A package-level micro-jet based cooling solution has been successfully developed for microelectronic devices with concentrated high heat flux. The Si Chip, diamond heat spreader and hybrid Si heat sink are bonded together through TCB process. The experiments have been conducted on the customized thermal test chip of 8 tiny hotspots. Large heat transfer coefficient is achieved with low pumping power. The hotspot cooling capability of 10kW/cm^2 was demonstrated and validated. The gates model simulations have been performed to evaluate the heat removal for GaN transistors. The heating power of 3.9W/mm can be dissipated, while keeping the peak gate temperature under 200°C. The developed package-level hotspot cooling solution shows promise in improving the performances of high power microelectronic devices.

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