A 99.8-dB SNDR 10kHz-BW Second-Order DT Delta-Sigma Modulator with Single OTA and Enhanced Noise-Coupling

Jiaju Lu[1,2*], Siqi Zhang[1,2*], Wang Ling Goh[1], Yuan Gao[2]
[1]School of Electrical and Electronic Engineering, Nanyang Technological University (NTU), Singapore
[2]Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR), Singapore
* Equal Contribution Authors, Email: lu0001ju@e.ntu.edu.sg, szhang054@e.ntu.edu.sg, gaoy@ime.a-star.edu.sg

***Abstract*—This paper presents a low-power second-order discrete-time (DT) Delta-Sigma Modulator (DSM) for Internet of Things (IoT) applications. The conventional noise coupling (NC) topology is improved with additional dual feedback paths to suppress the high-frequency gain of the noise transfer function (NTF), thereby reducing the internal voltage swing and relaxing the requirement of the quantizer resolution. In addition, stage-sharing technique is applied to reuse the OTA for both the integrator and the NC adder. Hence, second-order noise shaping is achieved with a single OTA. Implemented in a 130nm CMOS process, the proposed design demonstrated a simulated SNDR of 99.8dB in a 10kHz bandwidth with a 5.12MS/s sampling rate, consuming 200µW. State-of-the-art Schreier FoM (SNDR) and Walden FoM of 176.8dB and 125fJ/conv-step are achieved.**

Keywords— Delta-sigma modulator, discrete-time, stage-sharing, noise-coupling, high-resolution, second-order.

I. Introduction

Low-power Delta-Sigma ADC with a wide dynamic range has attracted significant research interests in recent years due to its wide applications in various kinds of Internet of Things (IoT) sensors. One of the key design parameters of the Delta-Sigma ADC is the order of the loop filter in the Delta-Sigma Modulator (DSM), which is the core of the whole ADC. First-order filter, though simple to implement, has difficulty achieving high resolution (>16 bits), due to its limited noise-shaping ability. High-order filters (above third order), however, are subject to instability and limited maximum input amplitude [1-4]. Hence, second/third-order filter is a favorable choice for practical applications because of its decent noise-shaping performance and good robustness.

Noise-coupling (NC) is one of the commonly adopted DSM topologies [5]. As shown in Fig. 1, by injecting the shaped quantization noise back into the loop filter, the system noise-shaping performance can be increased by one order. Different from the other topologies such as cascade integrated feedforward (CIFF) and cascade integrated feedback (CIFB), the NC structure has an inherent low-distortion feed-forward path without the need for an extra adder before the quantizer. This path makes the quantization noise the only component to be processed by the loop filter, hence relaxing the circuit linearity requirement. In addition, the feedback of the quantization noise also acts as a dither signal for the quantizer [6]. The idle tones and harmonics are therefore suppressed. However, to ensure the internal signal swing and the stability of the modulator, a multi-bit quantizer is inevitable for a traditional second-order NC topology [5]. To maintain overall system linearity, additional circuit blocks such as multi-bit digital-to-analog converter (DAC) and its associated dynamic element matching (DEM) circuits are required, leading to considerable area and power overhead [7]. Furthermore, traditional second-order loop involves at least two operational transconductance amplifiers (OTA). OTA usually consumes high power, and hence accounts for the major portion of the DSM power consumption [8-10]. Although passive devices such as capacitor arrays can also realize the function of summation and integration, the voltage signals will be attenuated and distorted due to parasitic capacitors and mismatches [5]. Hence, the design of a low-power high linearity NC-DSM remains a great challenge.

This work was supported by the Agency for Science, Technology and Research (A*STAR), Singapore under the Nanosystems at the Edge programme, grant No. A18A1b0055.

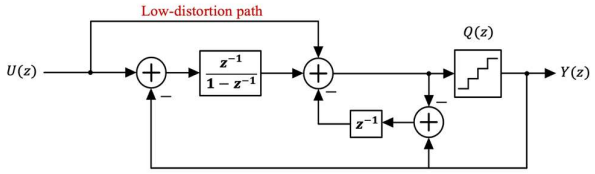


Fig. 1. Traditional NC-DSM structure with low-distortion feedforward path.

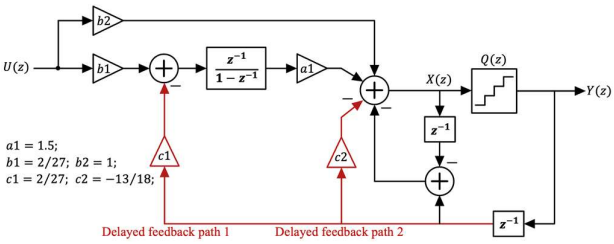


Fig. 2. Proposed NC-DSM structure.

In this paper, a novel second-order NC-DSM is presented to address the challenges listed above. An improved NC structure with dual feedback paths is proposed to suppress the high-frequency gain of the noise transfer function (NTF). Secondly, as the OTA in the switched capacitor (SC) circuit only functions in half of the clock cycle, stage sharing is applied to reuse the OTA for both the integrator and the NC adder. Only one OTA and a 1-bit quantizer are used in this circuit, which reduces both circuit complexity and power consumption. Simulation results show that the proposed design achieved 99.8dB SNDR and 10kHz bandwidth (BW) with 200µW power consumption. The rest of this paper is arranged as follows. The DSM architecture is introduced in Section II. Section III discusses the circuit implementation. The chip layout and simulation results are shown in Section IV. Finally, Section V concludes this paper.

II. DSM Architecture

The proposed NC-DSM with dual delayed feedback paths is illustrated in Fig. 2. The two paths highlighted in red are added to adjust the pole positions of the NTF. The delayed feedback path 2 serves as a fast loop for coarse error sensing and adjusts the quantization promptly in the next clock cycle. This fast adjustment, although crude, contributes to a better stability of the system. Path 1, on the other hand, has a slower response but a high DC gain because of the integrator in the loop. This path controls the in-band NTF magnitude and thus largely determines the steady-state accuracy of the DSM.

The NTF of a conventional second-order NC-DSM is

$$NTF_1 = (1 - z^{-1})^2 \tag{1}$$

After adding the dual feedback paths, the new NTF becomes:

$$NTF_2 = \frac{(1 - z^{-1})^2}{1 - (c_2 - 1)z^{-1} + (a_1 c_1 - c_2)z^{-2}} \tag{2}$$

After determining the oversampling ratio (OSR), loop order, and quantizer resolution, the NTF can be calculated using MATLAB SDToolbox. Coefficient optimization is required for the convenience of circuit implementation. Dynamic-range scaling is also adopted in this architecture. Scaling is realized through coefficient a1 in Fig. 2, by adjusting the capacitance ratio in the switched-capacitor (SC) circuit. By setting a1 to 1.5 and adjusting b1 and c1 accordingly, the output voltage of the first stage is scaled down by 1/3 without affecting the transfer function. The scaled signal alleviates the saturation issue of the OTA-based integrator and improves the linearity and stability of the system. The final coefficients selected for this design are listed in Fig. 2, and the corresponding NTF is:

$$NTF_2 = \frac{(1 - z^{-1})^2}{1 - \frac{31}{18}z^{-1} + \frac{15}{18}z^{-2}} \tag{3}$$

Fig. 3 shows the comparison of the magnitude response of the conventional NTF (NTF1) and the improved NTF (NTF2). An effective NTF for a DSM should have a low in-band gain to perform the noise-shaping and thus achieve a high signal-to-noise ratio in the bandwidth of interest. However, the out-of-band noise gain is raised by the NTF as a consequence. In fact, while the in-band quantization noise power is suppressed, the total quantization noise power across the spectrum is increased after being processed by the loop filter. Although the high-frequency noise can be removed by the subsequent decimation filter after the quantizer and will not appear in the final digital output, this part of noise is still noteworthy as it is amplified and circulates inside the loop filter. Consequently, even a small input scale can induce a large voltage swing in the loop filter, saturating the quantizer and leading to non-linearity and instability of the system. The common approach to improve this is to raise the resolution of the quantizer to directly compress the quantization noise. In this work, however, by adjusting the pole positions of the NTF, a conceptual low-pass filter surfaced whereby the NTF is multiplied with a low-pass transfer function [11]. In this way, the NTF poles move away from zero, and its high-frequency gain will be suppressed. The traditional second-order NTF's quantization noise power is defined as [12]:

$$\frac{\Delta^2}{12\pi}\int_0^{\pi} \left|NTF_1(e^{j\omega})\right|^2 d\omega = 6\pi\frac{\Delta^2}{12\pi} \tag{4}$$

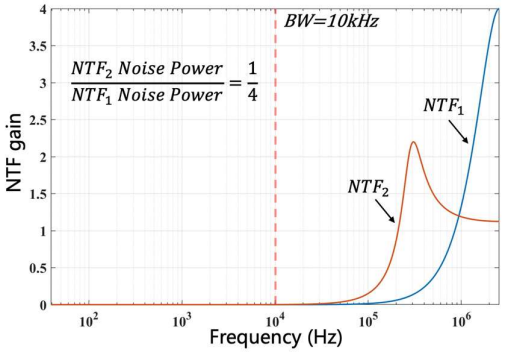


Fig. 3. Comparison of magnitude response of the conventional NTF (NTF1) and improved NTF (NTF2).

where Δ represents the spacing between two adjacent output levels of the quantizer. In this equation, the quantization noise is assumed as white noise with a spectral density of $\Delta^2/12\pi$. After the pole control, the new NTF's quantization noise power is defined as:

$$\frac{\Delta^2}{12\pi}\int_0^{\pi} \left|NTF_2(e^{j\omega})\right|^2 d\omega = 1.5\pi\frac{\Delta^2}{12\pi} \tag{5}$$

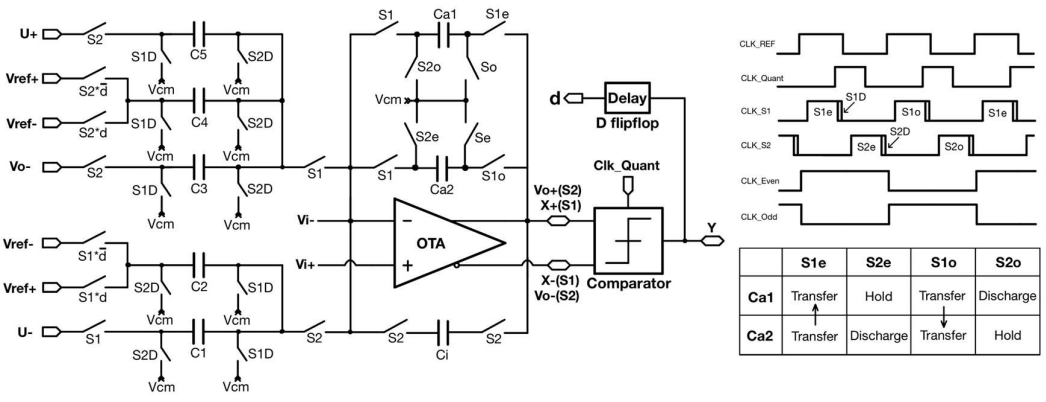
It can be observed that the noise power is reduced by 75%. In the actual circuit, this noise power reduction is translated to a much lower internal voltage swing. Tested with 546.875Hz, -2.9dBFS input in Simulink, the peak voltage before the quantizer is reduced from 5.5V to 0.54V. Hence, the requirement for the quantizer is lowered and the stability and linearity of the system are improved. Another advantage of the delayed feedback paths is the relaxed settling time for the quantizer. The conventional feedback paths require the quantizer to settle within half clock cycle so as to leave sufficient charging time for the input stage. In contrast, the delayed dual feedback paths allow a whole clock cycle for the quantizer to settle, which eases the speed requirement for the quantizer design.

III. Circuit Implementation

A. SC Circuit

A simplified SC circuit with the corresponding timing diagram is shown in Fig. 4. Only half of the fully differential circuit is drawn for the convenience of illustration. Note that the analog-domain delayed feedback path is realized by capacitors Ca1 and Ca2; whereas the digital-domain delayed feedback paths are implemented with a D flip-flop. Two digital paths, namely, the traditional NC noise feedback path and the newly added delayed feedback path $c2$ in Fig. 4 can be implemented by a single capacitor C4.

The stage-sharing technique is applied by feeding the output of the first-stage integrator back to the input of the adder and reusing the opamp in the next clock phase. Hence, a second-order loop filter can be realized with only one opamp. The operation of this circuit consists of four clock phases, S1e, S2e, S1o, and S2o, for even and odd clock cycles, respectively. The even and odd clocks are generated by a frequency divider. The detailed operation of the four clock phases is explained as follows. In phase S1e, the sampling capacitors (C1 and C2) of the integrator sense the input and the feedback signal, while the sampling capacitors of the adder (C3, C4, C5) and the addition capacitor Ca2 transfer their



	S1e	S2e	S1o	S2o
Ca1	Transfer	Hold	Transfer	Discharge
Ca2	Transfer	Discharge	Transfer	Hold

Fig. 4. Simplified SC circuit of the proposed structure.

changes to Ca1. Note that Ca2 stores the previous addition result and serves as the analog-domain feedback path of the NC loop in Fig. 4. In phase S2e, C1 and C2 transfer charges to the integration capacitor Ci. C3, C4, and C5 sample the first stage output, feedback signal, and input signal, respectively. Ca1 holds the previous addition result in phase S1e. Ca2 discharges itself. In the odd clock cycles S1o and S2o, the integrator's operation is the same as in S1e and S2e. The adder also works similarly except that the addition capacitors Ca1 and Ca2 alternate their roles.

The polarity inversion is accomplished by feeding the first-stage integrator with the opposite differential signals, including both the input signal and the feedback DAC signal, and connecting the first-stage differential output oppositely to the second stage, as shown in Fig. 4. The second stage sees the same signal as without this technique thus preserving the functionality of the overall loop filter. By inverting the polarity of the integrator, however, the opamp's differential output follows the same polarity across adjacent clocks, namely S1 and S2 most of the time. This technique reduces the short-term voltage swing of the opamp, relaxing the design requirements such as slew rate and bandwidth when compared to other stage-sharing designs [13].

B. OTA & CMFB

Fig. 5 shows the schematic of cross-coupled two-stage OTA for the SC circuit. To avoid the mismatch-induced instability, the size of M3 (M6) and M4 (M5) should be different. The first-stage output impedance is determined by the transconductance of the cross-coupled pairs. The gain of the first stage is written as:

$$A_v \approx -\frac{g_{m_{1,2}}}{g_{m_{3,6}} - g_{m_{4,5}}} \tag{6}$$

Although the gain is smaller than the traditional OTA structures used in DSM such as folded-cascode and telescopic, the cross-coupled structure has several advantages. It is more energy-efficient, in addition, it also offers a larger output headroom without transistor stacking, which allows low-voltage operation with improved linearity.

A specially designed SC common mode feedback circuit (SC-CMFB) is also adopted, as shown in Fig. 5 [14]. The conventional SC-CMFB circuit samples the common mode voltage at one clock phase and adjusts the common mode voltage of the OTA at the other. However, the intermittent feedback signal and the unsymmetric capacitor loading make

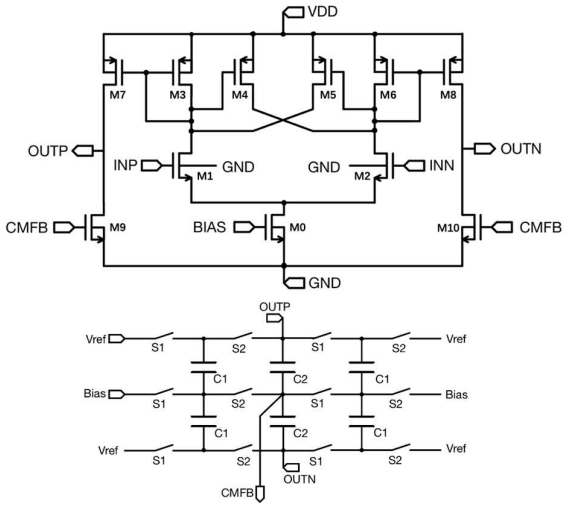


Fig. 5. Schematic of cross-coupled OTA and SC CMFB with symmetrical loading.

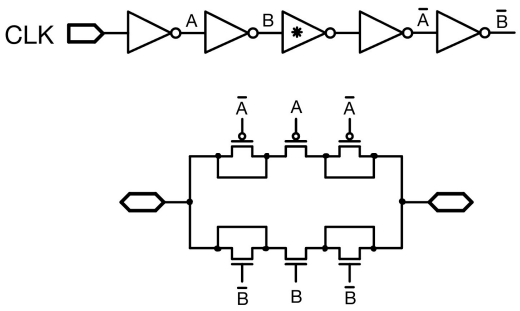


Fig. 6. TG switch with half-sized dummy transistors and extra delay.

the traditional structure insufficient for a stage-sharing circuit. The SC-CMFB in this work can provide a CMFB voltage and an equal capacitance load in both S1 and S2, by operating alternately through the left and right sides, thus offering a more stable common mode voltage.

C. Switch

All switches shown in Fig. 4 are based on transmission gates (TG) with dummy transistors to alleviate the channel charge injection [14]. As illustrated in Fig. 6, the TG transistor pair is enclosed by two dummy transistors with opposite clock phases. The inverter marked by an asterisk is for extra delay. This element guarantees that the dummies turn on later for

TABLE I. COMPARISON OF PERFORMANCE

	This work*	TCAS'22 [15]*	JSSC'16 [9]	JSSC'19 [16]	JSSC'20 [17]	TCAS'16 [18]	ISCAS'19 [19]*	ISCAS'23 [20]*
Number of Order	**2**	4	3	4	2	2	2	3
Process (nm)	**130**	28	65	65	65	180	180	55
Supply Voltage (V)	**1.2**	1.8	1	1.2	0.8	1.8	5/1.8	1.2
Fs (MHz)	**5.12**	1	6.4	10.24	3.072	20	2	5
BW (kHz)	**10**	15.625	25	20	24	156.25	1.93	50
Power (μW)	**200**	255	800	550	49	29.5	820	363.8
ENOB (bits)	**16.29**	15.85	15.52	16.45	14.6	9.3	14.89	15.42
SNDR (dB)	**99.82**	97.2	95.2	100.8	89.6	57.7	91.4	94.6
FoM_w (pJ/conv)	**0.125**	0.138	0.34	0.153	0.041	0.151	6.99	0.083
FoM_{SNDR} (dB)	**176.8**	175.1	170.1	176.4	176.5	155	155	176

*Simulation result. $FoM_w = Power/(2 \cdot BW \cdot 2^{ENOB})$; $FoM_{SNDR} = SNDR + 10log_{10}(BW/Power)$

effective charge cancellation. Since the channel charge is proportional to the transistor area, the two dummy transistors around can absorb the channel charge after the main transistors are turned off, assuming equal charge splitting to the source and drain. This assumption is generally valid if the environment seen by the two sides of the switch is similar, or if the clock's edge is very sharp. The series inverter is included in every switch to ensure fast clock switching.

IV. SIMULATION RESULT

The proposed DSM was implemented in a standard 130nm CMOS process. The chip layout is shown in Fig. 7, circuit block were arranged symmetrically to minimize mismatch. The active circuit occupies a chip area of 1mm × 1.2mm. The sampling clock frequency is 5.12MHz and the bandwidth is 10kHz. As shown in Fig. 8, SNDR of 99.8dB was achieved when the input frequency is 546.875Hz with an amplitude of -2.9dBFS. The PSD shows a high SFDR of 105.1dB, which indicates outstanding linearity performance.

Fig. 9 shows the power breakdown of key building blocks. The overall circuit power consumption is about 200μW. Among all components, the OTA consumes 70% of the total power, which also confirm the importance to save one OTA using the stage-sharing technique. The circuit performance is summarized and compared with the other recently reported designs in Table. I. This design presents an FoM_{SNDR} of 176.8dB, and an FoM_w of 125fJ/conv, which shows this design achieves competitive performance without high-order loop filter. The modified NTF transfer function also enables this design to achieve superior SNDR compared to other second-order DSM designs.

V. CONCLUSION

A 16-bit single-OTA second-order DSM has been demonstrated in 130nm CMOS technology. With a bandwidth of 10kHz, this design consumes 200μW under 1.2V supply. The proposed NC structure combines a low-distortion feedforward path and dual delayed feedback paths to suppress the high-frequency gain of the NTF. This new architecture significantly reduces the signal swing and improves the linearity of the system, relaxing the resolution requirement for the quantizer. Moreover, the stage-sharing technique is implemented to reduce the number of OTAs, thereby saving power. In addition, the SC circuit, CMFB, and switches are specially designed to meet the high resolution and stage-sharing structure. The simulation returns a peak SNDR of 99.82dB and an SNR of 101.2dB for a -2.9dBFS input at 546.875Hz. The design achieved state-of-the-art FoM 176.8dB (FoM_{SNDR}) and 125fJ/conv (FoM_w).

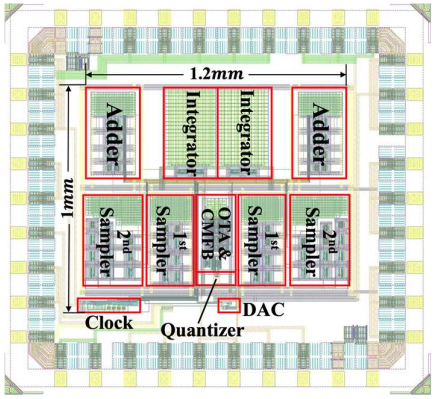


Fig. 7. The NC-DSM chip layout.

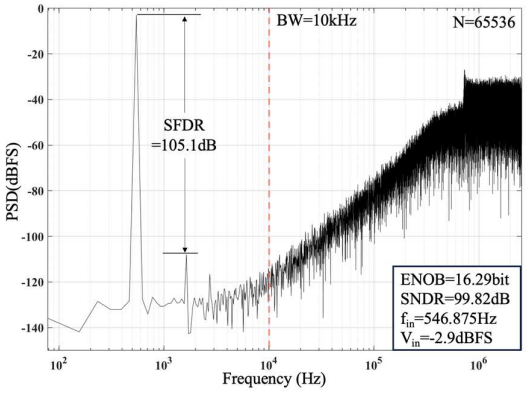


Fig. 8. Simulated NC-DSM output spectrum.

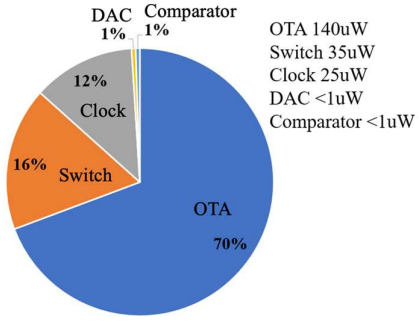


Fig. 9. Power breakdown of the proposed second-order NC-DSM.

REFERENCES

[1] K. Y. Leung, E. J. Swanson, Kafai Leung, and S. S. Zhu, "A 5 V, 118 dB ΣΔ Analog-to-Digital Converter for Wideband Digital Audio," in *Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 1997, pp. 218–219.

[2] YuQing Yang, A. Chokhawala, M. Alexander, J. Melanson, and D. Hester, "A 114 dB 68 mW Chopper-Stabilized Stereo Multi-Bit Audio A/D Converter," in *Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 2003, pp. 56–477.

[3] Z. Yang, L. Yao, and Y. Lian, "A 0.7-V 100-µW Audio Delta-Sigma Modulator with 92-dB DR in 0.13-µm CMOS," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2011, pp. 2011–2014.

[4] T. Christen, "A 15bit 140µW Scalable-Bandwidth Inverter-Based Audio ΔΣ Modulator with >78dB PSRR," in *Proceedings of the European Solid-State Circuits Conference (ESSCIRC)*, Sep. 2012, pp. 209–212.

[5] K. Lee, M. R. Miller and G. C. Temes, "An 8.1 mW, 82 dB Delta-Sigma ADC With 1.9 MHz BW and − 98 dB THD," *IEEE J. of Solid-State Circuits*, vol. 44, no. 8, pp. 2202-2211, Aug. 2009.

[6] H. Wang and G. C. Temes, "A Low-Distortion Power-Efficient Feedforward Technique for DT Delta-Sigma ADCs," *2023 IEEE International Symposium on Circuits and Systems (ISCAS)*, Monterey, CA, USA, 2023, pp. 1-4.

[7] W. Zhao et al., "A 0.025-mm2 0.8-V 78.5-dB SNDR VCO-Based Sensor Readout Circuit in a Hybrid PLL-ΔΣM Structure," *IEEE J. of Solid-State Circuits*, vol. 55, no. 3, pp. 666-679, Mar. 2020.

[8] R. Theertham, S. N. Ganta and S. Pavan, "Design of High-Resolution Continuous-Time Delta–Sigma Data Converters With Dual Return-to-Open DACs," *IEEE J. of Solid-State Circuits*, vol. 57, no. 11, pp. 3418-3428, Nov. 2022.

[9] Y. H. Leow, H. Tang, Z. C. Sun and L. Siek, "A 1 V 103 dB 3rd-Order Audio Continuous-Time ΔΣ ADC With Enhanced Noise Shaping in 65 nm CMOS," *IEEE J. of Solid-State Circuits*, vol. 51, no. 11, pp. 2625-2638, Nov. 2016.

[10] A. Suanes, L. Terés, M. Dei and F. Serra-Graells, "A 0.8mW 50kHz 94.6dB-SNDR Bootstrapping-Free SC Delta-Sigma Modulator ADC with Flicker Noise Cancellation," *2021 IEEE International Symposium on Circuits and Systems (ISCAS)*, Daegu, Korea, 2021, pp. 1-5.

[11] Shanthi Pavan; Richard Schreier; Gabor C. Temes, "High-Order Delta-Sigma Modulators," in Understanding Delta-Sigma Data Converters , *IEEE*, 2017, pp.83-116.

[12] Shanthi Pavan; Richard Schreier; Gabor C. Temes, "Sampling, Oversampling, and Noise-Shaping," in Understanding Delta-Sigma Data Converters , *IEEE*, 2017, pp.27-61.

[13] K. Lee, M. R. Miller and G. C. Temes, "An 8.1 mW, 82 dB delta-sigma ADC with 1.9 MHz BW and −98 dB THD," *2008 IEEE Custom Integrated Circuits Conference*, San Jose, CA, USA, 2008, pp. 93-96.

[14] O. Choksi and L. R. Carley, "Analysis of switched-capacitor common-mode feedback circuit," *IEEE Trans on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 50, no. 12, pp. 906-917, Dec. 2003.

[15] K. E. Lozada et al., "A 4th-Order Continuous-Time Delta-Sigma Modulator With Hybrid Noise-Coupling," *IEEE Trans. on Circuits and Systems II: Express Briefs*, vol. 69, no. 9, pp. 3635-3639, Sept. 2022.

[16] B. Wang, S. -W. Sin, S. -P. U., F. Maloberti and R. P. Martins, "A 550-µW 20-kHz BW 100.8-dB SNDR Linear-Exponential Multi-Bit Incremental ΣΔ ADC With 256 Clock Cycles in 65-nm CMOS," *IEEE J. of Solid-State Circuits*, vol. 54, no. 4, pp. 1161-1172, Apr. 2019.

[17] S. Ma, L. Liu, T. Fang, J. Liu and N. Wu, "A Discrete-Time Audio ΔΣ Modulator Using Dynamic Amplifier With Speed Enhancement and Flicker Noise Reduction Techniques," *IEEE J. of Solid-State Circuits*, vol. 55, no. 2, pp. 333-343, Feb. 2020.

[18] I. Lee, B. Kim and B. -G. Lee, "A Low-Power Incremental Delta–Sigma ADC for CMOS Image Sensors," *IEEE Trans. on Circuits and Systems II: Express Briefs*, vol. 63, no. 4, pp. 371-375.

[19] G. Chen, Y. You, W. Lu, X. Shi, Z. Chen and Y. Zhang, "A 16-bit 64-channel 2-order Incremental Σ-Δ ADC with On-Chip Decimator for X-ray Detections," *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, Sapporo, Japan, 2019, pp. 1-5.

[20] X. Hao, J. Chen, L. Meng, M. Zhao and Z. Tan, "A 94.6dB-SNDR 50kHz-BW 1-1-1 MASH ADC Using OTA-FIA Based Integrators," *2023 IEEE International Symposium on Circuits and Systems (ISCAS)*, Monterey, CA, USA, 2023, pp. 1-4.