# Low Cost Grounding Integration for Surface Ion Trap


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***Abstract*—Si substrate provide the integration platform for surface ion trap device fabrication. Grounding metal for the surface ion trap is necessary because of high RF voltage (>100V) applied and lower RF loss required within functionality. High resistivity Si substrate with floating metal grounding and low-grade Si substrate with connected grounding metal were integrated with surface ion trap. Ion trap resonance curves were observed at 47.1 MHz frequency for ion trap devices with different grounding metal. The curves have similar resonant power.**



***Keywords—Surface Ion trap device, Ground metal landed on low-grade Si substrate.***


## I. Introduction

Quantum computing becomes hot topic since IBM promoting quantum computing via cloud at 2016 [1]. There are different types of qubit [2], such as, superconducting loops, Trapped ion, silicon quantum dots, and topological qubits and diamond vacancies. G. Popkin summarized the pros and cons of each type of qubits in [2]. Trapped ion is stable with longevity. The lasers were used to cool and tune the ion [2]. Trapped ion attracted more attention due to exquisite and high efficiency. Trapped ions are used in quantum information system as communication qubit and memory qubits [3]. The outstanding challenge is the scaling of trapped ions to thousands of qubits and laser control of qubits [3]. Semiconductor foundry provided platform on the scaling of ion trap device and integrated photonic device for qubit functionality. R. J. Niffenegger et.al [4] demonstrated the integration of surface ion trap with six wavelengths of grating couplers and waveguides. These grating couplers were used for photoionization, pre-cooling, Doppler cooling and detection, re-pumping, etc. Integrated photonic beam profiles were measured by microscope, all the different wavelengths beams were focus on trapped ion area. This demonstration open the door for multiple trapped-ions quantum application, such as, quantum sensors and optical clocks [5]

To clear the top surface of ion trap, the electrical connection was designed and integrated through TSV [6]. The surface ion trap fabrication process was setup and improved in CMOS-compatible line [7]. Oxide-first-metal-last approach was developed for surface ion trap fabrication [7]. The metal electrodes confined $^{88}$Sr+ on the Si chip with integrated TSV reported in [6]. High resistivity Si substrate was used within surface ion trap fabrication in [6]. To reduce RF loss on the substrate, high resistivity Si substrate is one of obvious choice for ion-trap chip. The cost of 300mm high resistivity Si substrate is high. To reduce the cost of substrate, grounding metal was integrated within surface ion trap fabrication.

Grounding metal was inserted between ion trap device and Si substrate. Seokjun Hong et.al had been designed and fabricated grounding metal on top of Si substrate [8]. To increase ion-trap device performance, there is thicker oxide deposited for the top metal plane. The thicker oxide induce the higher stress. There is still 1μm oxide was deposited under grounding metal in [8]. To achieve the higher separation of grounding and top metal plate, R. C. Sterling et.al. used SOI ( 30μm Si/10μm $SiO_2$/600μm Si)[9]. The SOI is another high cost substrate because of complicated fabrication approach. The grounding metal was built at 600μm Si substrate after top 30μm Si and 10μm $SiO_2$ removal in [9].

We will report two types of grounding metal integration for the surface ion trap, follow by assembly of surface ion trap. The fabricated grounding metal was characterized by the inspection and cross-section. To shorten the functionally test, RF resonator test was setup. The resonator test for both types of ion trap devices was conducted. The resonate performance of both devices were reported. The costs of ion trap devices with conventional grounding and low cost grounding metal were compared in this paper.

## II. EXPERIMENT

### A. Conventional ion trap fabrication

One type of grounding metal was fabricated by single damascene process on high resistivity Si substrate. There is thin dielectric between grounding metal and high resistivity Si substrate. The fabrication process flow is shown in Fig.1.

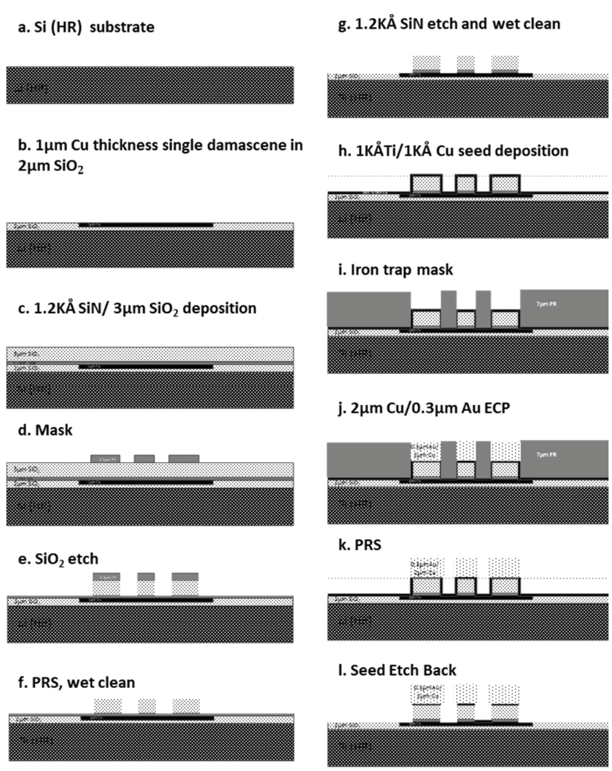


Fig.1 The conventional grounding fabrication major process flow.

2µm $SiO_2$ dielectric film was deposited on the high resistivity Si substrate. Grounding pattern was masked on top of the $SiO_2$ film. 1µm $SiO_2$ trench was etched by the plasma etcher, wet clean was followed for the polymer removal after dielectric etching and photoresist stripping. PVD and ECP were processed for the filling of grounding metal trench. Cu CMP flatted the grounding metal surface and formatted grounding metal that is shown in Fig.1b. 1KÅ SiN capping layer and 3µm $SiO_2$ films were deposited on top of grounding metal in fig.1c. Oxide dielectric was masked by the photoresist (fig.1d). Dry etching removed oxide for the trench of ion trap (fig.1e). 1KÅ SiN capping layer was opened after PRS and wet clean (fig.1f and 1g). 1KÅ Ti barrier/1KÅ Cu seed was sputter deposited for the metal plate ECP in fig.1h. ~3µm Cu /0.3µm Au metal films were electroplated after $O_2$ descum (fig.1i, fig.1j). Top metal electrodes were separated after photoresist strip and Cu/ Ti barrier /seed global wet etch (fig.1k, 1l). Ion trap device with conventional grounding layer was formed in fig.1i. 5µm $SiO_2$ was involved within grounding and surface ion-trap fabrication. High resistively Si substrate was used for the surface ion trap.

### B. Ion trap device with connected metal ground

This paper reduced the $SiO_2$ thickness from 5µm to 4µm and changed the high resistivity Si substrate to low-grade Si substrate. The major process flow is shown in Fig.2.

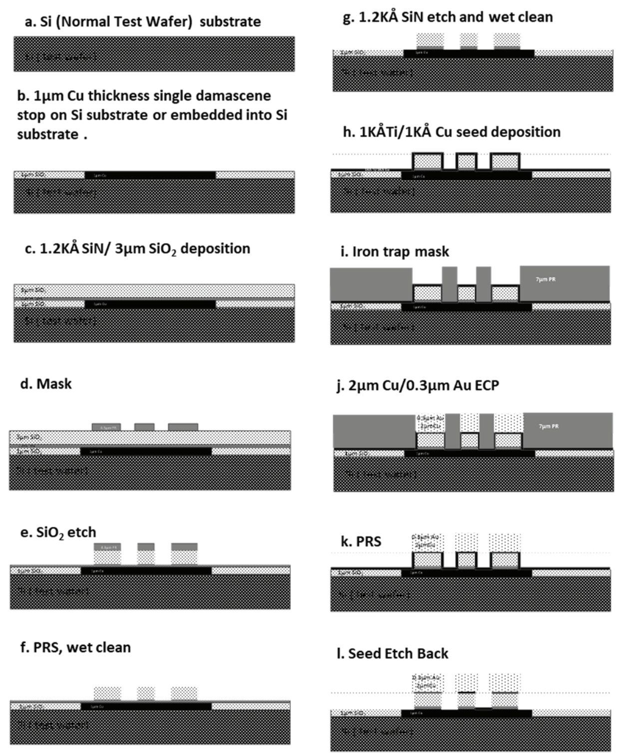


Fig.2 Ion trap with new grounding fabrication flow.

1µm $SiO_2$ was deposited on the low-grade Si substrate. Grounding pattern was masked on $SiO_2$ film by the photoresist. 1µm $SiO_2$ were dry etched and stopped on low-grade Si substrate after grounding lithography. PVD and ECP were processed after PRS and wet clean, followed by Cu annealing and Cu CMP. Single damascene grounding metal was formed and landed on low-grade Si substrate that is shown in fig.2b. 1KÅ SiN capping layer and 3µm $SiO_2$ were deposited on top of grounding metal in fig.2c. Oxide was patterned by the photoresist (fig.2d). Dry etching process was used to remove the trench oxide of ion trap device (fig.2e). 1KÅ SiN capping layer was opened by global dry etch after PRS (fig.2f) and wet clean (fig.2g). 1KÅ Ti barrier/1KÅ Cu seed was sputter deposited after $Ar^+$ plasma clean (fig.2h). Photoresist was used to mask electrode plate on top of Cu seed for metal electrode ECP in fig.2i. 3µm Cu /0.3µm Au was electroplated after $O_2$

descum (fig.2j). Top metal electrodes were separated after photoresist strip (fig.2k) and Cu/ Ti barrier /seed global wet etch in fig.2l.

Ion trap device with connected grounding metal was formed in fig.2l. Low-grade Si substrate replaced high resistivity wafer. Dielectric thickness was reduced from 5um to 4um. To reduce dielectric thickness, grounding metal can be integrated in low-grade Si substrate.

### *C. Assembly process for the ion trap*

The fabricated wafer with ion trap device was diced according to the design (8mmX 8mm). ~15-20um spaces between dicing line to device edge along x and y direction are

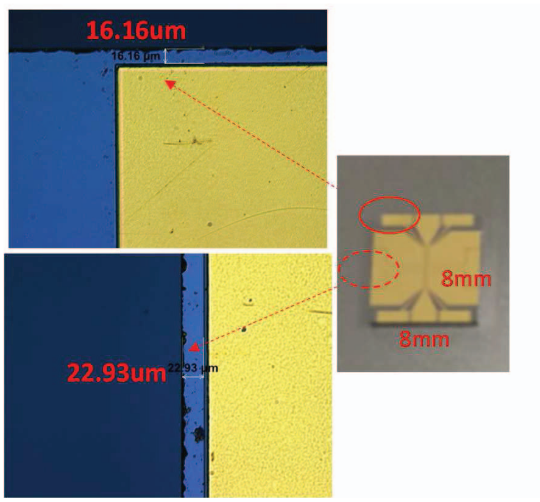

Fig.3. The diced ion trap device.

shown in fig.3.

To increase device height in the CPGA cavity after assembly, glass spacer was applied and diced same size. No conductive pasted was put on top of glass spacer. Tresky T8000 was used for the die attachment with force.

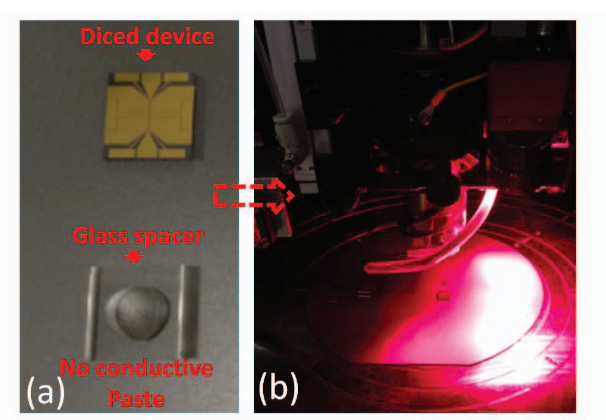

Fig.4. Device to glass space attachment by Tresky

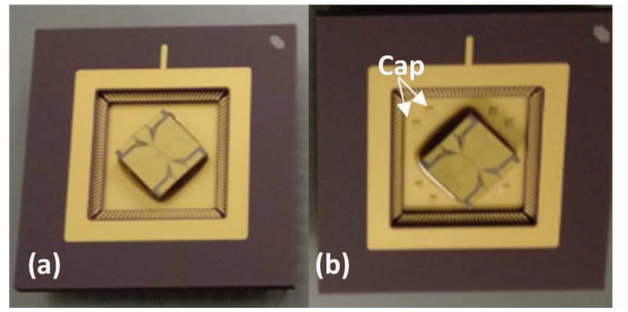

Fig.5 (a). Stacked chip assembled on CPGA. (b). flat capacitor was attacked on CPGA

The stacked chips was attached to CPGA substrate by Tresky along 45 degree. The stacking degree and wire bonding direction were designed to keep top electrode space for the subsequence laser travel within functionally testing. The stacked CPGA is shown in fig. 5a. The capacitors were required for the ion trap RF testing. The capacitors were manually attached on the CPGA through the conductive paste that is shown in Fig. 5b. The surface electrode plate was bonding to CPGA through the Au wire. The final inspection of ion trap package is shown in fig.6. The top electrode connected to the capacitors and CPGA pads by the Au wire. The electrical connection for the test went through the bottom pins. The resonator test was conducted after CPGA assembly.

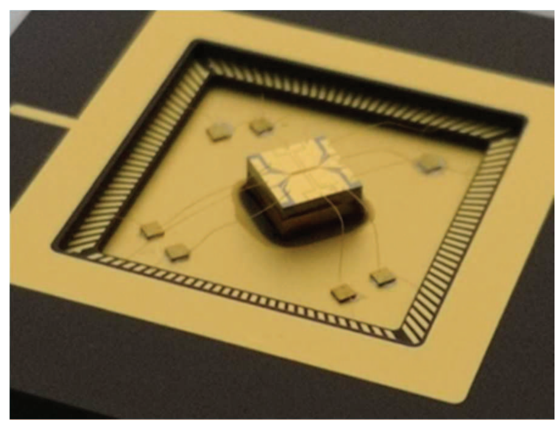
Fig. 6. The optical inspection of ion trap chip after assembly.

## III. RESULTS AND DISCUSSIONS

### *A. Fabricated grounding metal*

The optical inspection and cross-section of ion trap with grounding metal fabricated by the convention approach was reported in fig.7.

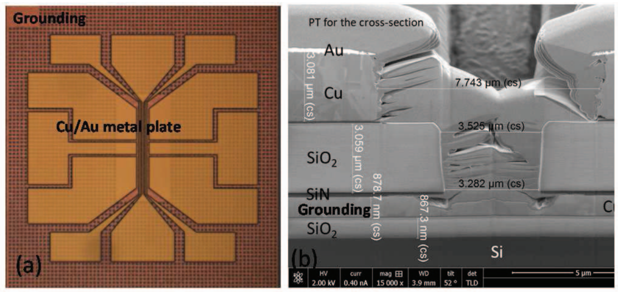


Fig.7. The optical inspection result of ion trap fabricated by conventional approach (a). The cross-section of ion trap electrode and grounding metal (b).

The bigger grounding pad was opened in Fig. 7a. The grounding pad was connected to CPGA through Au wire. To reduce device stress, square dielectric slot was designed and built under big metal grounding in fig.7a. The cross-section of ion trap with conventional ground is shown in Fig.7b. There is around 1µm $SiO_2$ under grounding metal. Cu grounding metal have undercut because of 3µm $SiO_2$ insulation layer dry etch and seed layer etch back in fig.7b.

The low cost grounding metal is shown in Fig.8a. The grounding metal was exposed within 3µm $SiO_2$ etch back in fig. 8a. 1µm Cu grounding metal was built on top of low-grade Si substrate. The cross-section of ion trap with this new grounding metal is shown in fig.8b. The grounding metal was landing on low-grade Si substrate with Ti barrier layer. Ground metal can be fabricated in low-grade Si substrate in the future.

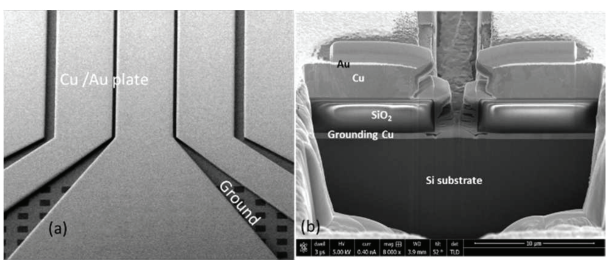


Fig.8. The SEM inspection result of ion trap (a). The cross-section review of ion trap with disclosed grounding (b).

Both types of grounding metal have similar process cost, but substrate have great different on the cost. If both structures perform same functionality, new grounding process effective reduced substrate cost.

Ion trap devices with same design and different grounding metal were assembled on the CPGA substrate for RF resonator testing.

*B. RF resonator test and results*

Surface ion trap performance testing is very long process because of high vacuum required and multiple laser setup. To reduce the testing time, RF resonator test is was setup and shown in Fig. 9.

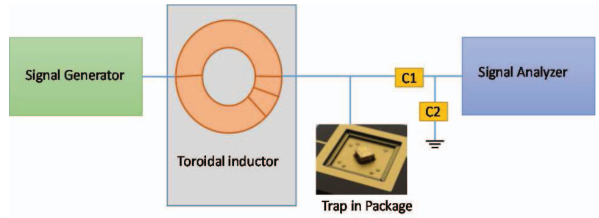


Fig.9. The basic test setup of RF resonator test with resonator test with ion trap.

Trap device was connected (as capacitor) through bottom pins to external inductor to form LCR resonate circuit. -10dBM RF power was supplied by signal generator in Fig.9. A set of capacitor dividers C1 and C2 (with C1: C2=1:20) is connected to the inductor and signal analyzer for suppressed power readout. Signal analyzer receive the resonance curve when liner frequency sweep from 10 to 100 MHz with 1MHz step. Ion trap devices with two types of grounding were characterized and reported in Fig.10.

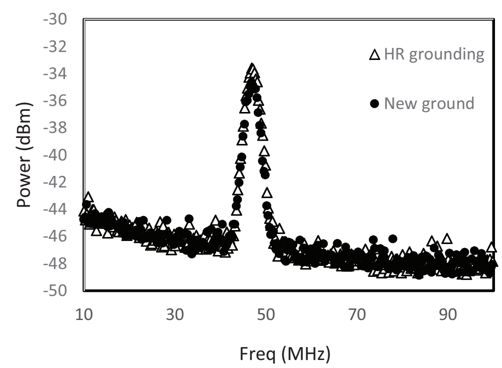


Fig. 10. Resonance curve of ion traps with conventional and new grounding system.

Ion trap with the connected grounding on low-grade Si substrate have same resonant frequency with conventional grounding metal floating on high resistivity substrate. Resonant frequency of both device is 47.1MHz, but resonant power of ion trap device with low coat grounding metal is ~ 3% lower than conventional grounding. The lower resonant power is within process variation.

Both structures performed the similar resonance, but the cost of substrate is quite different. The next part will analysis the cost reduction according to the cost model.

### C. *Cost comparision of grounding metal*

Interposer cost model had been setup and reported in [10]. The cost model was used for the calculation of ion trap wafer with conventional grounding and low cost grounding. The cost per wafer was calculated according to 5K/ month wafer fabrication. Major processed flows were described in fig.1 and 2. The cost was grouped to substrate, surface electrode, grounding metal and oxide trench. The comparation results of wafer cost with two type of grounding is shown in fig. 10.

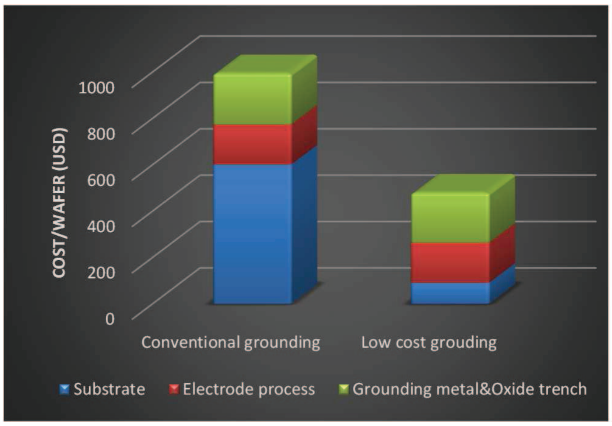


Fig.10. Cost comparison of both type of grounding

The total cost of ion trap device with new grounding reduced around half in fig.10. The major reduction from substrate cost. There is grounding process cost reduction also. Compared the grounding metal process cost, this is around 3% cost reduction for the low cost grounding process, but thinner oxide can reduce wafer warpage that reduce process challenge

**Conclusions**

Cu grounding metal was designed and fabricated on low-grade Si substrate. Compared with ion trap with grounding metal floating on $SiO_2$ dielectric film with high resistivity Si substrate, the ion trap with low-grade Si substrate has same resonant sequence at 47.1MHz and ~3% lower resonant power that is within process variation. However, new grounding metal reduced around half cost through the low-grade Si substrate and thinned dielectric film.

## ACKNOWLEDGMENT


The authors are sincerely grateful for funding support from A*STAR Quantum Technology for Engineering(A1685b0005). Authors also thank fab colleagues for the support and electrical testing from NTU during grounding process development.


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