A 2× Time-Interleaved 4-GSps 14-Bit DAC with On-Chip Calibration of Interleaving Nonlinearities

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***Abstract*—This work presents a high-linearity 2× time-interleaved (TI) current-steering (CS) digital-to-analog converter (DAC) facilitated by an on-chip calibration approach. To accurately analyze the impact of interleaving errors on high-resolution TI-DAC, a comprehensive function of spurious-free dynamic range (SFDR) is derived from time-domain modeling. Based on theoretical analysis, a foreground two-step calibration scheme with low-complexity circuits is proposed to address the issue of SFDR degeneration caused by narrowband locking. The calibration of gain error mismatch (GEM) can be achieved by efficiently compensating for current sources of each sub-DAC in the proposed GEM loop. The amplitude of the TI spurs induced by duty-cycle errors (DCE) exhibits a unimodal linear characteristic. Based on this characteristic, a compact cyclic-quantization circuit combined with a uniform grid search algorithm is proposed to realize a high-precision calibration for DCE. A 14-bit 4-GSps TI-DAC with the foreground on-chip calibration is realized in 65-nm CMOS. Measurement results demonstrate that with one single-tone calibration, the SFDR can be improved up to around 25 dB, achieving an SFDR ≥ 61dB across the entire first Nyquist zone.**

***Index Terms*—Current-steering (CS), digital-to-analog converter (DAC), high-linearity, on-chip calibration, time-interleaving (TI).**

I. INTRODUCTION

The rapid development of modern communication applications necessitates the increasing demand for high-speed, high-resolution digital-to-analog converters (DACs) [1]-[4].The DACs accurately convert digital data into analog signals suitable for transmission over complex channels. In wireless/wireline links, the DAC's role in signal generation and shaping is critical for maintaining high signal integrity, efficient bandwidth utilization, and overall system performance [5]-[8]. Among DAC architectures, the time-interleaved DAC (TI-DAC) with a current-steering (CS) design stands out as an optimal solution for extending operational bandwidth and relaxing the conversion speed requirements of each sub-DAC (sDAC) [9]-[17]. However, non-ideal factors within interleaved structures may degrade the dynamic performance of DACs, including offset mismatch (OSM), gain error mismatch (GEM), and interleaving duty cycle error (DCE) [18], [19].

Prior studies have provided theoretical analyses of nonlinear effects in single core DACs [20], [21]. A general mathematical model for TI-DACs was introduced in [22]. However, it did not provide functions describing the dependence of spurious-free-dynamic range (SFDR) on GEM and interleaving DCE. Recent advancements in interleaving nonlinearity analysis have led to the development of corresponding calibration methodologies. Theoretical analysis indicates that an interleaving spur occurs at the DC under Nyquist input [23]. According to this analysis, off-chip high-precision analog-to-digital converters (ADC) have been used to measure spurs for calibrating DCEs [17][18]. In [24], to show how timing skew creates a spur, phase error mismatch caused by timing skew was also incorporated into SFDR analysis. Moreover, timing skew and DCE were calibrated by using a phase shifter and tunable pull-up/down transistors, with error extraction performed by an external spectrum analyzer. However, GEM and DCE can cancel each other out, reducing their negative impact on SFDR, leading to a phenomenon known as narrowband locking in conventional single-tone calibration [25]. Specifically, the calibration process locks onto a single-frequency solution with non-ideal GEM and DCE, resulting in effective calibration only near the single-tone input frequency, rather than across the entire Nyquist band. To address this issue, a two-tone calibration method was proposed in [25]. While effective, this approach usually requires more calibration steps and high-performance ADCs to extract interleaving spurs. A pulsed-error pre-distortion scheme combined with quantization error cancellation was developed in [26], to correct gain and timing mismatches between DAC channels. This approach achieves notable SFDR improvement, but at the cost of using high-complexity circuits and a spectrum analyzer. Several digital calibration techniques have been proposed to mitigate interleaving errors. In [27], an enhanced error backpropagation scheme was introduced to compensate for interleaving errors using a digital feedback system incorporating an ADC and oscilloscope. Similarly, [19] and [28] proposed a pre-distortion-based calibration approach, where the parameters needed for the correction filter design are extracted using a spectrum analyzer and search algorithm.

Notably, previous research heavily relied on high-performance ADCs or external instruments for precise interleaving spur extraction, often requiring manual intervention or computer-based algorithms, which do not provide a fully on-chip solution that is compact, efficient, and cost-effective. In this work, we derive a comprehensive function of SFDR for a 2× TI-DAC based on a time-domain mathematical model. This function reveals the separate and coupled effects of input signal frequency and interleaving errors on the dynamic performance of the TI-DAC. Based on the derivations and analysis, an effective two-step calibration approach and corresponding circuits are proposed with a low area and fully on-chip implementation. This work applies the proposed calibration techniques to a 14-bit, 4-GSps TI-DAC in TSMC 65-nm CMOS process, achieving a suppression of the interleaving spur within the first Nyquist zone to below −63 dBc. The SFDR is significantly improved, exceeding 61 dB across the whole first Nyquist zone. During normal operation, the power consumption is 363 mW and with an active area of 1.47 mm^2. Compared to state-of-the-art 2×TI-DACs, this work achieves the best figure of merit (FoM) of 6.7×10^4.

This article is organized as follows. Section II presents the architecture overview of provideI-DAC and the impact of

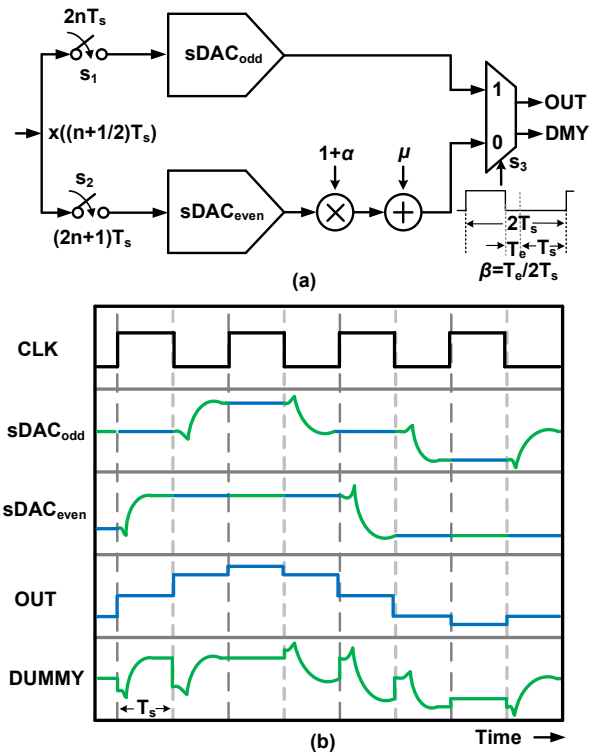


Fig. 1. (a) Block diagram of a 2× TI-DAC, including GEM, OSM and DCE. α, μ and β are the normalized value of GEM, OSM and DCE, respectively. T_e is the time duration of DCE. (b) Operation timing diagram of a 2× TI-DAC with no interleaving errors.

nonlinearities within the first Nyquist zone and provides insights into the calibration approach. Section III introduces the calibration scheme. Section IV delves into the circuit details. The measurement results and conclusions are presented in Sections V and VI, respectively.

II. Interleaving Nonlinearities Analysis and SFDR Estimation

A simplified block diagram of the TI-DAC is depicted in Fig. 1(a). It consists of two identical cores, each independently processing even and odd samples at half the rate of $f_s/2$ (2 GS/s). The outputs of the two sDACs are multiplexed by a 2:1 analog multiplexer (AMUX) using a half-rate clock (CLK). The operational timing of CLK and even/odd data signals is illustrated in Fig. 1(b), where CLK is an ideal clock with a 50% duty cycle.

The interleaved architecture mitigates most settling-related errors commonly occurring in current-steering DACs, but it also introduces certain non-ideal factors that can degrade performance. For instance, GEM and DCE can lead to an interleaving spur at $f_s/2$-f_0 for any signal tone of f_0. Additionally, spurs due to OSM may appear at DC and $f_s/2$. Another existing timing error is sampling phase mismatch. However, small mismatches do not cause deviations in the sampled digital input, and the interleaving structure can mitigate sDAC settling errors. Therefore, its impact is not considered in this work.

Detailed mathematical models of these non-idealities and comprehensive analyses in both time and frequency domains

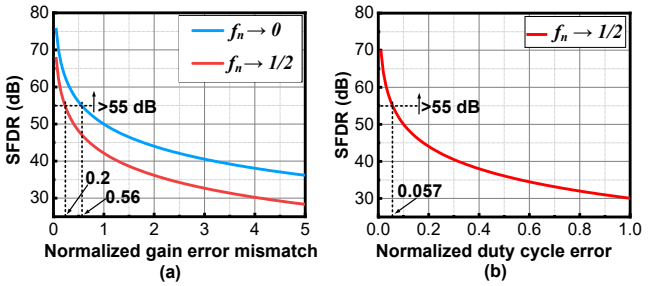


Fig. 2. The simulated SFDR varies with (a) normalized gain error mismatch and (b) normalized duty cycle error.

are provided in Appendix A, establishing relationships between SFDR and interleaving errors as below:

$$\mathrm{SFDR}=-20\log_{10}\left|2\pi f_n\beta+\frac{\alpha}{2+\alpha}\cdot\frac{2f_n}{1-2f_n}\cot(\pi f_n)\cos\left[\pi(1-2f_n)\beta\right]\right| \quad (1)$$

where the normalized DCE β is defined as $T_e/2T_s$, f_0 is a frequency of a single-tone signal used to excite DAC, the normalized frequency f_n is defined as $f_n=f_0/f_s$.

A. Gain Error Mismatch

As analyzed in appendix A, the GEM α affects both the fundamental amplitude and the amplitudes of the interleaving spur located at $f_s/2$-f_0. To investigate the impact of α on SFDR, β is set to 0 in (1), and the resulting SFDR is

$$\mathrm{SFDR}_\alpha=-20\log_{10}\left|\frac{1}{2/\alpha+1}\cdot\frac{2f_n}{1-2f_n}\cot(\pi f_n)\right| \quad (2)$$

With a fixed α, an increase in the input signal frequency results in a monotonic decrease in SFDR, signifying a decline in DAC's linearity. Therefore, it is crucial to analyze situations in which the single-tone frequency approaches the boundaries, particularly as f_n approaches 0 and 1/2. By applying trigonometric approximations, (2) can be simplified to

$$\mathrm{SFDR}_\alpha\big|_{f_n\to 0}=-20\log_{10}\left|\frac{2}{\pi(2/\alpha+1)}\right| \quad (3a)$$

$$\mathrm{SFDR}_\alpha\left|_{f_n\to\frac{1}{2}}\right.=-20\log_{10}\left|\frac{\pi}{4/\alpha+2}\right| \quad (3b)$$

As shown in (3), given the small α value, the denominator tends to be dominated by α, with every doubling of α leading to 6-dB degradation in SFDR. Fig. 2(a) depicts the relationship between SFDR and GEM at the DC input ($f_n\to 0$) and at the Nyquist input ($f_n\to 1/2$). It is evident that a smaller GEM results in a better SFDR. It should be noted that the SFDR with normalized output frequency approaching Nyquist is poorer than the SFDR with normalized output frequency approaching DC.

B. Duty Cycle Error

By setting α=0 in (1), the effect due to interleaving DCE can be isolated as shown below

$$\mathrm{SFDR}_\beta=-20\log 10\left|2\pi f_n\beta\right| \quad (4)$$

Similarly, SFDR decreases monotonically as f_n increases. When f_n remains constant, doubling the DCE results in a 6 dB decrease in SFDR. Additionally, with f_n approaching DC, the

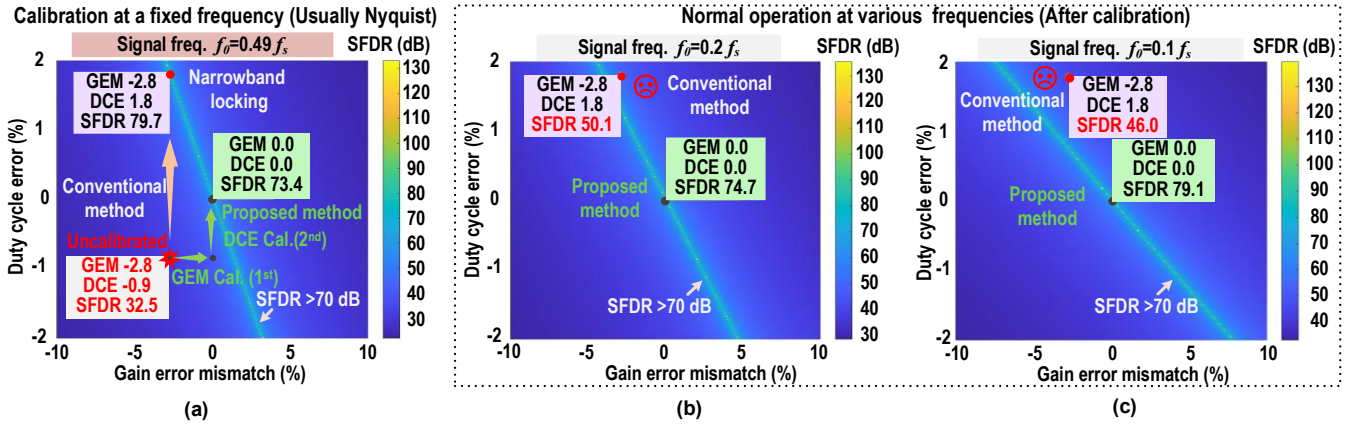


Fig. 3. Comparison of systematically simulated SFDR between the conventional and proposed single-tone calibration methods, highlighting the phenomenon of narrowband locking.

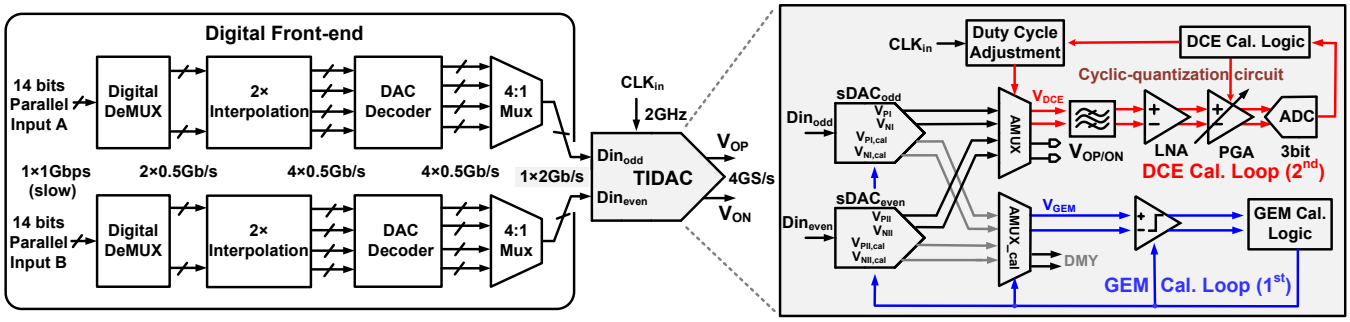


Fig. 4. System diagram of the proposed 2x TI-DAC with the proposed on-chip calibration scheme.

spur introduced by the DCE is too small to be observable. But when f_n approaches the Nyquist frequency, the changes of DCE have a significant impact on SFDR, as shown in Fig. 2(b). In this design, we target an SFDR larger than 55 dB, which implies β less than 0.057%. It is challenging to measure such a small DCE. In our proposed DCE calibration, this is achieved by indirectly monitoring the amplitude of the interleaving spurs induced by DCE.

C. Offset Mismatch

It is proved that the offset mismatch μ is independent of f_n and does not degrade the SFDR of the TI-DAC, as shown in Appendix A. Based on the derived equation $Y_s(j\omega)$, which is a frequency-domain representation related to OSM, $Y_s(j\omega)$ only exhibits components at integers multiple $\omega_s/2$. We can further analyze the frequency characteristics and components induced by OSM, by setting k to 0, 1, and 2, then three spurs in the frequency interval of $[0, f_s]$ can be approximated as

$$Y_{s0}(j\omega)=\mu\left(\pi+\frac{\omega_s\beta}{2}\right)\delta(\omega) \qquad 5(a)$$

$$Y_{s1}(j\omega)=-2\mu\cos\left(\frac{\omega_s\beta}{4}\right)\delta\left(\omega-\frac{\omega_s}{2}\right)e^{-j\frac{\pi-\omega_s\beta/2}{2}} \qquad 5(b)$$

$$Y_{s2}(j\omega)=-\mu\sin\left(\frac{\omega_s\beta}{2}\right)\delta(\omega-\omega_s)e^{-j(\pi-\omega_s\beta/2)} \qquad 5(c)$$

It can be observed that spurs due to OSM do not appear within the first Nyquist frequency zone, thus SFDR is insensitive to OSM. Additionally, the amplitudes of these three spurs are also influenced by DCE, but the effect of offset mismatch is predominant. Apparently, reducing μ to zero entirely removes these three harmonics, altering β does not produce similar impacts.

D. Joint Impact of GEM and DCE on SFDR

Since α and β have significant effect on SFDR for f_n closed to 0.5, (1) can be simplified by approximating f_n to 1/2 and assuming α is sufficiently small (e.g. $\leq\pm$0.227%) and is obtained without considering other non-ideal factors while targeting SFDR larger than 55dB. The resulting SFDR in terms of α and β is

$$\mathrm{SFDR}\left|_{f_n\to\frac{1}{2}}=-20\log_{10}\left|\pi\beta+\frac{\pi}{4}\alpha\right|\right. \qquad (6)$$

To attain an SFDR more than 55 dB, the total sum of $\beta+\alpha/4$ should be less than 0.18%. In fact, infinite SFDR can be attained if the absolute value in (1) becomes zero, which relates the GEM to DEC and f_n as follows:

$$\alpha=\frac{2}{(1-2f_n)\pi\beta/\cot(\pi f_n)+1}-2 \qquad (7)$$

From (7), it is clear that large SFDR can be obtained by tuning α or β. However, this is only effective at one particular f_n. Furthermore, the simulated results of SFDR as a function of α and β at various normalized input frequencies are plotted in Fig. 3. Note that as long as the GEM and DCE satisfy (7), an extremely high SFDR can be achieved. But such an SFDR can only be achieved at one f_n value instead of entire Nyquist bandwidth, because the cancellation is only effective for certain combination of α and β at particular f_n. As shown in Fig. 3(a), due to narrowband locking, the conventional single-tone calibration can achieve good SFDR at the

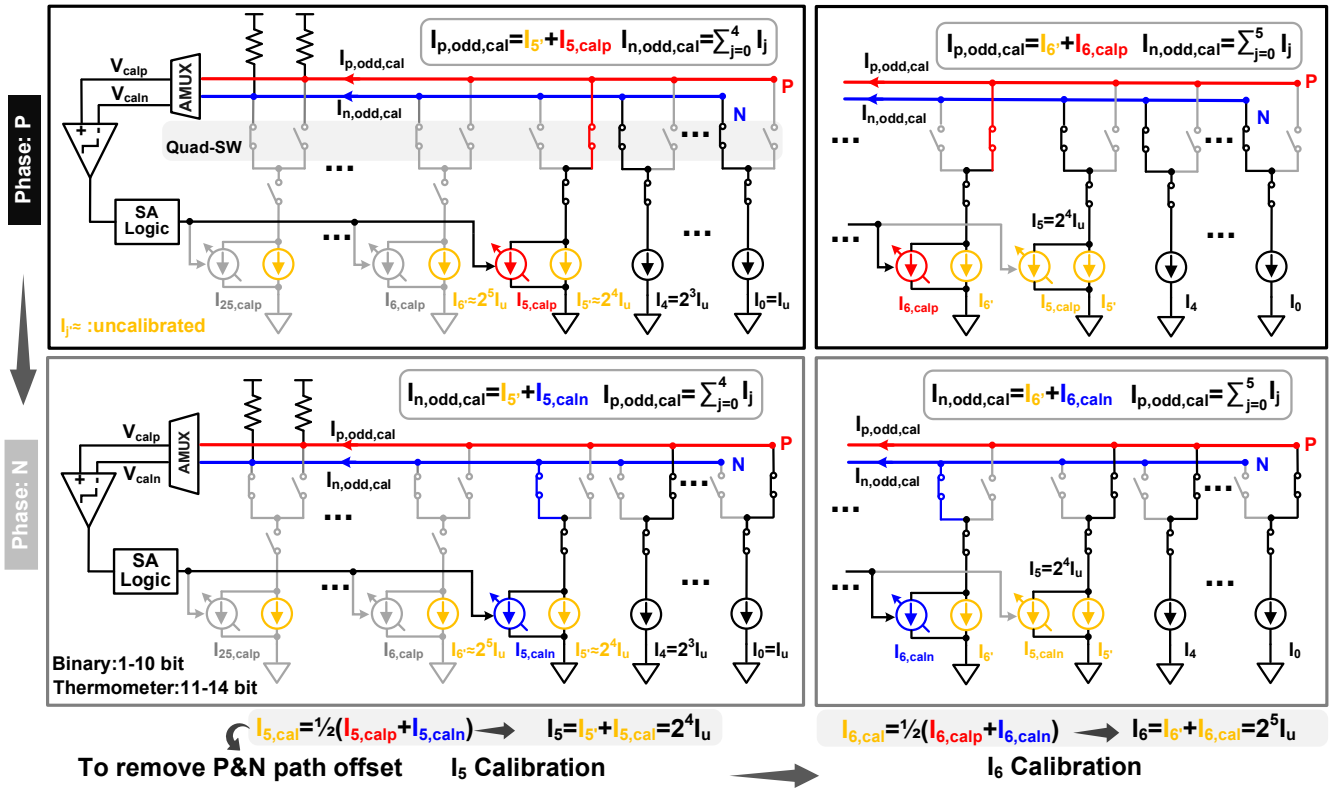


Fig. 5. Example of the CSM calibration of 5th bit and 6th bit in $sDAC_{odd}$ during the proposed GEM calibration process.

Nyquist input. However, as the input signal frequency changes, SFDR rapidly degrades, as illustrated in Fig. 3(b) and (c). Based on our theoretical analysis, to achieve a good SFDR across the entire Nyquist zone with single-tone calibration, GEM calibration should be performed first, followed by DCE calibration. A similar current source mismatch (CSM) calibration was performed first and then DCE calibration was used in [29], but it does not address interleaving mismatches, such as GEM and timing skew, which are critical in TI-DACs.

For medium/low-resolution DACs (less than 9 bits), GEM usually can be ignored, and a moderately good SFDR can be achieved solely through DCE calibration [17]. However, in high-resolution DACs, GEM cannot be ignored for achieving a higher SFDR. According to (7), a straightforward approach is to calibrate GEM or DCE, once f_n changes. However, this is impractical and time-consuming. In this work, GEM is first reduced to a negligible level, followed by DCE calibration, ensuring a good SFDR across different input frequencies, as illustrated in Fig. 3 and later from our measurement. This two-step calibration approach eliminates the issue of having DCE calibration partially correcting the error due to GEM at one particular frequency, resulting in sub-optimal performance of DCE calibration at other frequencies, which leads to the narrowband locking phenomenon. It should be noted that our approach did not correct frequency dependent error associated with timing skew and duty-cycle errors. Hence, we will still expect degraded SFDR performance at higher input signal frequencies. The details of the proposed two-step calibration approach will be discussed in the following section.

III. System Implementation with Calibration

Fig. 4 illustrates a block diagram of the proposed DAC system. In the digital front-end, two parallel data of 14 bits with 1-Gbps bit rate are initial input, and then, after 2× interpolation, they are converted into four 0.5-Gbps signals. Internal interpolation is adopted due to frequency limitations of package pins and digital circuits. The input signals are decoded and converted into two 14-bit 2-Gbps signals through 4:1 MUXs, which are input into the sDACs within the TI-DAC. Subsequently, the two analog outputs undergo a 2 GHz dual-edge-triggered 2:1 AMUX and the 4-GSps differential output signal is obtained.

For high-precision DACs, not only GEM and DCE need to be calibrated to suppress interleaving spurs, but also CSM of sDACs must be considered. According to the results in Section II, achieving an SFDR of 55dB for AMUX operating at 2 GHz, the frequency of AMUX requires the DCE to be less than 285 fs, making the direct measurement challenging. To reduce hardware overhead, the DCE calibration can be realized by monitoring the interleaving spur for f_n approaching 0.5. In addition, for the proposed two-step calibration approach, GEM needs to be calibrated first before DCE to eliminate narrowband locking. Thus, we propose a static calibration of both GEM and CSM in the first step, followed by DCE calibration. It should be noted that the proposed approach is hardware-friendly for on-chip implementation.

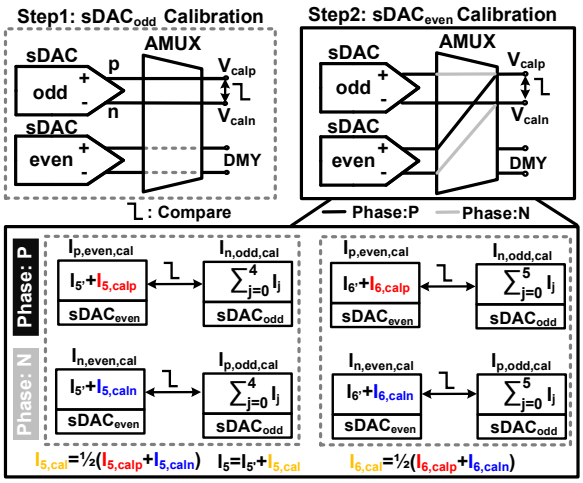


Fig. 6. Example of the calibration of 5th bit and 6th bit in sDAC$_{even}$.

A. Calibration of sDACs' Nonlinearity and Gain Error Mismatch

Conventional calibration methods may encounter substantial hardware and power penalties, like the use of a high-precision ADC. Although [18] concludes that high linearity ADC is not required, ADC still needs enough bits to ensure that calibrated differential non-linearity (DNL) of DAC is small enough to achieve a good SFDR. To reduce the hardware complexity and overhead, we propose a foreground GEM and CSM calibration method that requires only one high-precision comparator.

In this work, the sDACs' absolute current mismatch in the four LSB bits (D[3:0]) can be effectively minimized, so the current source calibration is initiated from the current source controlled by D[4], which has current of 2^5 I_u. The example of source calibration is shown in Fig. 5. The calibration of current source controlled by D[4] is divided into P and N phase. In P phase, the current source required calibration is connected to the P output terminal of the sDAC, while all current sources controlled by the lower LSB bits (D[3:0]) are steered into the N output terminal. Based on the results of the comparator and successive approximation (SA) logic, the compensation current source, $I_{5,calp}$ will then be added to the current source controlled by D[4] to ensure the close matching between the N and P output terminal. In phase N, the above procedure is repeated by swapping the current sources between P and N output terminals. Finally, the calibration codes obtained from the two phases are averaged to eliminate the effects of the path offset. The whole process is repeated for higher bits throughout the CSM calibration process for sDAC$_{odd}$.

Notably, to reduce additional hardware overhead for GEM calibration of two sDACs, we further improve the current calibration of sDAC$_{even}$. As shown in Fig. 6, after completing the CSM calibration of sDAC$_{odd}$, the calibration of sDAC$_{even}$ follows, using sDAC$_{odd}$ as a reference for cross-comparison. This cross-comparison is realized through AMUX and the following comparator. The calibration procedure remains the same as that for sDAC$_{odd}$, except that the current source controlled by D[4] in sDAC$_{even}$ is compared with the sum of the current sources controlled by D[3:0] in sDAC$_{odd}$. This approach enables the simultaneous compensation of both the CSM of sDAC$_{even}$ and the GEM of the two DACs. Moreover, the cross-comparison does not degrade DNL/INL because: (1) the high-precision comparator undergoes a three-stage offset self-calibration to minimize error introduction; (2) the two-phase averaging strategy systematically cancels out mismatches by swapping the reference and input during calibration; (3) The unit current source dimension is deliberately minimized to reduce parasitics, while a mismatch margin of four times the standard deviation ensures sufficient correction capability; and (4) the sequential reference incorporation method ensures that the calibrated current sources from sDAC$_{odd}$ are progressively used as references for sDAC$_{even}$ calibration, maintaining consistency and alignment between both DACs.

Additionally, the current sources controlled by D[4:13] are intentionally designed to be smaller than their ideal binary-weighted currents, so that after accumulating the current sources needing calibration with the corresponding calibration sources, the total currents can approach their ideal values. Moreover, high-speed DACs are extremely sensitive to the load connected to the output port. Placing an on-chip comparator at the actual output of the TI-DAC would unavoidably result in a bandwidth reduction. To address this issue, a dedicated calibration output path is designed in this work. The specific circuit implementations are introduced in Section V.

B. Calibration of DCE using Cyclic-Quantization Circuit

To eliminate the dependency on off-chip devices or high-resolution ADCs, which are usually adopted in conventional calibration methods, we propose a hierarchical uniform grid search method to find the optimal DCE compensation point. In addition, a cyclic-quantization circuit is proposed for the interleaving spur extraction during the search process. It consists of on-chip 3-bit ADC, a bandpass filter (BPF), a low-noise amplifier (LNA), and a programmable gain amplifier (PGA).

The detailed DCE calibration loop is illustrated in Fig. 4. A simplified block diagram and the transient simulation results are shown in Fig. 7. The loop is connected to the dummy output node of the TI-DAC. When calibrating, a high-frequency sinusoidal input is applied to the DAC, and the sampling phase of sDACs is inverted to send resulting DAC output signal to be output to the DUMMY end. The output is first fed into a BPF to extract out the interleaving spur. This is then followed by an LNA and a PGA to amplify the spur amplitude before sending it to a 3-bit flash ADC to quantify the spur amplitude.

As shown in Fig. 7, a random DCE's optimal calibrated point is assumed to fall to point x (0.33), which is also the desired compensation point. The proposed DCE calibration method is divided into four-level grid searches, quantifying the spur amplitudes of DCE on $2\times2^2+1$ grid points in each level. In the first-level grid search, the initial DCE compensations range is from -0.8% to +0.8%, with an interval of 0.2%. According to (4), the spur amplitude will be mapped to each grid point, and it increases linearly on both sides of the lowest amplitude (i.e. optimal compensation point), referred as unimodal linearity. This property allows the calibration procedure to concentrate exclusively on the

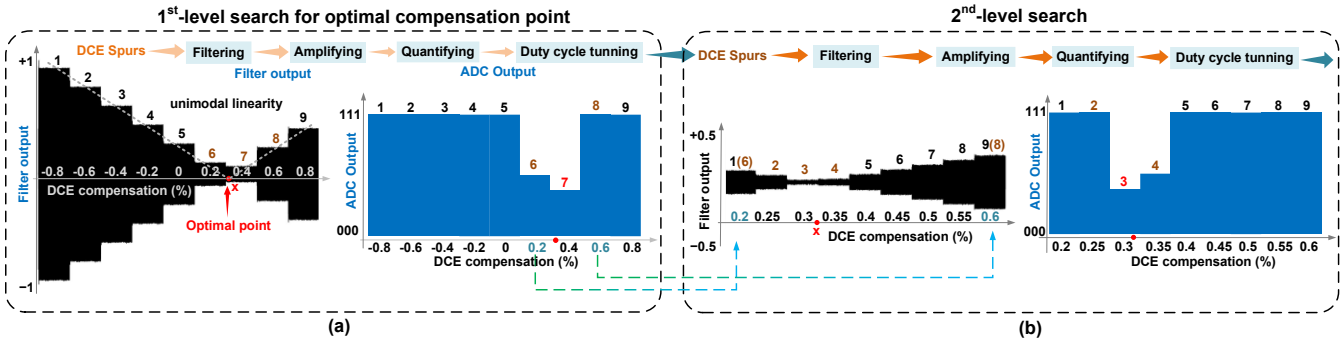


Fig. 7. The proposed DCE calibration scheme.

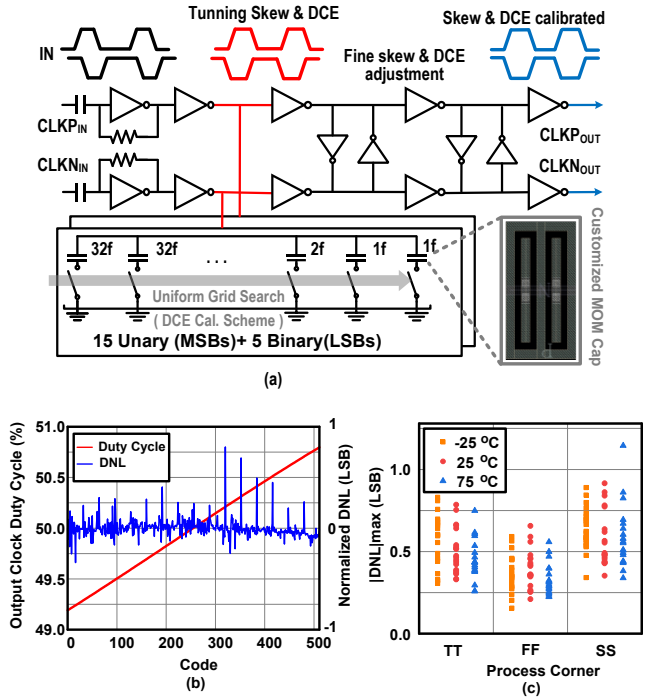


Fig. 8. (a) Clock generation circuit with DCE compensation arrays. (b) Simulated DNL of DCE compensation, and (c) maximum DNL distribution from 20 Monte Carlo simulations across different corners and temperatures.

interval containing the minimum spur, eliminating the necessity for high-precision quantization in all intervals employed in conventional approaches.

During the 1st level search, once the minimum point is found (i.e., point 7), the left and right points of this minimum point are selected as a new range for the 2nd search, as shown in Fig. 7 (a). Because point 6 and point 8 encompass the whole region that contains the minimum point. Similarly, point 2 and point 4 will be selected as a new range for the third level search, as shown in Fig. 7 (b).

The required gain of the PGA is obtained through manually introducing specific DCEs into simulations. Additionally, this gain is halved to effectively double the maximum quantization range at each calibration level, thereby providing sufficient redundancy to address the mismatch between the PGA gain and the DCE compensation amount. The remaining interleaving spur after the BPF linearly reduces with the injected duty cycle compensation.

In conclusion, the proposed DCE calibration method is realized using on-chip circuits without large computing overheads. Because the auxiliary ADC has two storage units, at each compensation grid point, it compares each quantized output code of the ADC with the stored codes, only storing the maximum and minimum values iteratively. After a sufficient number of samples, the stored maximum and minimum values are subtracted to obtain the amplitude of the interleaving spur corresponding to that compensation point. The input signal frequency for the foreground calibration is set at 1.999 GHz, placing the time-interleaving spur at 1 MHz, which results from the trade-off among in-band noise, PGA gain, filter area, and calibration time.

IV. Core Circuit Details

The clock generation circuit employs AC-coupled input clocks fed into the first inverter stage, as shown in Fig. 8, which is biased at its switching point using feedback resistors. Coarse DCE correction is achieved at this initial stage [30]. For fine adjustments, a digitally controlled 2×9-bit capacitor array and two cross-coupled inverter-based latches are used to modify both duty cycle and timing skew. The capacitor array introduces controlled delays to both clock signals, while the latches convert excess timing skew into anti-phase DCE compensation, effectively canceling intrinsic DCE and timing skew [31]. The jitter introduced by the clock generation circuit is approximately 10 fsrms. In this case, the smallest step size is ±0.003125% (±15.6 fs), which is overdesigned to achieve optimal performance initially. Fig. 8(b) and (c) show the simulated DNL of the DCE compensation circuit with random mismatch. The DNL of the circuit remains below 0.8 LSB in typical condition (TT, 25°C). Furthermore, its monotonicity is preserved in most cases, even when considering process and temperature variations. Combined with the inter-level redundancy incorporated in the grid search, this monotonicity ensures that the DCE calibration can converge.

As shown in Fig. 9, the TI-DAC core consists of two current-steering sDACs and two 2:1 AMUXes. Each sDAC outputs two sets of differential currents. The TI-DAC has eight output ports, connected to the power supply via off-chip load resistors. AMUX(CAL) is employed exclusively during foreground calibration. The two CS sDACs are implemented with 10-bit binary-coded LSBs associated with 4 thermometer-coded MSBs. In this work, the thermometer coded MSBs are purposely chosen to be fewer than conventional DAC design to reduce the number of comparisons needed for CSM/GEM calibration. This helps

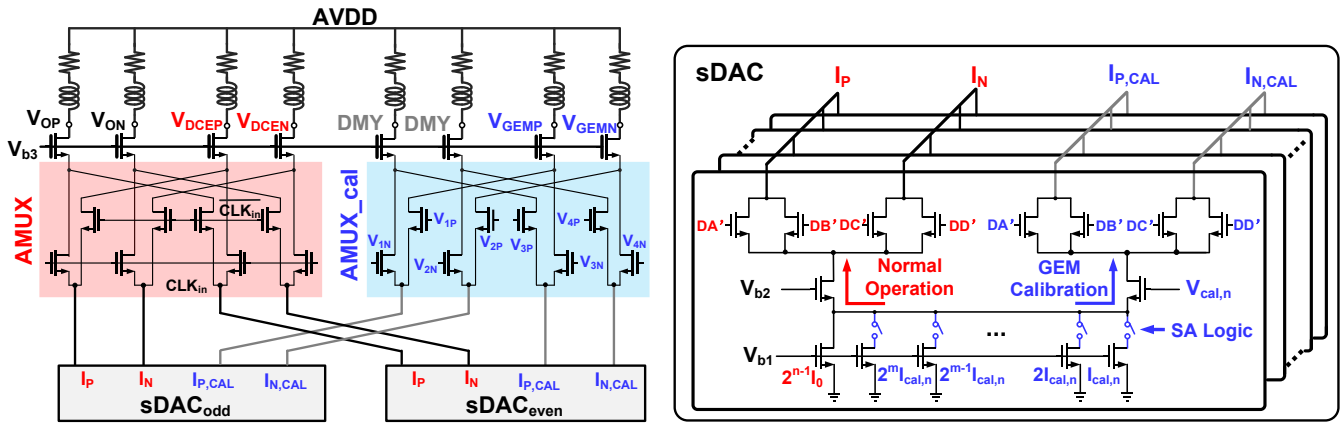


Fig. 9 The proposed 2x TI-DAC.

improve CSM calibration accuracy, reduces current calibration array switches, and simplifies the binary-thermometer decoding circuit. It should be noted that during static GEM calibration, the quad-switches operate at a lower frequency. As a result, smaller digital drivers are employed, resulting in insignificant overhead less than 1%. The additional dummy branch will incur one additional cascode transistor and one quad-switch per cell, as well as one additional AMUX. The cascode transistor contributes to additional 21% area overhead of the total current source array. As quad-switch size is related to current source size and dominated by the MSB cell, the quad-switch is shared among all MSB bits in the calibration path, reducing the area overhead down to 12.5% of the current source array. It should be noted that the above-mentioned area overhead is based on smaller current source area due to the relaxed passive matching requirement offered by the dummy branches. Hence, the area overhead percentage would be even smaller if a current source array with actual passive matching requirements is adopted.

The AMUX employs a source-coupled Gilbert-cell topology similar to [32]. The circuit consists of two interleaved switching paths, where linearized transconductance stages serve as the primary data inputs, ensuring stable signal conversion. Above them, cascode current switches, driven by a differential half-rate clock, perform nonlinear current steering by directing the respective input signal either to the output path or a dummy path, effectively mitigating nonlinear distortions. These common-gate isolation transistors further prevent unwanted loading effects. To increase DAC linearity, switch size is tailored to match the magnitude of the current sources they control. However, this causes variable delays in control signals for different bits, leading to timing discrepancies between summing currents from each branch, and affecting high-speed performance. To address this, each quad switch is paired with a phantom switch, sharing the same control signal, ensuring uniform parasitic capacitance across all bits. Moreover, shunt and series peaking inductors extend the effective output bandwidth, while bleeding currents of 4mA are also added to improve CS DAC linearity [17]. Additionally, a clock correction circuit is implemented to simultaneously calibrate timing skew and duty-cycle mismatch, ensuring precise interleaving and minimizing jitter-induced signal degradation. By incorporating design optimizations such as noise isolation,

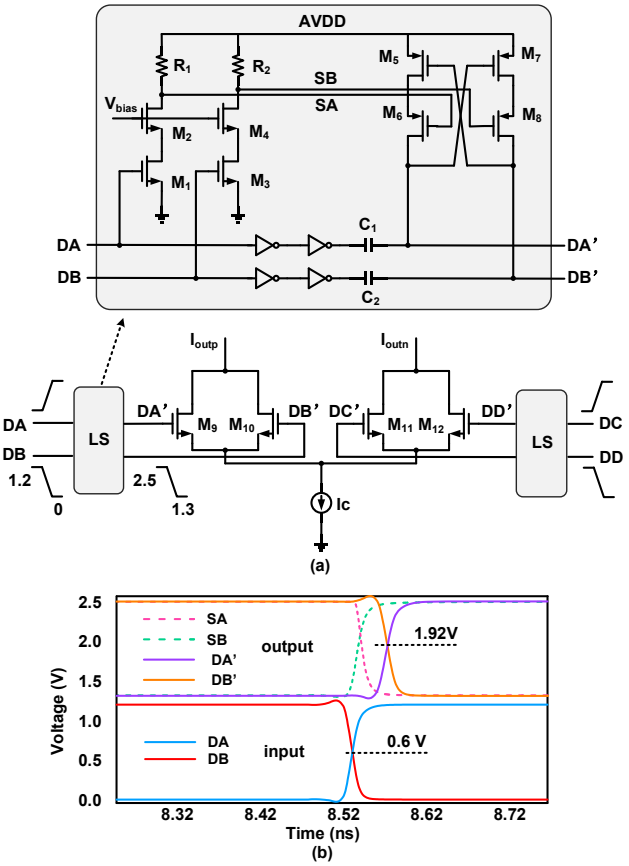


Fig. 10. (a) The proposed capacitor-based level shifter. (b) Simulated waveforms

parasitic reduction, layout matching, negative supply utilization [33], and clock calibration, the conventional AMUX architecture remains a viable solution for high-speed TI-DACs. In advanced process with lower supply voltages, AMUX may suffer from reduced signal swing and more distortion. In addition, precise clock signals are required to prevent interleaving spurs caused by duty cycle and timing mismatches. As a result, AMUX faces challenges such as additional noise, voltage headroom constraints, timing mismatches, and switching delays when adopted in high-speed TI-DACs.

To enhance the output impedance and operating speed, cascode NMOS transistors are utilized as current sources. A quad switching method is applied to the switches [34], ensuring output independence from the varying input code.

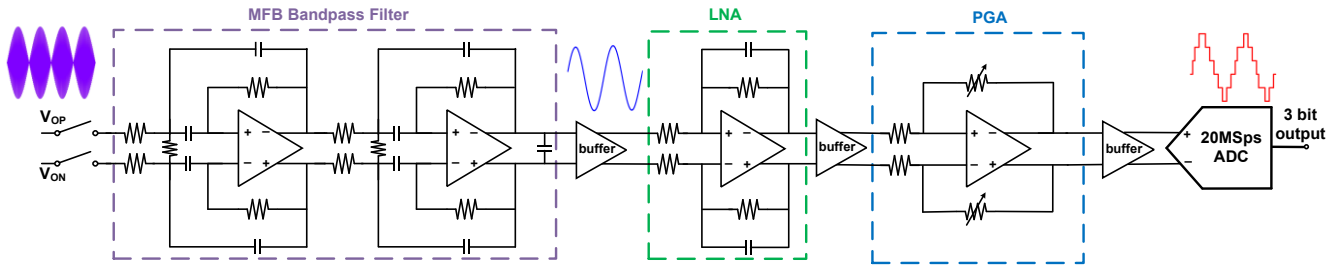


Fig. 11. The proposed cyclic-quantization circuit for interleaving spur extraction in the DCE calibration loop.

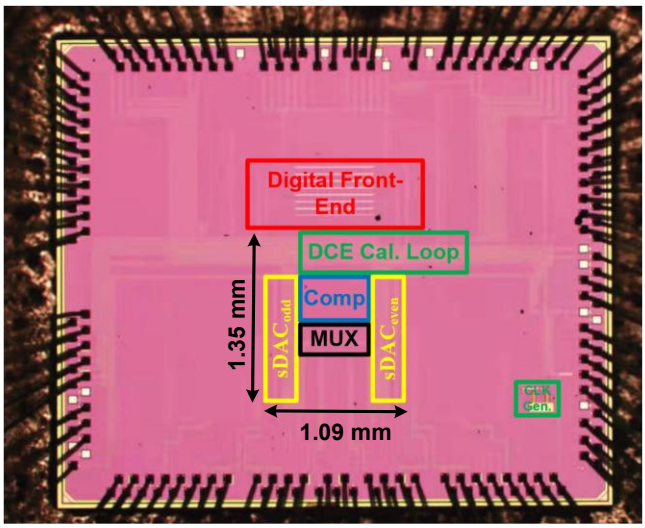


Fig. 12. Chip microphotograph of the proposed 14-bit 2-time interleaved 4-GSps DAC, using a 65-nm CMOS proces.

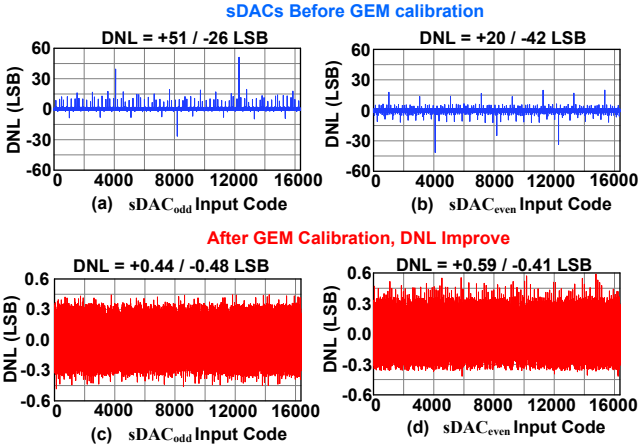


Fig. 14. Comparison of measured worst DNL across 20 chips measurement before GEM calibration and improved results after the calibration.

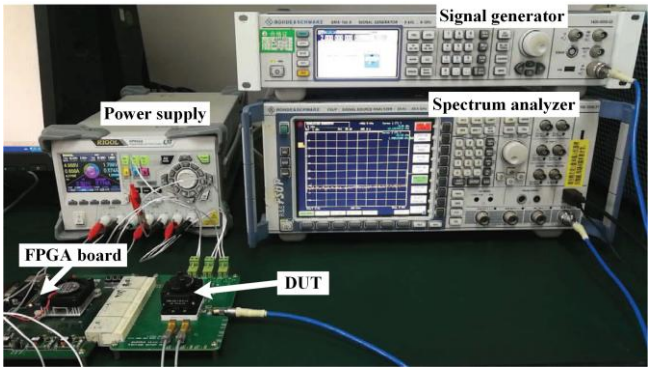


Fig. 13. Overview of measurement setup.

To increase DAC linearity, switch size is tailored to match the magnitude of the current sources they control. However, this causes variable delays in control signals for different bits, leading to timing discrepancies between summing currents from each branch, and affecting high-speed performance. To address this, each quad switch is paired with a phantom switch, sharing the same control signal, ensuring uniform parasitic capacitance across all bits.

Each current source transistor is paralleled with a binary-weighted calibration array. To mitigate parasitic capacitance and offset the additional area introduced by the calibration branches, the transistor sizes are reduced, which, in turn, increases the current mismatch to approximately 3%. Based on the standard deviation of each current source, the number of bits in the calibration array for each bit is designed to vary between 3 to 7 bits. The unit current $I_{cal,n}$ in the calibration array, is also determined by the same consideration. The two cascode transistors above the current source will determine whether the current is sent to the path for normal operation, or to the path for CSM/GEM calibration. It should be noted that during calibration, the quad-switches will operate at a lower operating frequency. A single quad-switch is shared among all MSB bits in the calibration path, effectively minimizing the overhead of the calibration branches.

To control the quad-switch transistors on the 2.5V-supply path, a level shifter is utilized to raise the logic level from 1.2 V to 2.5 V. We propose a capacitor-coupled level-shifter, seen in Fig. 10(a), that contains a cross-coupling unit, a delay inverter, and coupling capacitors. The control signals DA and DB have opposite potential. The conducting path charges one coupling capacitor to (AVDD-DVDD) ·C, while the other coupling capacitor remains floating. As a result, the quick changes in the switch signal alternately recharge the two coupling capacitors. The intersection of the rising/falling edge on the transition point is decided by the cross-coupling unit's common-mode level. As shown in Fig. 10(b), simulated results show that the common-mode level is shifted from 0.6 V to 1.92 V.

Fig. 11 shows the proposed cyclic-quantization circuit (CQC) for the spur extraction in the DCE calibration. A 2nd-stage active bandpass filter with a multiple feedback (MFB) topology is employed. It has a lower and an upper cutoff frequency of 600 kHz and 2 MHz, respectively, to effectively suppress out-of-band noise and spurs. The gain of the LNA is 20 dB, and the PGA has an adjustable gain range from 20 dB to 56 dB with a gain step of 12 dB. This PGA gain increases incrementally as the DCE compensation range decreases. The key consideration for the LNA and PGA is noise reduction,

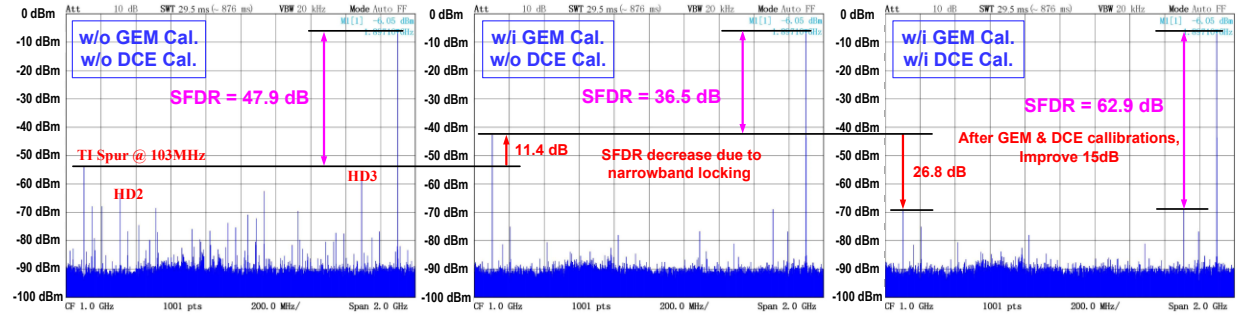


Fig. 15. Measured output spectra with an input of 1.897 GHz and a sampling rate of 4 GS/s. (a) Before calibration. (b) After GEM calibration. (c) After DCE calibration.

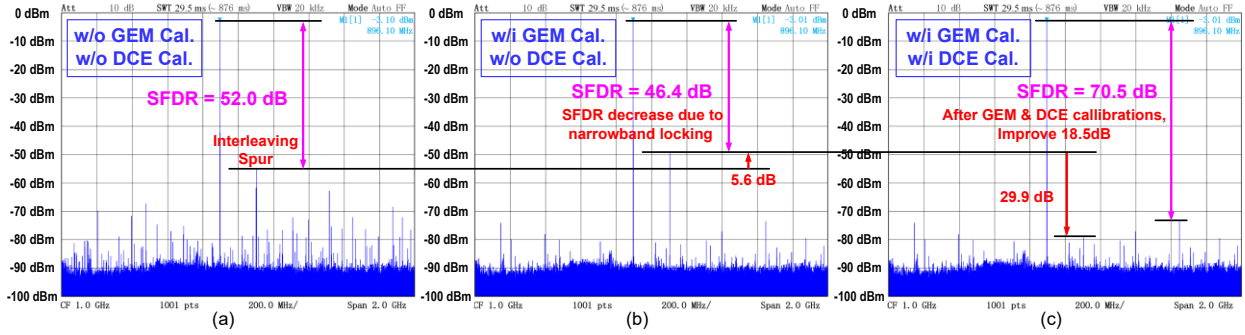


Fig. 16. Measured output spectra with an input of 896 MHz and a sampling rate of 4 GS/s. (a) Before calibration. (b) After GEM calibration. (c) After DCE calibration.

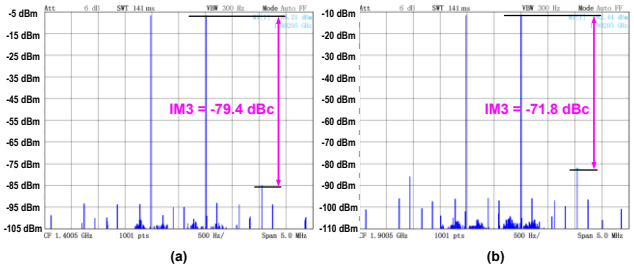


Fig. 17. Measured two-tone spectra at 4GSps, with center frequencies of (a) 1.405 GHz, and (b) 1.905 GHz.

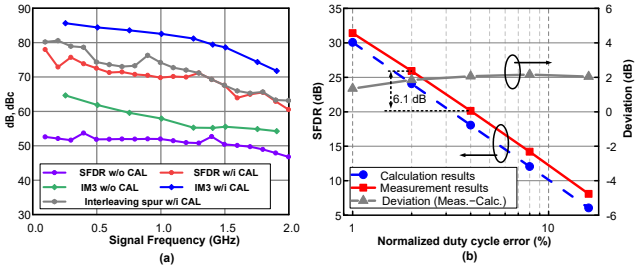


Fig. 18 (a) Measured SFDR and IM3 with/without on-chip calibration and calibrated interleaving spur with different signal frequencies. (b) Measured SFDR under different DCEs.

without any explicit requirements for linearity, as long as monotonicity is ensured. The auxiliary ADC adopts a typical flash structure with offset averaging, with only 3 bits of accuracy and a sampling rate of 20 MHz. The primary design consideration for the LNA and PGA is noise suppression, ensuring that the in-band noise remains below half of the minimum spur resolution of 80 μV, without stringent linearity requirements as long as monotonicity is preserved. Simulations indicate that the equivalent input noise of the CQC front end is 27 μVrms, with a total harmonic distortion (THD) of -44 dB.

Additionally, the high-precision comparator for GEM calibration employs a 5-stage preamplifier to suppress the input offset of the following latch. Output offset storage (OOS) is incorporated after the 1st, 2nd, and 4th stages. Each preamplifier stage provides approximately 10 dB of gain to ensure that the stored output offset voltage on the following capacitor does not saturate. Before calibrating each bit, the DAC's output common-mode voltage is extracted, and an OOS is performed to account for variations in comparator input offset due to changes in the output common-mode voltage during the calibration. The comparator operates at a frequency of 1 MHz, achieving a precision of 17 bits, with a power consumption of 8.9 mW. After calibration, the comparator is turned off to achieve power saving.

V. Measurement Results

The proposed 14-bit 4-GSps TI-DAC was fabricated in a TSMC 65-nm CMOS process. The microphotograph of the chip is shown in Fig. 12. Each sDAC, including the current calibration array, occupies an area of 0.24 mm². The area for the DCE calibration loop is about 0.39 mm². The total active area of the TI-DAC is approximately 1.47 mm², including on-chip calibration circuits and clock circuits.

The power consumption of the TI-DAC is 363 mW when operating at 4 GSps, excluding calibration circuits. It is capable of delivering a maximum output current of 16 mA, in conjunction with external 25-ohm load resistors, and achieves a differential output swing of 0.8 Vpp. The digital supply voltage is 1.2 V, and the analog supply voltage is 2.5 V.

The measurement setup, illustrated in Fig. 13, comprises the design-under-test (DUT) chip, various power supplies, a Rohde & Schwarz 6-GHz signal generator SMA-100A, a

TABLE I
COMPARISON WITH STATE-OF-THE-ART TIME-INTERLEAVED DACS

	This work	JSSC 2015 [17]	TCAS-II 2018 [1]	JSSC 2021 [23]	TCAS-I 2022 [25]	TVLSI 2023 [31]	TCAS-I 2023 [40]	ISSCC 2018 [29]
Architecture	2 × Time-interleaving						Single Channel	
Technology [nm]	**65**	28 FDSOI	65	16	14	65	65	16
Supply [V]	**1.2/2.5**	1	1.2	0.8	N/A	1/2.5	1.0/2.5	1.0/3.0
Power [mW]	**363**[c]	110	136	88	N/A	613	849	350
Core Area [mm^2]	**1.47**[d]	0.04	0.072	0.03	N/A	1.05	0.85	0.52
Resolution [bits]	**14**	9	6	8	10	14	16	16
Sampling Rate [GSps]	**4**	11	20	28	40	6	4	6
SFDR$_{low\text{-}freq}$ [dB]	**78**	59	46	47	N/A	61	80	88
SFDR$_{Nyquist}$ [dB]	**61**	52	35	37	48	52	65	67
Interleaving-spur$_{worst}$ [dBc]	**-63**	-55	-38	-37	-48	-62	N/A	N/A
IM3low-freq [dBc]	**-86**	-70	N/A	-60	N/A	N/A	-88	-92
IM3Nyquist [dBc]	**-72**	-52	N/A	-37	N/A	N/A	-71	-73
FoM[a]	**6.7×10^4**	3.8×10^4	1.1×10^3	6.6×10^3	N/A	5.8×10^3	5.7×10^4	6.2×10^5
Calibration Type	**Auto/ On chip**	Manual/ Off-chip	N/A	Manual/ Off-chip	Auto/ Off-chip	Manual/ Off-chip	N/A	Auto/ On chip
Calibration Cost[b]	**Low**	Medium	N/A	High	High	High	N/A	Low

[a] $FoM = \frac{2^{\frac{SFDR_{Best}-1.76}{6.02}} \times 2^{\frac{SFDR_{Worst}-1.76}{6.02}} \times f_{clk}}{P_{total}-P_{load}}$ [35]. The larger the better.

[b] Consider the on-chip/off-chip hardware overhead used for extracting/compensating errors

[c] Power consumption of the foreground on-chip calibration are not included during normal operation.

[d] Including on-chip calibration circuits.

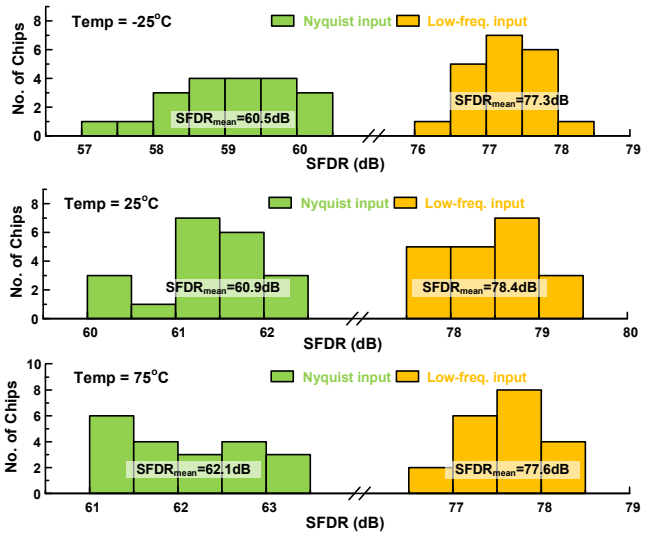


Fig. 19. Measured calibrated SFDR of 20 chips versus temperature.

26.5-GHz spectrum analyzer FSUP, and an FPGA board used for digital code generation.

The worst static linearity was selected from measurements on 20 chips to validate the effectiveness of the GEM calibration. The DNLs of two sDACs are shown in Fig. 14(a) and (b), reaching 51 and 42 LSB, respectively. After the CSM and GEM calibration of this TI-DAC, the measured DNLs, as shown in Fig. 14(c) and 14(d), are within 0.48 and 0.59 LSB, respectively.

Fig. 15 illustrates the spectrum of the DAC outputting a 1.897 GHz signal at a sampling rate of 4 GSps. Without any calibration, the achieved SFDR is limited to 48 dB due to the interleaving spur at 103 MHz frequency, as shown in Fig. 15 (a). After the GEM calibration, the interleaving spur increases by 11.4 dBc, as shown in Fig. 15 (b). This is because there is a partial cancellation of GEM and DCE before calibration, which is also proven by (7). Therefore, eliminating GEM through calibration, the SFDR deteriorates. Additionally, it can be observed that once internal nonlinearity in sDAC is calibrated, harmonics in the output spectrum are significantly suppressed. After the DCE calibration, the interleaving spur decreases by 26.8 dB. At this point, the SFDR of TI-DAC is limited to 62.9 dB by the 3rd harmonic. Additionally, after GEM calibration, the internal CSM within each sDAC is also corrected. As a result, the amplitude of several spurs observed in Fig. 15(a) is significantly reduced, as shown in Fig. 15(b) and (c).

Fig. 16 illustrates single-tone test results at a mid-band frequency. When the DAC outputs an 897 MHz signal at a sampling rate of 4 GSps, the interleaving spur is suppressed by 24.3 dBc after calibration, resulting in an SFDR improvement of 18.5 dB. The two-tone test results with a 3 MHz frequency offset are shown in Fig. 17(a) and (b). At center frequencies of 1.405 GHz and 1.905 GHz, the calibrated DAC achieves IM3 of -79.4 dBc and -71.8 dBc, respectively. Fig. 18(a) illustrates the SFDR and IM3 across

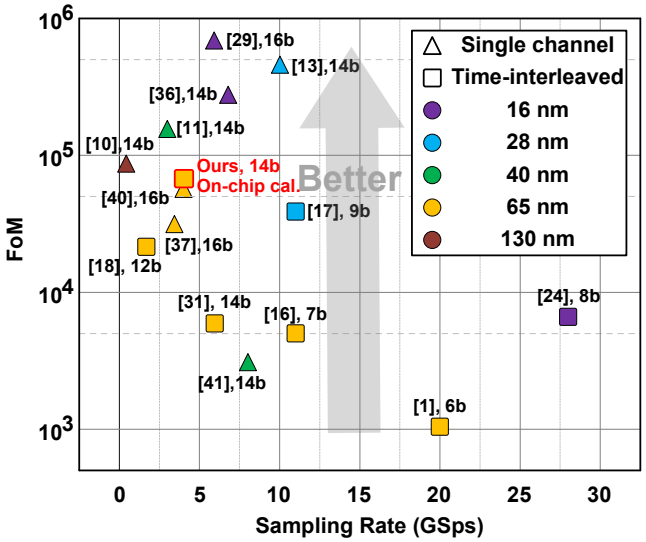


Fig.20. FOM comparison with other state-of-the-art single channel DACs and TI-DACs

different output frequencies, both before and after the completion of all calibrations.

The DCE calibration needs to be redone when the clock frequency changes, as the DCE and timing skew vary with clock frequency. However, GEM does not require recalibration in this case. To validate the mathematical model derived in this paper that links the DCE and GEM to the resulting interleaving spur, an experiment was also conducted to validate the accuracy of the model. In this experiment, timing errors are manually injected into the TI-DAC to mimic duty cycle errors, and the resulting interleaving spurs become the limiting factor for SFDR.

From our simulation, DCE only needs to cover +0.8 to -0.8%. However, to cater for model validation, we have purposely designed DCE to cover a much wider range, i.e. from 1% to 10%. At f_n=0.49, Fig. 18(b) displays both the calculated and measured SFDR. In the measurements, doubling the DCE results in a 6-dB degradation of the SFDR, which aligns with the theoretical calculations. However, a discrepancy of approximately 2 dB between the measured and calculated results is observed. This discrepancy may arise from several factors: the time model of the TI-DAC may not perfectly match the actual circuit due to non-ideal elements such as parasitic in the circuit, or non-ideal transmission attenuation with measurement devices and cables. Additionally, assumptions and approximations made during the formula derivation could contribute to this difference.

Fig. 19 shows the measured SFDR distribution (after calibration) of 20 chips at various temperatures. The measured worst $SFDR_{Nyquist}$ is 57.3 dB at -25°C, the best $SFDR_{Nyquist}$ is 63.2 dB. Most measured results of $SFDR_{Nyquist}$ and $SFDR_{low\text{-}freq}$ exceed 60 dB and 77 dB, respectively.

Table I summarizes the proposed 14-bit TI-DAC performance and comparison with state-of-the-art TI-DAC. By adopting the proposed calibration scheme, this work achieves the highest SFDR at both low-frequency and Nyquist inputs. Our work is the only reported DAC with on-chip calibration. Compared to [31] which is also a 14-bit DAC, we achieve a 10 dB better SFDR across the Nyquist band, albeit at slightly lower sampling frequency. Our FoM is also the best among all TI-DAC. The slightly larger area is due to the additional calibration DAC and on-chip calibration adopted in this work.

TABLE II
COMPARISON WITH HIGH-RESOLUTION ADC

	[38]	[39]	This work
Type	Pipeline-SAR ADC	NS-SAR ADC	Proposed calibration circuit
Process [nm]	55	55	65
ENOB [bit]	13.2	13.8	15.8*
BW [MHz]	0.5	11.95	10
Area [mm²]	4.1	5.4	**0.51**

*Calculated based on the input-referred noise and full-scale range of the cyclic quantization circuit.

As shown in Fig. 20, due to channel mismatches, the FOM of a TI-DAC is usually inferior to that of a single-channel DAC, especially when the process of the latter is more advanced (such as [13],[29],[36]). Additionally, these single-channel DACs should achieve higher operating speed by adopting time-interleaved architecture and better FOM by leveraging the proposed calibration techniques to minimize interleaving nonlinearities.

Table II illustrates the area advantage of our proposed cyclic quantization circuit in comparison with an equivalent high-performance ADC needed for the DCE calibration. The significant area overhead saving proves the feasibility of our proposed technique for on-chip calibration. As we can turn off the circuit after calibration, power is not a key consideration here.

VI. CONCLUSION

This paper presents a 14-bit, 4-GSps TI-DAC with a fully on-chip foreground calibration scheme, implemented in 65-nm CMOS technology. Our proposed two-step calibration approach based on time-domain SFDR analysis overcomes the narrowband locking issue, which commonly plagues the single-tone calibration technique. To facilitate fully on-chip calibration, a low-complexity uniform grid search algorithm, exploiting unimodal linearity of DCE-induced spurs, eliminates the need of high-resolution ADCs. We also introduce a cross-comparison calibration method to reduce sub-DAC calibration complexity. This work represents the first reported 2× TI-DAC with a fully on-chip low-complexity calibration scheme, while achieve the best SFDR and best FoM across the Nyquist frequency range while occupying only 0.51 mm² of calibration circuitry area.

APPENDIX A

MODELING AND INTERLEAVING ERRORS ANALYSIS OF 2-CHANNEL TI-DAC

A. Time-Domain Modeling

To evaluate the dynamic performance of the TI-DAC, the mathematical model of the TI-DAC (shown in Fig.1) is represented in Fig. 21. The input signal is characterized as a continuous-time analog signal $x(t)$. Then, the sDACs are modeled as unity gain amplifiers, where the noise e_{da} is introduced to simulate the random quantization noise. The gain error mismatch α and offset mismatch μ are equivalently represented at the respective inputs of the two channels. The two sampling switches are represented by impulse train functions, and the AMUX is depicted as two window functions, denoted as $h_{odd}(t)$ and $h_{even}(t)$, each characterized by

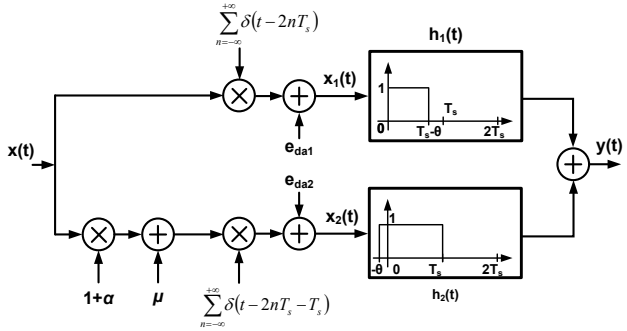


Fig. 21. Systematic model of a 2-time interleaved DAC. Random quantization white noise (e_{da}) is ignored in this paper.

the DCE β. These window functions alternately enable the outputs of the sDACs, $x_{odd}(t)$ and $x_{even}(t)$, which are then superimposed to the output of the TI-DAC.

Since this study primarily examines the effects of 2-channel mismatch, the random quantization noise is not considered. Timing skew, defined as the mismatch in clock signal arrival times between even and odd channels in a TI-DAC, is closely coupled with DCE. While timing skew introduces interleaving spurs, DCE further exacerbates them by disrupting the effective timing balance between channels. With the proposed DCE calibration scheme and clock correction circuit, timing skew is inherently corrected alongside DCE adjustment. Therefore, to simplify the systematic model (Fig. 21), timing skew is not explicitly included. A detailed analysis of timing skew is provided in [24].

The subsequent sections will clarify that harmonics primarily arise from the mismatch, rather than the noise. The input signal, $x(t)$, undergoes time-interleaved sampling and following the introduction of GEM and OSM, the time-domain outputs of the two sDACs are expressed as

$$x_{odd}(t)=x(t)\sum_{h=-\infty}^{+\infty}\delta(t-2nT_s) \tag{8a}$$

$$x_{even}(t)=[\mu+(1+\alpha)x(t)]\sum_{h=-\infty}^{+\infty}\delta(t-2nT_s-T_s) \tag{8b}$$

where the $T_s=1/f_s$ represents the quantization cycle of the TI-DAC. Then, the time-domain output of TI-DAC y(t) is derived by convolving ($\otimes$) the sDAC outputs with their respective window function for selection and then summing them, resulting in

$$y(t)=x_{odd}(t)\otimes h_{odd}(t)+x_{even}(t)\otimes h_{even}(t) \tag{9}$$

in which

$$h_{odd}(t)=\begin{cases}1, & 0\le t\le T_s-2T_s\beta\\ 0, & \text{otherwise}\end{cases} \tag{10a}$$

$$h_{even}(t)=\begin{cases}1, & -\theta\le t\le T_s\\ 0, & \text{otherwise}\end{cases} \tag{10b}$$

(9) can be divided into two parts, $y_s(t)$, which is independent of the input x(t), and $y_d(t)$, which is related to x(t). For ease of analysis, continuous-time Fourier transforms on these two parts will be separately performed and the impact of nonlinearities in the dual-channel system on the SFDR will be examined.

B. Frequency Domain Derivation and Dynamic Parameter Analysis

After taking the Fourier transform and expanding the trigonometric functions of $y_s(t)$ extracted from (8), the time-domain and frequency-domain signals can be represented as

$$y_s(t)=\mu\sum_{n=-\infty}^{+\infty}\delta(t-2nT_s)\otimes h_{even}(t) \tag{11a}$$

$$Y_s(j\omega)=e^{-jk\pi}\mu\left[\sin\left(\frac{k\pi}{2}\right)\cos\left(\frac{\Omega}{2}\right)+\sin\left(\frac{\Omega}{2}\right)\cos\left(\frac{k\pi}{2}\right)\right]\cdot\frac{2}{k}\sum_{k=-\infty}^{+\infty}\delta\left(\omega-k\frac{\omega_s}{2}\right)e^{-j\frac{k\pi-\Omega}{2}} \tag{11b}$$

Where $\Omega=kT_s\beta\omega_s$, Due to the impulse train function $\delta()$, $Y_s(j\omega)$ only has components at frequencies that are integer multiples of $f_s/2$, which are not within the first Nyquist zone and therefore SFDR will not be affected by the noise, which is independent of the input x(t).

The part of (9) that is related to x(t) is extracted as $y_d(t)$, and its frequency domain representation is given as $Y_d(j\omega)$, which can be expressed as

$$y_d(t)=x(t)\cdot\sum_{h=-\infty}^{+\infty}\delta(t-2nT_s)\otimes h_{odd}(t)+(1+\alpha)\cdot x(t)\cdot\sum_{h=-\infty}^{+\infty}\delta(t-2nT_s-T_s)\otimes h_{even}(t) \tag{12a}$$

$$Y_d(j\omega)=\frac{1}{2T_s}\sum_{k=-\infty}^{+\infty}x\left(j\omega-k\frac{\omega_s}{2}\right)\cdot[H_{odd}(j\omega_o)+(1+\alpha)e^{-jk\pi}H_{even}(j\omega_o)] \tag{12b}$$

Within the first Nyquist zone，sinusoidal input signal only have the frequency components of ω_o, thus, $H(j\omega)$ can be replaced by $H(j\omega_o)$. In practice, the output switching duty-cycle for a 2-time interleaved DAC is around 50% with a tiny mismatch. This mismatch is produced by both the imbalanced driving capability of PMOS and NMOS transistors in logic gates, as well as the time delay difference between the two clock pathways. For GSps DAC design, the β before calibration can be practically limited to 3%Ts, collaborated with a duty-cycle stabilizer [43], by properly sizing the ratio of PMOS/NMOS and symmetrizing the clock tree. Therefore, after the trigonometric expansion in (12b), terms containing $2T_s\beta\omega_0$ are further approximated using infinitesimal simplification.

Setting $k=0$ in (11b) and combining it with trigonometric simplification, the frequency-domain function for the fundamental wave can be expressed as

$$Y_{d0}(j\omega)=\frac{(2+\alpha)\pi\delta(\omega-\omega_0)}{2j}e^{-j\frac{\omega_0(T_s-2T_s\beta)}{2}}\cdot\mathrm{sinc}\left(\frac{\omega_o T_s}{2}\right) \tag{13a}$$

which is located at the input frequency $\omega_0/2\pi=f_0$. Setting k=1 in (11b), then the spur is expressed as

$$Y_{d1}(j\omega)=\left|\frac{2\pi\delta\left(\omega-\left(\frac{\omega_s}{2}-\omega_0\right)\right)}{j2T_s\left(\frac{\omega_s}{2}-\omega_0\right)}\right|\cdot\left|(2+\alpha)\sin\left(\frac{\omega_0T_s}{2}\right)\sin\left(\left(\frac{\omega_s}{2}-\omega_0\right)T_s\beta\right)+\alpha\cos\left(\frac{\omega_0T_s}{2}\right)\cos\left(\left(\frac{\omega_s}{2}-\omega_0\right)T_s\beta\right)\right| \tag{13b}$$

This spur is located at $(\omega_s/2-\omega_0)/2\pi$ and is the only interleaving spur within the first Nyquist zone. All other spurs with k values greater than 1 are outside the zone, Therefore, they do not affect the SFDR and are not considered.

Based on (12b), (13a), and (13b), the harmonic distortion within the first Nyquist zone is the ratio of the amplitude of the spur at $\omega_s/2-\omega_0$ to the fundamental at ω_0, which can be expressed as

$$HD_1 = \frac{Y(j\omega)|\omega=\omega_s/2-\omega_0}{Y(j\omega)|\omega=\omega_0} \quad (14)$$

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