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Inelastic-Stress-Induced Threshold Instability and Mobility Degradation in AlN/GaN MIS-HEMTs on Si

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This work investigates the impact of stress-induced effects on the stability of AlN/GaN MIS-HEMTs on Si employing PECVD-SiN as a passivation layer. DC and temperature-dependent *C–V*/*I–V* measurements together with TCAD simulations are used to correlate stress state, defect behavior, and channel transport. As-deposited PECVD-SiN introduces strong inelastic stress that compresses the 2DEG near the GaN surface and drives an anomalous reverse shift of the threshold voltage of ~−0.3 V between 300 and 475 K, with room-temperature mobility limited to ~700 $cm^2 V^{-1} s^{-1}$ by remote scattering. Arrhenius analysis of the drain current yields an activation energy E_a = 0.059 eV, attributed to thermally activated charging and restructuring of bulk and interface defects coupled to the stress field. Post-passivation annealing at 450 °C largely relaxes the inelastic component, broadens the potential well, and reduces E_a to 0.019 eV. The mobility increases to ~1260 $cm^2 V^{-1} s^{-1}$ and exhibits a polar-optical-phonon-like temperature dependence, while the V_{TH}–T behavior changes to a weak positive coefficient. These results offer insights on the temperature stability of stress-induced GaN MIS-HEMTs from a material perspective. [doi:xxx]

GaN-based high electron mobility transistors (HEMTs) on Si offer high electron mobility, high sheet carrier density, and low-cost, large-diameter substrates, and have therefore been widely adopted in RF power applications and compact, high-efficiency RF front ends.[1-4] As requirements on output power density, operating frequency, and integration continue to increase, GaN-on-Si HEMTs are approaching their electrical and thermal limits, so stability under realistic operating conditions has become critical.[5,6] However, these devices still suffer from current collapse, increased dynamic on-resistance, threshold-voltage (V_{TH}) shift, and off-state leakage associated with surface and buffer traps,[7-10] which under high-voltage, high-temperature, and RF operation can severely degrade long-term stability and even cause premature failure in power electronics systems.

To enable both depletion- and enhancement-mode operation on the same GaN-on-Si platform, stress engineering has been used to tune polarization and channel charge for V_{TH} control.[11-13] For example, Li *et al.* used LPCVD-SiN to modify the barrier stress and realized an E-mode device with 1.07 W/mm at V_D=6 V.[11] Wang *et al.* reported that removing *in-situ* SiN relaxes tensile stress in AlN barrier layer, inducing a positive V_{TH} shift and yielding 5.59 W/mm at V_D=25 V.[12] Cui *et al.* also reported that optimizing stress relaxation via an annealing process in InAlN/GaN HEMTs enabled an f_{max} of 270 GHz.[14-15] However, the stability of such stress-induced states has rarely been addressed, even though the metastable nature of the stress field and stress-driven defect reconfiguration can lead to V_{TH} shift, mobility degradation, and leakage variation during long-term operation.[16-18] Hence, this calls for quantitative analysis of the stress imposed by surface films on the barrier, including its components, spatial distribution, and temperature response, in a device-relevant bias and temperature window.

In this work, AlN/GaN MIS-HEMTs on Si with PECVD-SiN passivation are used to clarify the origin of the imposed stress and to separate the roles of elastic and inelastic stress in controlling V_{TH} and the temperature dependence of channel mobility. Temperature-dependent measurements before and after post-passivation annealing (PPA) show that, prior to PPA, inelastic stress stored in PECVD-SiN induces thermally activated

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accumulation of negatively charged defects, causing a reverse V_{TH} shift of ~−0.3 V from 300 to 475 K, a nearly flat μ–T behavior with room-temperature mobility limited to ~700 cm^2 V^{-1} s^{-1} by remote scattering, and an activation energy E_a=0.059 eV. After PPA, the inelastic component is largely released, the room-temperature mobility increases to ~1260 cm^2 V^{-1} s^{-1} with a phonon-limited μ–T trend, and E_a is reduced to 0.019 eV, while V_{TH} develops a weak positive temperature coefficient. These results provide a mechanistic basis for stability assessment of stress-induced GaN MIS-HEMTs and quantitatively link stress state, defect kinetics, and macroscopic transport behavior.

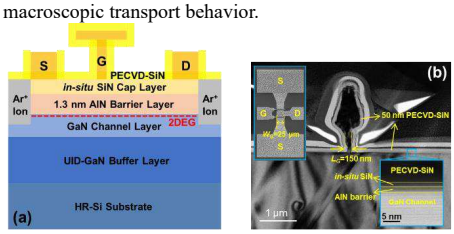

Fig. 1. (a) Schematic cross-section of AlN/GaN HEMTs on Si. (b) Cross-sectional transmission electron microscopy (TEM) image of the gate region of the AlN/GaN MIS-HEMT on Si, inset shows the device layout and the PECVD-SiN / *in-situ* SiN / AlN / GaN epitaxial stack.

Fig. 1(a) shows the device and epitaxial structure. From bottom to top, the stack consists of a 6-inch high-resistivity Si substrate, an unintentionally doped GaN buffer, a 300 nm GaN channel, a 1.3 nm ultrathin AlN barrier, and a ~1.6 nm *in-situ* SiN cap. The *in-situ* SiN serves as a protective cap to maintain the integrity of the ultrathin AlN barrier and functions as the gate dielectric in HEMTs. Non-contact Hall measurements give a sheet resistance (R_s) of 5500 Ω/sq, a sheet carrier density (N_s) of 3.9 × 10^{11} cm^{-2}, and a mobility of 1300 cm^2 V^{-1} s^{-1}. High-resistivity isolation was formed by Ar$^+$ implantation. Ti/Al/Ni/Au ohmic contacts for source and drain were annealed at 775 °C for 30 s in N_2. A T-gate with a 150 nm gate length was defined by electron-beam lithography using a bilayer resist and metallized with Ni/Au. A 50 nm SiN passivation film (refractive index = 2.33) was deposited at 300 °C by PECVD for surface passivation and stress modulation. After passivation, the contact resistance (R_c) was ~0.3 Ω·mm and the R_s was reduced to 462 Ω/sq. To distinguish different stress components, post-passivation annealing (PPA) was carried out on devices with 50 nm PECVD-SiN at 450 °C for 60 s in N_2. Finally, fluorine-based plasma etching was used to open contact windows in the interconnect metal for electrical measurements.

As shown in Fig. 1(b), the cross-section of the AlN/GaN MIS-HEMT on Si was examined by bright-field transmission electron microscopy (BF-TEM). The 50 nm SiN passivation layer uniformly covers the T-shaped gate and access regions. The source–gate spacing L_{SG} and gate-drain spacing L_{GD} are 1.1 μm and 1.75 μm, respectively; the gate length is 150 nm and the source–drain spacing L_{SD} is 3 μm. As indicated in the upper-left inset, the total gate width W_G is 2 × 25 μm. The lower-right inset, acquired in high-angle annular dark-field (HAADF) mode, clearly resolves the ~1.6 nm *in-situ* SiN cap and the ~1.3 nm ultrathin AlN barrier at the AlN/GaN interface.

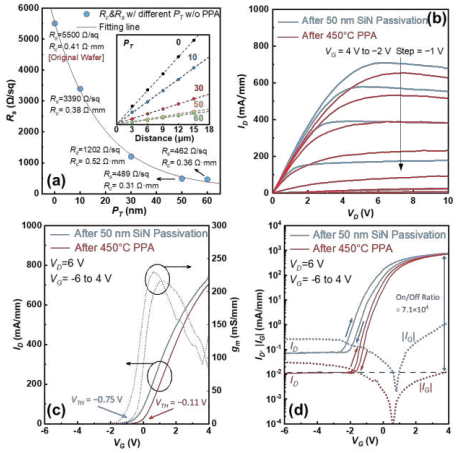

Fig. 2. (a) TLM-extracted R_c and R_s versus P_T (inset shows the TLM plot and fitting). (b) Output curves for devices after 50 nm PECVD-SiN and after PPA. (c) Linear-scale transfer curves with dashed transconductance. (d) Semi-log double-sweep transfer curves with dashed $|I_G|$.

Fig. 2(a) shows the R_s and R_c extracted by transmission line model (TLM) for different SiN passivation thicknesses (P_T). Under identical annealing conditions, R_s decreases from 5500 Ω/sq at P_T = 0 nm to 462 Ω/sq at P_T = 60 nm. This trend suggests that the thickness-induced tensile stress introduced by PECVD-SiN increases rapidly at small P_T and then gradually saturates as P_T further increases, and the resulting enhancement in piezoelectric polarization is mainly responsible for the reduced R_s. The inset TLM fit indicates a stable R_c.

Fig. 2(b) compares the output characteristics of AlN/GaN MIS-HEMTs with a 50 nm PECVD-SiN passivation layer before and after PPA at 450 °C, with V_G swept from 4 to −2 V in steps of −1 V. The maximum drain current ($I_{D,max}$) decreases from 711 mA/mm before PPA to 656 mA/mm after PPA.

Fig. 2(c) shows the transfer characteristics on a linear scale. Before PPA, the device exhibits

transconductance ($G_{m,max}$) of 230 mS/mm and V_{TH} of −0.75 V. After PPA, the dc performance is slightly degraded: $I_{D,max}$ is reduced, $G_{m,max}$ decreases to 216 mS/mm, and V_{TH} shifts positively to −0.11 V. Fig. 2(d) shows the transfer curves on a semi-logarithmic scale. After PPA, the on/off ratio reaches 7×10^4. The off-state drain leakage $I_{D,leak}$ is reduced from 7×10^{-2} to 1.1×10^{-2} mA/mm, and the gate leakage $I_{G,leak}$ decreases from 2.6×10^{-1} to 2.9×10^{-2} mA/mm. The change in hysteresis indicates that PPA relaxes part of the PECVD-SiN-induced stress and lowers the channel carrier density, leading to a reduced saturation current, while improved SiN densification and bonding to the *in-situ* SiN cap suppress interface traps and surface leakage, thereby reducing off-state leakage currents.

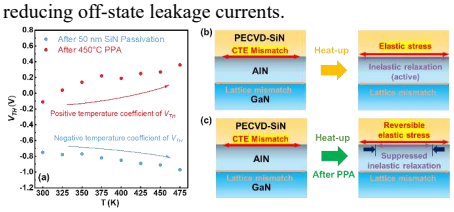

Fig. 3. (a) V_{TH}-T curves (300 to 475 K, 25 K step) after 50 nm PECVD-SiN and after 450 °C PPA. (b) Before PPA, CTE mismatch includes elastic stress and active inelastic relaxation. (c) After PPA, most inelastic stress is pre-released, leaving mainly elastic stress during heating.

Fig. 3(a) compares the V_{TH}–T behavior of devices with 50 nm PECVD-SiN passivation before and after PPA at 450 °C. Before PPA, V_{TH} exhibits a negative temperature coefficient, shifting from −0.75 V at 300 K to −0.98 V at 475 K. After PPA, V_{TH} shows a positive temperature coefficient, shifting from −0.10 V at 300 K to 0.35 V at 475 K.

Fig. 3(b) and 3(c) shows the stress mechanisms governing the shift in V_{TH}. Following SiN passivation, tensile stress is imposed on the AlN barrier through both the lattice mismatch at the AlN/GaN interface and the thermal-expansion mismatch at the PECVD-SiN/AlN interface. The lattice-mismatch stress is set at the AlN growth temperature and is therefore largely locked in, so only a weak dependence on subsequent thermal steps up to 450 °C is expected. A similarly stabilized stress state is associated with the *in-situ* SiN because it is formed at high MOCVD temperature, and appreciable changes before and after annealing are not anticipated. By contrast, the CTE-related stress is established between the PECVD deposition temperature of about 300 °C and room temperature, and a stronger temperature sensitivity is therefore introduced. Reversible elastic stress is accompanied by a metastable inelastic component that is enabled by internal stress relaxation and defect rearrangement within PECVD SiN. Before PPA, substantial inelastic relaxation can be activated upon heating, and an anomalous negative temperature shift V_{TH} is consequently produced. After PPA, most inelastic relaxation has been pre-released, so the temperature response is governed primarily by reversible elastic stress and a slower, approximately linear positive shift of V_{TH} is obtained. Consistent behavior is revealed by Raman spectroscopy of the AlN E_2 mode. A peak at 656.58 cm^{-1} is observed without the *in-situ* SiN, a red shift to 654.36 cm^{-1} is induced by 50 nm PECVD SiN, and a tensile stress of 655 MPa. After 450 °C PPA, a blue shift to 654.88 cm^{-1} is measured, giving 501 MPa, which is consistent with reduced $I_{D,max}$ and improved stability.

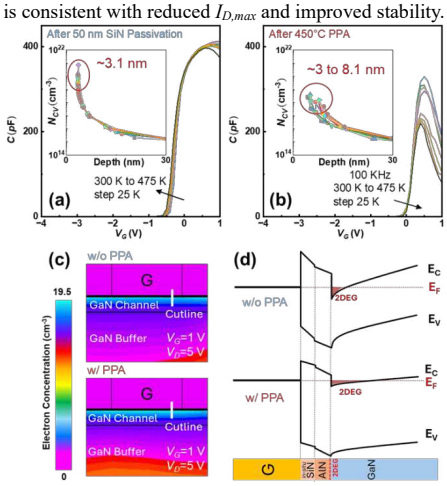

Fig. 4. (a), (b) Temperature-dependent C–V characteristics and N_{CV} evolution of AlN/GaN MIS-HEMTs on Si after 50 nm PECVD-SiN passivation and after PPA, respectively. (c) The electron concentration at bias conditions V_G= 1 V, V_D=5 V, obtained by TCAD simulation. (d) Corresponding band diagram along the cutline in (c).

Fig. 4(a) and 4(b) show temperature-dependent C–V measurements on C–V ring structures before and after PPA, with V_G swept from −4 to 1 V and the temperature increased from 300 to 475 K in steps of 25 K. Before PPA, the devices exhibit a reverse shift of V_{TH} with temperature (negative temperature coefficient), whereas after PPA V_{TH} recovers a positive temperature coefficient. The insets in Fig. 4(a)–(b) depict the vertical potential profile and 2DEG distribution under the gate. Before PPA, when inelastic stress is still stored in the PECVD-SiN layer, the high-density electron gas is compressed into a narrow region located ~3.1 nm below the gate. After PPA, the depth of the 2DEG is shifted from ~3 nm to ~8.1 nm into the GaN channel layer.

As shown in Fig. 4(c)–4(d), Silvaco TCAD was used to analyze the on-state devices before and after PPA

at V_G=1 V and V_D=5 V. After deposition of the 50 nm SiN passivation, the channel electrons are strongly confined near the GaN surface, and the band diagram along the cutline reveals a shallow, narrow quantum well pinned by the combined effect of strong localized stress and charged defects. In this state, inelastic stress in the PECVD-SiN is stored in the form of bulk defects and H-related bonds and is released upon heating through bond reconfiguration and defect charging, reflecting its metastable nature. After 450 °C PPA, most of the inelastic stress is pre-relaxed and the AlN barrier is mainly subjected to reversible elastic stress. The calculated band profile then shows a significantly broadened potential well under the gate, with electrons below the Fermi level extending deeper into the GaN. These results indicate that inelastic stress is strongly coupled to the metastable reconstruction of bulk defects, H-related bonds, and charged defect states inside the SiN layer.

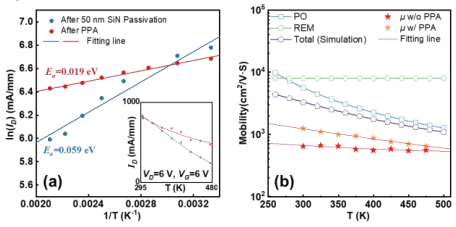

Fig. 5. (a) Arrhenius analysis of drain current E_a energies before/after PPA. (b) Temperature-dependent mobility decomposed into polar-optical-phonon and remote scattering components with total mobility comparison.

Fig. 5(a) shows the temperature dependence of I_D extracted at V_D=6 V and V_G=6 V for devices before and after PPA over 300 to 475 K (25 K step), as sketched in the inset. The drain current decreases with temperature in both cases, but the pre-PPA device shows a much steeper reduction. This behavior is attributed to inelastic stress stored in the PECVD-SiN as metastable bulk defects and H-related configurations. During heating, thermally activated defect charging and structural rearrangement modulate both the channel sheet density $n_s(T)$ and the gate overdrive $V_{OV}(T) = V_G(T) - V_{\mathrm{TH}}(T)$. By analogy with an Arrhenius-type relation,[19] the temperature dependence of I_D is described by:

$$I_D(T) \propto n_s(T)\mu(T)V_{OV}(T) \approx I_0 \exp\left(-\frac{E_a}{k_B T}\right) \quad (1)$$

where I_0 is a weakly temperature-dependent prefactor, E_a is the activation energy, and k_B is the Boltzmann constant. Rearranging Eq. (1) yields Eq. (2) :

$$E_a = -k_B T \ln\left(\frac{I_D(T)}{I_0}\right) \quad (2)$$

from which the activation energies in Fig. 5(a) are obtained, representing the effective barrier for defect charging and stress relaxation. Before PPA, E_a=0.059 eV, inelastic stress drives the thermal activation of a large number of negatively charged defects that deplete the 2DEG, so that $n_s(T)$ decreases and $I_D(T)$ drops rapidly despite a modest increase in gate overdrive. After PPA, most inelastic stress is released and the defect landscape becomes more stable; $I_D(T)$ is then mainly governed by polarization-related changes, giving a smaller E_a=0.019 eV and a much slower decrease of current with temperature.

As shown in Fig. 5(b), the contributions of polar optical phonon scattering (PO) and remote scattering (REM) to the mobility were extracted, and the total mobility was obtained from $1/\mu_{\mathrm{total}} = 1/\mu_{\mathrm{PO}} + 1/\mu_{\mathrm{REM}}$.[20] Before PPA, the mobility remains nearly constant at ~700 cm^2 V^{-1} s^{-1} over the measured temperature range, indicating that remote Coulomb scattering from inelastic-stress-induced bulk/interface defects dominates. After PPA, the room-temperature mobility increases to 1260 cm^2 V^{-1} s^{-1} and decreases with temperature in a trend closer to PO-limited behavior, consistent with a weakened REM contribution. In the framework of Eq. (1), the pre-PPA device operates with a persistently low $\mu(T)$ controlled by REM, so the temperature dependence of $I_D(T)$ is dominated by the inelastic-stress-driven evolution of $n_s(T)$ and the suppressed mobility, leading to the larger extracted E_a. After PPA, intrinsic scattering processes dominate the reduction of $I_D(T)$ with temperature.

In conclusion, this study demonstrates that inelastic stress plays a dominant role in the anomalous V_{TH} shift and mobility degradation. Before PPA, inelastic stress stored in the PECVD-SiN layer drives the ultrathin-barrier AlN/GaN MIS-HEMTs on Si into a region characterized by an activation energy E_a=0.059 eV, a reverse V_{TH} shift of about −0.3 V over 300 to 475 K, and a room-temperature mobility of only 700 cm^2 V^{-1} s^{-1} limited by remote scattering (REM). After PPA, E_a is reduced to 0.019 eV, the room-temperature mobility increases to 1260 cm^2 V^{-1} s^{-1} the μ–T behavior becomes polar optical phonon-limited, and V_{TH} exhibits a weak positive temperature dependency. These results provide a mechanistic basis for stability assessment of stress-engineered GaN MIS-HEMTs.

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