28.5 A 0.6V/0.9V 26.6-to-119.3μW ΔΣ-Based Bio-Impedance Readout IC with 101.9dB SNR and <0.1Hz 1/f Corner

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Bio-impedance (BioZ) is an important physiological parameter in wearable healthcare sensing. Besides the inherent cardiac and respiratory information, BioZ can be also used for other emerging applications such as non-invasive blood status sensing [1]. A conventional 4-electrode (4E) setup eliminates the effect of electrode-tissue impedance (ETI) at the expense of user comfort, system complexity, and cost. On the other hand, a 2-electrode (2E) setup avoids short-falls of 4E but can only capture relative changes of BioZ instead of its absolute value. In addition, a readout front-end (RFE) with wide dynamic range (DR) and high signal-to-noise ratio (SNR) is needed to deal with small BioZ variation (0.1~10Ω) as well as large baseline resistance (>10kΩ). A conventional RFE architecture employing an instrumentation amplifier (IA) and ADC has to trade-off between resolution, DR and noise [2,3]. Although flicker noise in the current generator (CG) is mitigated through dynamic element matching (DEM) [2], the reference current (IREF) noise issue remains unaddressed. In [5], digital-assisted baseline cancellation and IREF correlated noise cancellation are proposed, which help eliminate IREF noise and input-dependent noise [4] due to the large signal in the current-balance instrumentation amplifier (CBIA). Nevertheless, larger noise is still observed due to the finite residual current (I_{res}) from the baseline cancellation.

This paper presents a BioZ measurement architecture with the following key features. (1) A ΔΣ-based BioZ RFE, which provides 1st-order noise shaping. Compared to [5], it achieves smaller area and power by eliminating the SAR-ADC. (2) With a Gm-C integrator, 1b quantizer, and digital loop filter (DLF), the feedback IDAC can closely track the input signal and result in smaller I_{res}. Therefore, a smaller non-linear effect in the trans-conductance (TC) stage is induced with smaller input-dependent noise. Similar to [5], DEM and IREF correlated noise cancellation are adopted. The overall system sensitivity is only limited by the thermal noise. (3) Clocked-averaging DEMs are employed in IDAC, CG, and IREF to modulate the flicker noise to high frequency, greatly improving the noise performance. This circuit achieves 101.9dB SNR within a 4Hz BW, <0.1Hz 1/f noise corner, and low power.

Figure 28.5.1 shows the overall block diagram of the proposed circuit. CG generates a differential square wave current with tunable amplitude (5 to 100μA_{pk}) and frequency (f_{CG}) of 1 kHz to 1 MHz. The current is injected to the body and the resulting differential voltage is measured by RFE. The input is filtered by a high-pass filter (HPF) to remove the DC offset. Then, it is pre-modulated to in-(I) and quadrature-(Q) phase components at the chopping frequency (f_{chop}). Each component is processed by the RFE that consists of a TC stage, a Gm-C integrator, a 1b quantizer, a DLF, and a feedback IDAC. This architecture exhibits 1st-order noise shaping, which leads to wider DR and higher SNR. The TC stage is used here because it can provide a high common-mode rejection ratio (CMRR) and power optimization. By separating the TC stage and the Gm-C integrator, power consumption can be optimized according to the noise requirement. The TC output current is subtracted by the feedback IDAC to create an I_{res}, which is integrated by the Gm-C integrator. This contrasts with [5], where a trans-impedance (TI) amplifier is used, and the achievable residual is ultimately limited by the TI gain. The integrator output voltage is then quantized by a clocked comparator. If the 1b output is employed to directly control the IDAC, its coarse output resolution eliminates the zero I_{res} advantage provided by the Gm-C integrator. Hence, DLF is employed to produce finer IDAC control. With all these techniques combined, the IDAC is able to closely track the input and generate near zero I_{res} at steady state, which effectively eliminates the non-linear effect that induces the input-dependent noise within the TC stage.

Figure 28.5.2 shows the schematic of the key building blocks. In the TC stage, the main noise source is the input differential pair. Hence, most power budget except for CG block is allocated to TC, whereas the Gm-C integrator can be optimized for power efficiency. To achieve this, the current mirror gain between TC and Gm-C stage is set smaller than unity (k=1/4). To lower the noise, a few techniques are adopted. First, chopper stabilization is employed to reduce the 1/f noise of the TC stage and the Gm-C integrator. Second, three DEMs are employed for the IDAC, CG, and IREF to mitigate the mismatch of current sources as well as reducing 1/f noise. Finally, correlated noise current cancellation [5] is adopted by using the same IREF for CG and IDAC. As the TC generates output current related to CG while IDAC tries to track and compensate the TC output current, their correlated noise current output tends to cancel each other and results in lower noise. With a 1b quantizer output, the IDAC output tracks the TC output through a high-switching square wave, leading to large residual between the two. To tackle the issue, an IIR-based DLF with infinite DC loop gain is implemented, so that IDAC can track the resulting waveforms closely with much smaller I_{res}.

Figure 28.5.3 shows the DEM scheme for CG, IREF, and IDAC. One notable difference compared to [5] is the high switching frequency used in the IDAC to mitigate the flicker noise. To minimize the static current in the IDAC, a single-ended IDAC is used [6]. However, the IDAC output fluctuation increases the number of switching DEM elements in one conversion period. This makes the IDAC more susceptible to high-frequency switching noise, deteriorating noise and linearity. Due to the slow-changing BioZ signal and small value parameters (α and β in Fig. 28.5.2) in the DLF, the IDAC output variation is minimized to keep the number of DEM switching elements close to constant, and in turn reduce the switching noise [6]. Furthermore, the DEM algorithm for the IDAC is improved over [6] to further reduce the flicker noise of the diode-connected transistors (M_{p_I}/M_{n_I}, M_{p_Q}/M_{n_Q} for I-and Q-phase) and cascoded transistors.

This circuit is fabricated in 40nm CMOS and occupies an active area of 0.6mm^2. The RFE consumes 8.8 to 16μW from 0.1 to 100mV_{pk} (2E case), and 17.8 to 103.3μW from the CG (I_{CG}=5 to 100μA_{pk}) under 0.9V supply. The digital part consumes 453nW under a 0.6V supply. Figure 28.5.4 shows the measured noise spectrum, which clearly exhibits 1st-order noise shaping with very low flicker noise corner frequency. The effectiveness of DEMs on CG and IREF for 1/f noise mitigation is observed. It also indicates that applying DEM on the IDAC, including diode-connected $M_{P\_I,Q}/M_{N\_I,Q}$, helps to reduce noise the most. The noise density for 20Ω at 100μA is 52.5nV/sqrt(Hz) at 1Hz, translating to 0.52mΩ/sqrt(Hz). With 2kΩ at 50μA, the noise density is 149nV/sqrt(Hz) at 1Hz, translating to 2.9mΩ/sqrt(Hz). One striking observation is the flatness of the measured noise spectrum, indicating the effectiveness of the proposed techniques with near-zero residual in eliminating the flicker noise. Figure 28.5.5 shows the results using 2E (gel) for respiration and 4E (gel) for heartbeat test with electrodes attached to chest, clear BioZ variations are observed. The measured SNR and R_{rms} with BioZ in the range of 20Ω to 20kΩ is shown and compared with [5]. It can be observed that the proposed design achieves better R_{rms} and better SNR in the range above 100Ω and 600Ω, respectively. The measured chip performance is summarized and compared with prior arts in Fig. 28.5.6. This design achieves the smallest power consumption and area while attaining the highest SNR among designs in the table. The achieved SNR_{max} and FoM are >6dB and >9dB better than prior arts, respectively. Figure 28.5.7 shows the chip micrograph.

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References:
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[4] H. Ha et al., "Measurement and Analysis of Input-Signal Dependent Flicker Noise Modulation in Chopper Stabilized Instrumentational Amplifier," *SSCL*, vol. 1, no. 4, pp. 90-93, Apr. 2018.
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[6] H. Son et al., "A Low-Power Wide Dynamic-Range Current Readout Circuit for Ion-Sensitive FET Sensors," *TBioCAS*, vol. 11, no. 3, pp. 523-533, June 2017.

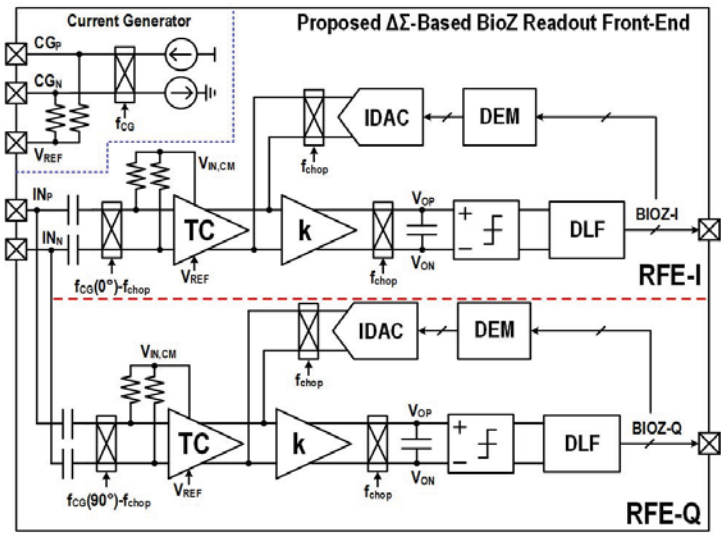

Figure 28.5.1: System overview of I/Q channel for the ΔΣ-based BioZ readout front-end.

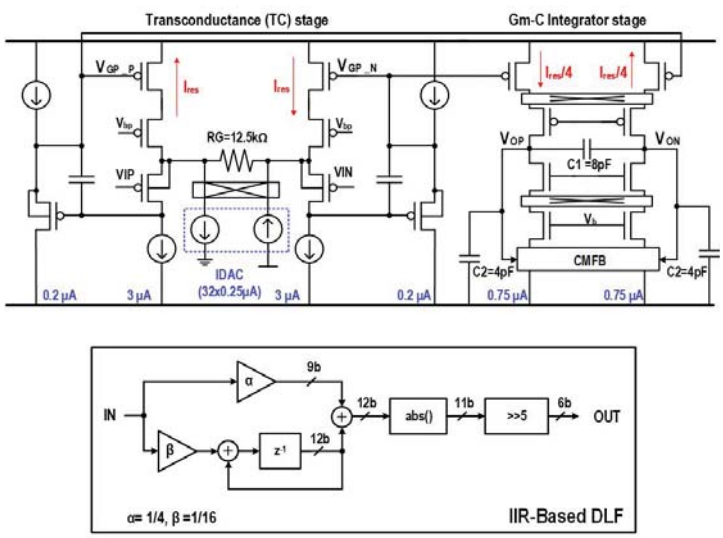

Figure 28.5.2: Detailed implementation of TC and Gm-C integrator, and IIR-based DLF.

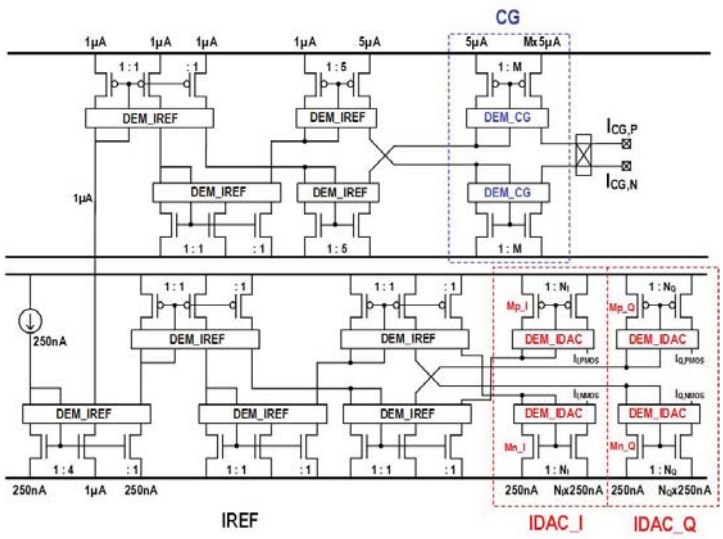

Figure 28.5.3: Scheme of DEMs for CG, IREF, and IDAC. DEM_IDAC includes diode-connected transistors (Mp_I,Q/Mn_I,Q, respectively).

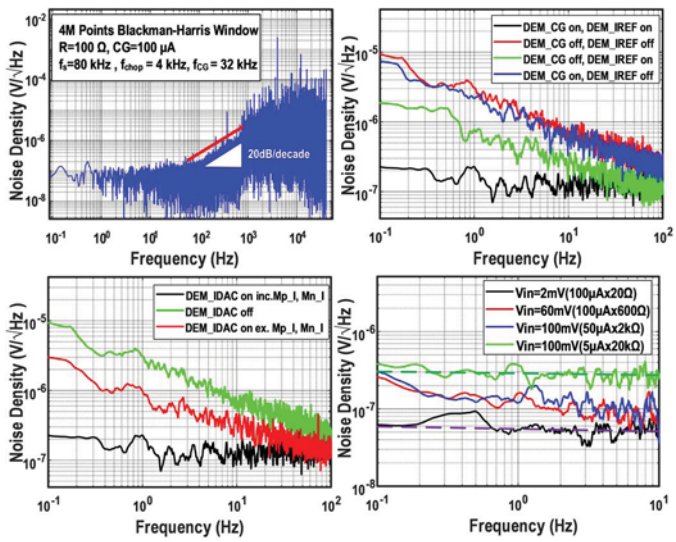

Figure 28.5.4: Measured noise spectrum; noise comparisons (for CG=15μA, R=6kΩ) with and w/o DEMs in CG, IREF, and IDAC; noise spectrum for various input signals.

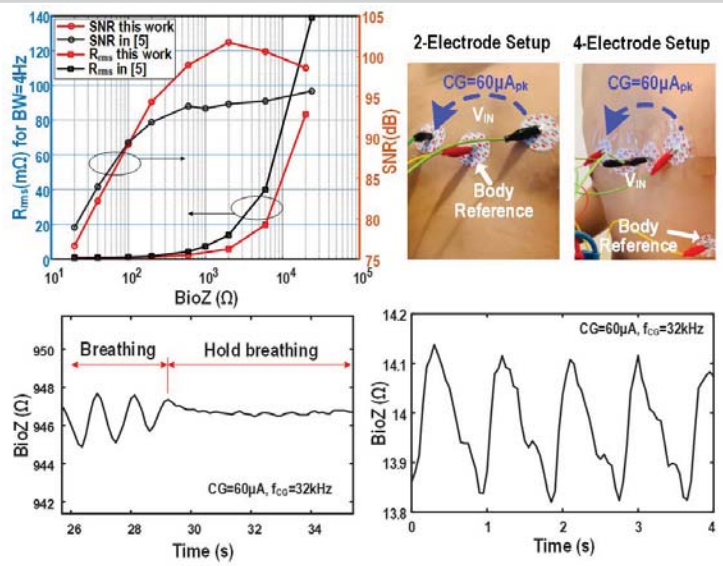

Figure 28.5.5: Measured SNR and R_{rms} with BioZ from 20Ω to 20kΩ. In-vivo experiments with 2E and 4E for respiration and heartbeat monitor.

Parameters	VLSI'17 [2]	JSSC'18 [3]	JSSC'19 [5]	MAX30001	ADS1292R	This work
Tech. (μm)	0.18	0.13	0.055	N/A	N/A	**0.04**
Supply (V)	1.2/1.8	1.5/3.5	1.2	N/A	N/A	**0.9/0.6**
Stimulation signal	Square (I)	Pseudo-sine (I)	Square (I)	Square (I)	Square (V)	**Square (I)**
Input range (kΩ)	1	10	24	5.625	10	**20**
Current magintude (μA_{pk})	5~100	5~50	5~100	8~96	0~100	**5~100**
Current frequency (kHz)	1~1024	4~100	1~1024	0.125~131	32~64	**1-1024**
Noise Density Rn @ 1Hz (mΩ/sqrt(Hz))	1.1 (R=20Ω) 26 (R=1kΩ)	0.7 (R<50Ω) 9.5 (R=2kΩ)	0.4 (R=40Ω,100μA_{pk}) 7 (R=2kΩ,60μA_{pk})	40[a] (R=680Ω)	40[a] (R=2kΩ)	**0.52 (R=20Ω,100μA_{pk}) 2.9 (R=2kΩ,50μA_{pk})**
SNR_{max}(dB)[b] (BW=4 Hz)	76.6	91.4	95.7	78.6	87.9	**101.9**
Power (μW) of Readout	18.7	89[d]	18.9 ~34.9	N/A	N/A	**8.8~16**
Power (μW) of CG	54~229	56~95	31~154.7	N/A	N/A	**17.8 ~ 103.3**
Power (μW)	72.7~247.7	145~184	49.9~189.6	320	335	**26.6~119.3**
Area (mm^2)	0.88	0.96	0.74	N/A	N/A	**0.6**
FoM (dB)[c]	124.5	135.6	143.5	119.6	128.6	**152.6**

[a] Peak-to-peak value [b] SNRmax=max(R/Rrms) where Rrms=Rn*√BW or Rpp/√2
[c] FoM= SNRmax+10*log(BW/Power) where power is the sum of max. in readout and min. in CG

Figure 28.5.6: Chip summary and benchmark with the state of the art.

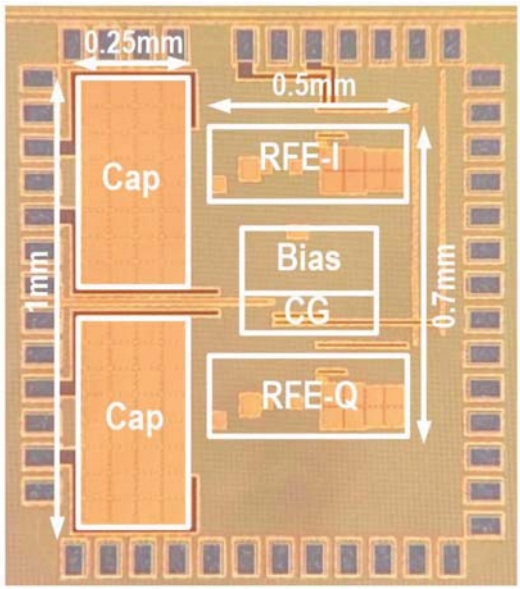

Figure 28.5.7: Die photo.