High-Performance Amplifier Package Design for Heterogenous Integration on Si-interposer

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***Abstract*—The RF design for the wire bond and flip-chip Power Amplifier (PA) MMIC on the High Resistivity (HiR) Si-interposer are presented in this paper. The HiR Si-interposer is to support multiple off-the-shelf RF and Baseband ICs for complex advanced RF frontend modules using heterogeneous integration. A two-sided thermal cooling solution is adopted for this high-performance integration architecture. The high-power dissipation MMIC is integrated using flip-chip assembly so that the heat can be dissipated through the top heat spreader. For the other ICs, they are integrated using wire bond assembly so that their heat will be dissipated through the bottom HiR Si-interposer.**

Keywords—Heterogenous Integration, Power Amplifier integration, Si-interposer, RF frontend, System-in-Package

I. Introduction

The growing demand for wireless applications such as 5G/6G, Advanced Radar, and Satellite Communication has increased the packaging complexity, the operating bandwidth, and the RF output power level for the RF frontend modules. The packaging of this RF frontend modules challenge is compounded by the demand for package miniaturisation and the increases in integration density. In modern Radar and Software Defined Radio designs, advanced CMOS processor chip is integrated into the RF frontend module to support multifunction signal processing.

The RF frontend consists of RF Compound semiconductor MMIC and Digital/Baseband CMOS IC. These high-performance circuits require an effective thermal solution. Currently, there are several high-power dissipation RF packaging developments which have shown promising results [1]-[5]. Most of their solutions are to integrate the high-power dissipation chip inside the through cavity of the Si substrate so that the heat can be transferred to the heat spreader below. In this Heterogenous Integration (HI) development, a two thermal path solution is proposed to provide for different ICs in the RF frontend package. The two-sided thermal solution has a top heat spreader for flip-chip IC and a bottom PCB metal plane through the HiR Si-interposer for wire bond IC as shown in Figure 1. The high-power dissipation ICs such as the RF PA and the Field Programmable Gate Array (FPGA) will be assembled using flip-chip integration so that their heat dissipated will be conducted via the heat spreader and to the external thermal solution. The heat spreader is also used as a metal casing to protect the IC inside the package from external environmental effects. For the lower power dissipation RF chip, they will be assembled using wire bonds so that their heat will be conducted through the HiR Si-interposer and to the thermal Via and metal plane in the PCB substrate. In this way, two thermal solutions can be realized for the 2.5D HiR-Si interposer package to enhance the RF performances.

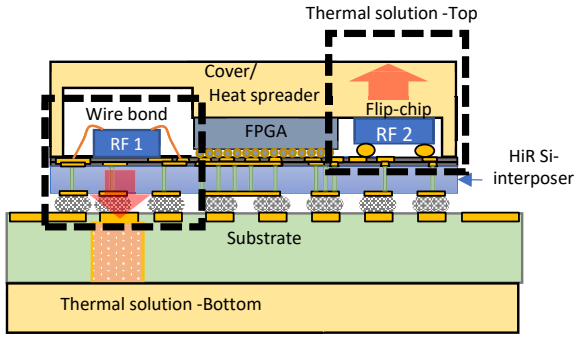

Figure 1: Si-interposer RF frontend module design with two-sided thermal solution

In the high-performance RF frontend module, PA packaging is the most demanding integration design, especially at high frequencies. The increase in RF output power level increases the power dissipation and requires an efficient thermal management solution without affecting the RF performance. The current focus of this development is PA integration on HiR Si-interposer using Commercial Off-the-shelf (COTS) chips. The same PA MMIC is used for the development of both the wire bond and flip-chip integration designs for the two-sided thermal solution. In the actual implementation, other chip such as LNA or Mixer MMIC will be integrated using wire bond assembly instead.

II. Heterogenous Integration Design

The substrate for the HI platform needs to provide both lateral and vertical low-loss signal routing with a good impedance match for the RF integration. In addition, passive circuits including inductors and capacitors are also required. For Digital circuits, the CMOS processor chip has a pin count of more than 1000 which requires high-density routing. Hence, the substrate will also need to provide a high-density signal line with linewidth spacing of 2µm or less for the digital

circuit integration. Finally, the substrate also needs to have low thermal resistance for the heat dissipation generated by the chips.

Table 1 shows the material properties of some of the common substrates extracted from [6]. Low-Temperature Co-fired Ceramic (LTCC) is widely used in moderate power level RF circuit packaging due to its low loss tangent (tanδ) and acceptable thermal conductivity. But for advanced RF frontend module which requires additional Digital circuit integration, its line width/spacing of around 75µm to 50µm is not sufficient. Glass substrate has the best tanδ and it can be processed at wafer level to give fine line width/spacing of 2µm. However, it has a poor thermal conductivity which limits its application in high-power RF circuit integration. Laminate substrate R03010 has good tanδ, and the circuit is fabricated using the cost-effective panel-level process. However, it also suffers from low thermal conductivity and is unable to give the fine line width spacing required for high-density I/Os integration.

Table 1: Substrate Material properties

Material	ε_r @10GHz	10^{-4} tanδ @10GHz	Surface roughness (µm)	Thermal conductivity (W/m.K)
LTCC	7.8	15	0.22	30
Glass	4-7	1	0.025	0.8-1.2
HiR-Si	11.9	10-100	<0.001	100-150
SiC	10.8	20	<0.001	120-200
RO3010	10.2	35	-	0.66

Silicon Carbide (SiC) has the best thermal conductivity with good tanδ, but the fabrication technology is not mature. In addition, the 8" or 12" High Resistivity (HiR) wafer size required for interposer is not readily available. HiR Si has a low tanδ in the range of 0.0010 to 0.01 at 10GHz and a high thermal conductivity of 100-150 W/m.K. HiR Si 12" wafer is widely available, and the fabrication process is matured due to the advanced development of the Back-End-Of-Line (BEOL). It is not only able to provide fine line width/spacing of less than 2µm, but it can also provide the Through Silicon Via (TSV) diameter of 10µm [7]. Hence, Hi-R Si is a good substrate for high-performance circuit integration.

A. Thermal Design and Analysis

For the thermal analysis, a COTS PA is simulated in both wire bond and flip-chip configurations on the HiR Si-interposer to compare the thermal performance. The PA used in this evaluation is a GaN-on-SiC wide band amplifier MMIC which has DC blocking capacitors on both RF ports and are matched to 50 ohms. It can provide > 2W of saturated output power achieving ~23% power-added efficiency. The dimensions of the PA die are 2.75 x 2.75 x 0.10mm.

For the wire-bond PA design, its backside is attached to the Si-interposer and then connected to the substrate through solder balls, as shown in Figure 1 – RF1. The PCB is populated with through Via and metal planes connected to a cool plate in the simulation. For the flip-chip PA design, a Copper heat spreader is attached directly to the backside of the PA, as shown in Figure 1–RF2. The simulation model details can be found in [6]. The preliminary thermal performance of a PA simulated under 50% Pulse mode and Continuous Wave (CW) operating conditions are shown in Figure 2. As the flip-chip design has a lower thermal resistance path, the temperature of the PA is lower compared to the wire-bond PA. In the 50% Pulse mode, with a maximum (Max) power dissipation of 6.45W, the temperature of the wire bond PA is ~181°C while the flip-chip PA is ~143°C. In the CW mode, with a Max power dissipation of 12.9W, the temperature of the wire bond PA is ~293°C while the flip-chip PA is ~221°C.

The result shows that the flip-chip design with a direct heat spreader design has a better thermal performance and hence it will be used for high-power dissipation chips in the package. The wire bond with Si-interposer design has lower cooling efficiency and it will be used for the lower power dissipation ICs. The separation of thermal path design can also be used to minimise thermal crosstalk for those temperature-sensitive chips.

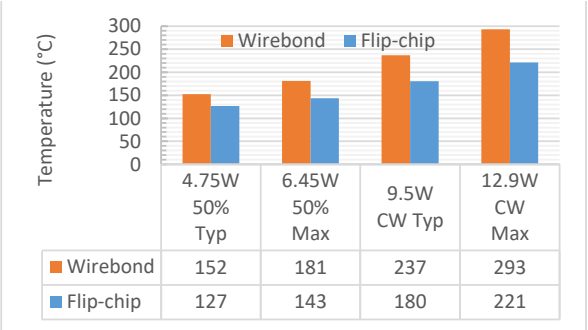

Figure 2: Simulated thermal performance of the same chip in wire-bond (RF1) and flip-chip (RF2) assembly on the same module design.

B. RF Design and Analysis – Wire bond

The RF performance of the wire bond and the flip-chip designs are evaluated using the same COTS PA MMIC on a simplified HiR Si-interposer test vehicle to reduce the evaluation time. The stack-up of this simplified HiR Si-interposer is shown in Figure 3, it consists of 2 metal layers, the 1st metal layer (M1) is 1µm thick while the 2nd metal layer is 2µm thick. The RF interconnect is used for the RF signal routing and hence a thicker metal is preferred to minimise the resistance. UBM is also deposited on M2 for the flip-chip and wire-bond assembly. The test vehicle design is such that the RF signal can be measured directly on the top surface and no TSV is required.

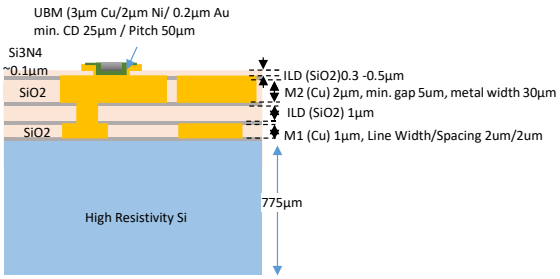

Figure 3: HiR-Si interposer stack-up design for the test vehicle

The design of the COTS PA MMIC is meant for wire bonding integration to a PCB 50Ω microstrip transmission line. However, for this HiR Si-interposer integration design, a CPW transmission line is used instead as there is no TSV and backside metal plane for the Ground (Gnd). For the actual full functional package design in which a TSV interposer will be

used, the CPWG design will be used as it has better isolation performance. The pad design of the COTS PA MMIC is shown in Figure 4. The RF IN and RF OUT are on opposite sides, and they have a pad dimension of ~180 x 90µm which is good for multi-wire bonding. In the datasheet, the RF Gnd pads besides the RF I/Os are not wire bonds during integration. These Gnd pads are probably used for on-wafer-level testing during production. For all III-V RF MMIC designs, the backside of the chip is the Gnd plane. Typically, it is connected directly to the Microstrip transmission line Gnd plane and the DC power supply Gnd during packaging or integration.

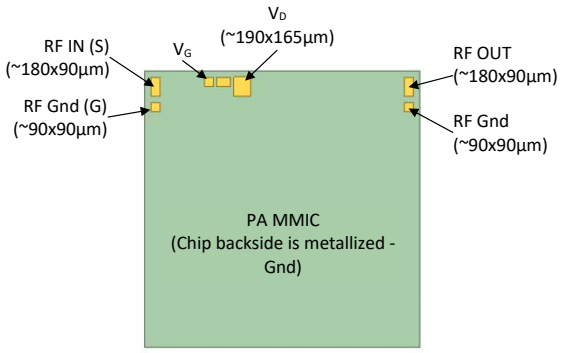

Figure 4: PA MMIC I/Os pads design

The design of the wire bond PA on the HiR Si-interposer is shown in Figure 5. The direct distance between the interposer and chip pads is designed at 410µm. This is based on the internal wire bond and the die-attached process tolerances. Generally, it is preferred to have a minimum gap for the best RF interconnect performance. Besides the RF signal line being wire bonded to the HiR Si-interposer, the additional Gnd pad beside the RF I/O pad in the chip is also wire bonded to the CPW Gnd as shown in Figure 5. The design of the CPW for both RF IN and RF OUT is the same. It has a signal width of 50µm, a spacing of 30µm, and a length of 2mm. The CPW design allows the standard GSG RF probe to measure directly on the HiR Si-interposer.

In order to reduce the inductance of the wire bond, a multi-wire bond design is used. The simulated performance of different wire bond configurations is shown in Figure 6. Standard gold wire of 1 mil diameter is used for the wire bond. The results show that the 3 signal wire bond (x3 Signal) design has the best Return Loss (RL) response followed by the 2 signal plus 1 Gnd wire bond (x2 Signal x1 Gnd). However, there is no significant difference in their Insertion Loss (IL) of ~0.36dB up to ~25GHz. The 2-signal wire bond (x2 Signal) has the worst RL and IL of -19dB and ~0.42dB, respectively. From these simulation results and the limitation of the wire bonding machine, the x2 Signal with x1 Gnd wire bond design is used. However, in the full functional package design, 3 signals plus 1 Gnd should be used to improve the reliability performance. For simplicity design, the biasing capacitors and the resistor are designed on the PCB instead and are connected from the HiR Si-interposer using a wire bond again, as shown in Figure 12.

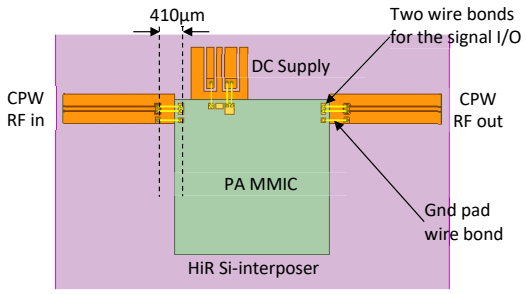

Figure 5: Simulation model for wire bond PA MMIC integration design on HiR Si-interposer

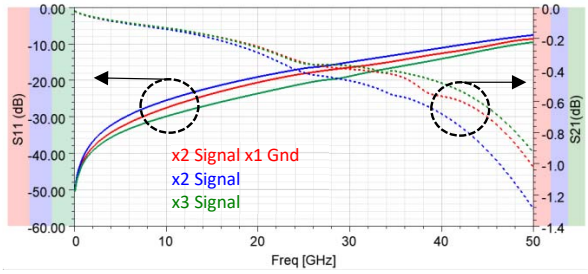

Figure 6: Simulated frequency response of various wire bond design

C. RF Design and Analysis – Flip-chip

For COTS MMIC, especially III-V chips, they are designed with the top surface of the active area as air, which has a dielectric constant (D_k) of 1 and a very low loss tangent. These MMICs are designed for wire bond assembly which has a face-up integration, as shown in Figure 12. However, for the proposed flip-chip assembly, the chip will be face-down. The material above the active area is now silicon or substrate material, which has a D_k of >1. Hence, the MMIC performance will be deteriorated due to this loading effect. If there is a metal plane or circuit immediately on the surface, the effect will be more severe. The impact can be minimized by increasing the gap between the active area and the interposer. The gap is set by the micro-bump height.

A simplify flip-chip assembly model as shown in Figure 7 is used to analyse the effect of the dielectric loading effect. For III-V chip, Microstrip transmission line is usually used for the circuit design. A 50ohms Microstrip transmission line of 70μm width and 1mm length is designed on the MMIC chip. The chip is 0.1mm thick and the backside of the chip is grounded. The simulated Return Loss (RL) of the idea assembly is as shown in Figure 8. The MMIC Microstrip line without the HiR Si-interposer has a RL of ~-42dB for frequency up to 20GHz. Next, the HiR Si-interposer without metal plane is then modeled below the MMIC. The gap between the MMIC and the HiR Si-interposer is set to the micro-bump (µBump) height of 40µm, 60µm, and 80µm. The RL drops to -32dB, -36dB, and -38dB, respectively for frequencies up to 20GHz. The RL is affected by the HiR Si-interposer proximity, and a bigger height is preferred. However, due to process challenges, the targeted micro-bump height is set to between 60 to 80µm for this flip-chip assembly.

The impact of a metal plane on the HiR Si-interposer on the flip-chip MMIC is also simulated. For a metal plane on top (F_Gnd) of the HiR Si-interposer, and the micro-bump height of 60µm, the RL drops to less than 20dB for frequencies up to 20GHz. For the metal plane on the backside (B_Gnd) of the HiR Si-interposer, with the same micro-bump height of 60µm, the effect is much less severe, and the RL drops to less than -29dB for frequency up to 20GHz. Hence, the HiR Si-interposer design should avoid designing a metal plane directly below the MMIC.

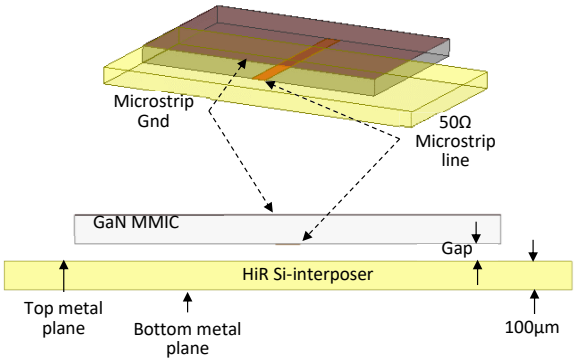

Figure 7: Flip-chip simulation model for assembly height (Gap) analysis

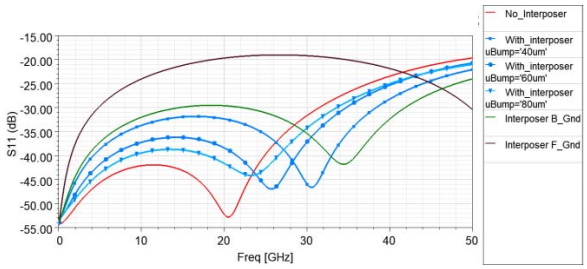

Figure 8: Return Loss (S11) of the flip-chip assembly on HiR Si-interposer with height Gap (uBump), and additional metal (Gnd) plane on the interposer.

The PA MMIC is flip-chip integrated using the CPW transmission line circuit which is the same as the wire bond design. Figure 9 shows the simulated response of the 3 possible types of flip-chip transition designs, that is Ground Signal Ground (GSG), Ground Signal (GS), and Signal (S). The result shows that both GS and S designs have a dip in the frequency response at around 35GHz but not the GSG design. The dip occurs outside the operating frequencies range of the PA. In addition, the RF I/Os of the PA MMIC design have only a Signal (S) and Gnd (G) pad, hence the GS CPW transition is used.

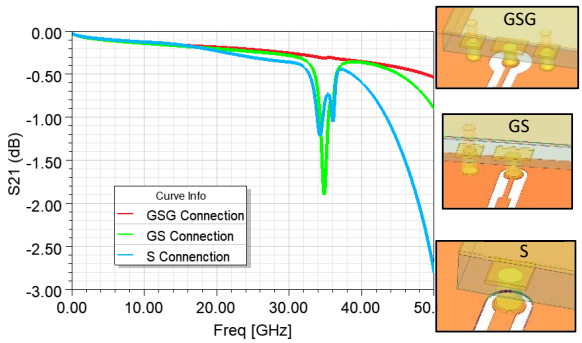

Figure 9: MMIC RF I/Os transition to HiR Si-interposer CPW

The design of the flip-chip PA MMIC on the HiR Si-interposer is shown in Figure 10. The GS flip-chip transition includes an impedance tunning section on the CPW transmission line. The simulated result of the full package shows that there is a small resonance at about 31GHz. The resonance frequency is also affected by the size of the MMIC, the resonance frequency reduces when the size of the MMIC increases. For this design, the resonance frequency is still outside the PA operating frequencies of up to 20GHz.

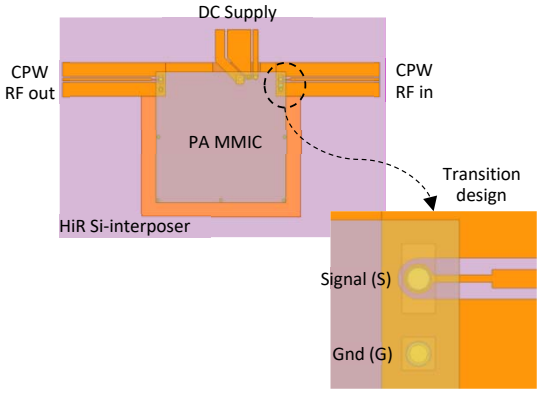

Figure 10: Simulation model for flip-chip PA MMIC integration design on HiR Si-interposer

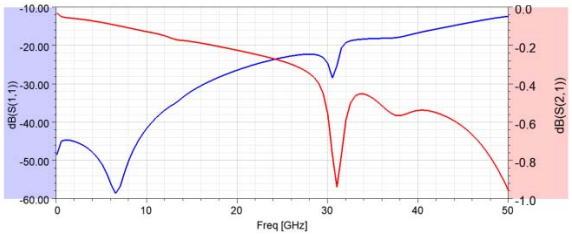

Figure 11: Simulated IL (S21) and RL (S11) of the flip-chip interconnect from the HiR Si-interposer CPW to MMIC PA Signal pad

III. Measurement

The PA MMIC assembly and the measurement setup are shown in Figure 12. The PA MMIC is first attached to the HiR Si-interposer using solder preform. Next, the PA MMIC I/Os are wire bonded to the HiR Si-interposer using 1mil Gold wire. The wire bond connection of the RF I/O (S) consists of

2 wires and the Drain voltage (V_D) consists of 4 wires. The HiR Si-interposer with the wire-bonded PA MMIC is then assembled on the PCB using conductive epoxy. The PCB has a cavity for the HiR Si-interposer to sit inside so the external wire bond length of the DC supply can be minimized. The RF signals are then measured directly on the HiR Si-interposer CPW transmission line using the standard GSG wafer probe connected to the measurement test equipment.

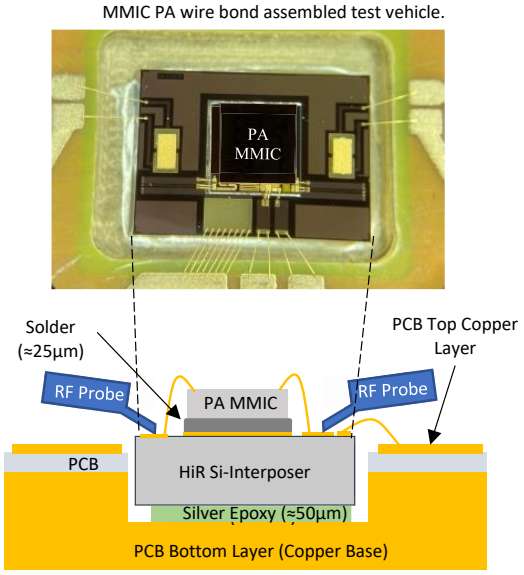

Figure 12: Wire bond PA top view and test setup

The measured small signal responses of assembled wire bond design sample (A1) with an RF input power of 0dBm are shown in Figure 13. The samples are placed on a metal chuck during the measurement. The measured result shows that the gain is lower than 25dB at the lower frequencies range when compared with the datasheet results at room temperature. A possible cause could be heating up of the chip due to lack of temperature control.

The measured large signal response of 3 samples (A1, A2 and A3) with an RF input power of 18dBm at room temperature is shown in Figure 14. The result shown are close to the datasheet response. From the measured results, A2 has the lowest output power. Comparing the three samples, A2 has the greatest assembly variation. The chip is slightly shifted during die attachment and caused a tilted wire bond profile.

Currently, the measurement with temperature monitoring is ongoing and will be presented in future. Nevertheless, the measurement results of the 3 samples have a similar response profile as the datasheet without abnormality. This shows that the wire bond circuit integration of the PA on the HiR Si-interposer using CPW transmission line is feasible.

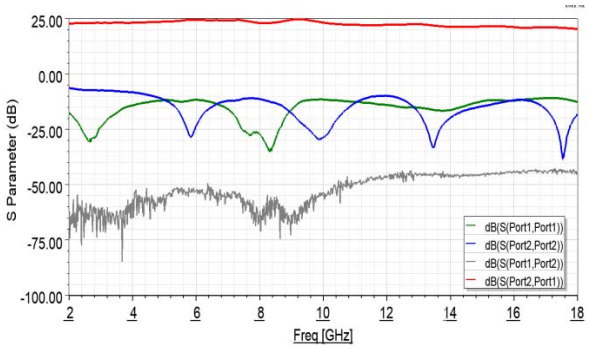

Figure 13: Measured small signal wire bond PA in HiR Si interposer response for sample A1.

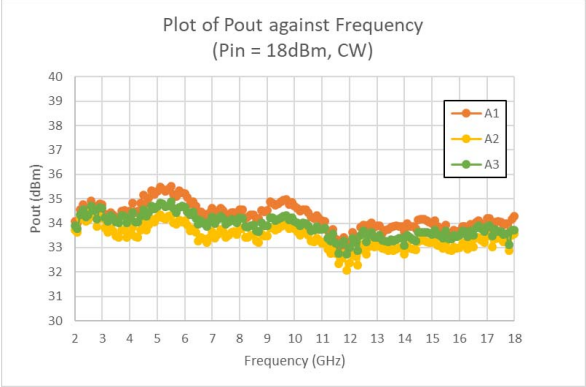

Figure 14: Measured Large signal measurement result.

The PA MMIC flip-chip assembly on the HiR Si-interposer is still progress. Gold (Au) stud bumping are first made on the I/Os pad of the PA MMIC. Solder balls are then placed on the Au stud using solder jetting process. The PA MMIC is then flip-chip assembled on the HiR Si-interposer. Figure 15 shows flip-chip assembly of the dummy MMIC on the HiR Si-interposer. The X-ray picture shows the RF I/O and the RF GND are not shorted and they are using single stud bump. For the V_D connections, 4 Au stud bumps are made, and they are shorted together by the solder ball. The V_G and the supply Gnd are also connected using single Au stud bump due to the limited pad size. The side view picture shows that the gap between PA MMIC and the HiR Si-interposer is around 73µm as shown in Figure 16.

Unfortunately, the assembly of the actual MMIC PA cannot proceed as schedule and is not ready for measurement at the time of manuscript submission due to equipment breakdown. The measurement result of the is during flip-chip PA together with the assembly process detail will be presented in future.

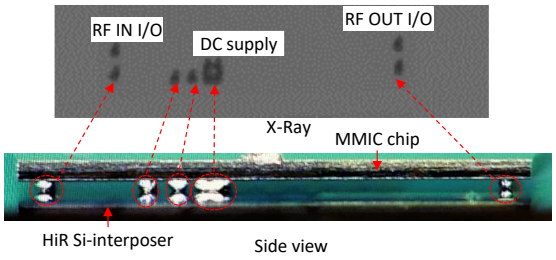

Figure 15: X-ray and side view of the flip-chip assembly of the MMIC on HiR Si-interposer

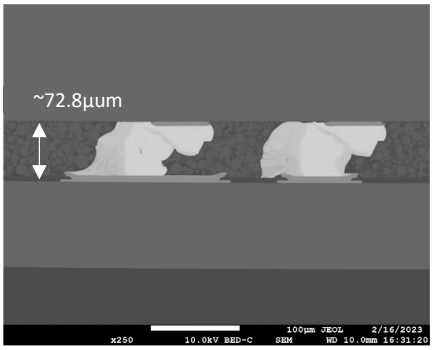

Figure 16: Cross section of the Au stud joint

IV. CONCLUSION

A HiR Si-interposer for complex multi-chip RF frontend with two-sided thermal solution is proposed. The integration designs are evaluated using COTS PA MMIC in this paper. The HiR Si-interposer is used to provide both low-loss RF connection and good thermal conduction. The ICs are integrated using both wire bond and flip-chip assemblies. The low-power dissipation chips are wire bond and uses HiR Si-interposer as the heat spreader. The high-power dissipation chips are flip-chip assembled so that the backside of the ICs are connected to the metal casing which act as a heat spreader to provide higher efficiency thermal solution.

The preliminary measurement result of the COTS PA MMIC integrated using wire bond to the CPW circuit on HiR Si-interposer shows similar RF response profile as the manufacturer datasheet. The flip-chip PA design assembly is in progress and the measurement result will be presented when ready.

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