Effects of SiO_2 Hard Masks on Si Nanophotonic Waveguide Loss for Photonic Device Integration

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***Abstract*— As the basic building block for photonic device integration, silicon nanophotonic waveguide requires low-loss propagation for high-performance ultra-compact photonic device. We experimentally study silicon dioxide hard masks grown by two different methods, i.e., thermal oxidation and plasma-enhanced chemical vapor deposition for silicon nano-waveguides fabrication and their effects on the propagation loss. It is found that the denser and smoother quality of thermally grown silicon dioxide increases the etch selectivity against silicon and reduces the line edge roughness transferred to the silicon nano-waveguide sidewalls, hence resulting in a lower loss as compared to the plasma-enhanced chemical vapor deposition silicon dioxide hard mask. With thermally grown silicon dioxide as a hard mask, the silicon nano-waveguides loss can be halved for a 650 nm wide nano-waveguide, and the loss is comparable to a waveguide fabricated with a resist etch mask.**

***Index Terms*—dielectric materials, optical waveguides, loss measurement**

I. Introduction

RECENT development of silicon (Si) integrated photonics has the capability of sub-micron light confinement for dense photonic integration and enables the multi-functional photonic system on chip combining III-V semiconductor devices on-top via wafer-bonding [1-3]. As the basic building block of the photonic system on chip technology, the Si nanophotonic waveguide requires low-loss propagation for high-performance ultra-compact photonic devices. The formation of the Si waveguide through etching two trenches is preferred [4-5] over the direct negative resist approach [6-7] so that most of the Si material is still left on the substrate for bonding purpose.

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As Si waveguides cross-sectional dimensions reduce towards sub-microns, maintaining its propagation loss at 1-2 dB/cm becomes challenging [8]. To reduce the Si nanophotonic waveguide loss, advanced patterning technology [5] such as 193 nm immersion lithography has been used. Many post-fabrication techniques have also been used, such as thermal oxidation [9-12], laser annealing [13], etchless process [14] and wet chemical clean [15-16], as the fabricated waveguide without any post-processing exhibits a high loss due to the side-wall roughness. A recent use of hydrogen silsesquioxane (HSQ) resist [6] as a direct mask for low-loss Si waveguides is not suitable for wafer-bonding for III-V semiconductor device integration as: (1) a good bonding quality requires a large area of Si at the passive device region to serve as a sturdy platform for bonding. Negative mask like HSQ does not form the platform for bonding as most of the Si areas will be removed after etching; (2) the high temperature plasma from inductively-coupled plasma (ICP) etching will burn the resist hard mask, resulting in stubborn residues of resist staying on the Si surface after etching. This will greatly reduce the bonding quality. Hence, a hard etch mask is required to fabricate Si nano-waveguide for applications towards heterogeneous III-V on Si integration.

Researchers have also investigated the different factors in the fabrication that will affect the propagation loss of silicon nanophotonic waveguides, such as the writing strategies of electron beam lithography [17] and the covering material like amorphous titanium dioxide [18]. However, so far, there has been no study on the material quality of the hard mask used and its effect on Si waveguides loss performance. In this letter, we experimentally study the influence of two types of silicon dioxide (SiO_2) hard masks, i.e. grown by thermal oxidation and plasma-enhanced chemical vapor deposition (PECVD) on the performance of Si nano-waveguides propagation loss. The results show that Si nano-waveguides fabricated using thermally oxidized SiO_2 hard masks give a lower propagation loss as compared to those using PECVD SiO_2 hard masks. For a 650 nm wide Si nano-waveguide, propagation loss is halved when thermally grown SiO_2 is used as a hard mask. This is because thermally grown SiO_2 is denser than PECVD SiO_2 and hence will provide a higher selectivity which results in less line edge roughness transferred to the Si sidewalls during etching.

II. EXPERIMENTAL DETAILS

The substrate used is 6-inch silicon-on-insulator (SOI, Soitec) wafers with a 340 nm thick Si layer and a 2 μm thick buried oxide. The top Si layers of these substrates are thinned down to 300 nm using wet thermal oxidation at 1000°C.

Thermal oxidation passes steam or oxygen (O_2) at high temperature through a furnace with the SOI wafers in it. Thermally grown SiO_2 formed when Si surface reacts with O_2 at high temperature. This reaction will cause the SOI layer to thin down as the Si layer becomes thermally grown SiO_2. For every 100 nm thick thermally grown SiO_2, 40 nm thick Si will be required. The 6-inch SOI wafers are subsequently diced into 24 mm × 24 mm square samples and these samples are divided into two batches. The first batch uses the 100 nm thick thermally grown SiO_2 directly as a hard mask for Si nano-waveguide fabrication. The second batch undergoes 3 minutes of diluted hydrofluoric (HF) acid dip to completely remove the thermally grown SiO_2. These samples then go through an organic solvent ultrasonic clean before the 100nm PECVD SiO_2 growth.

Both batches of samples with 100 nm thick thermally grown and PECVD SiO_2 are then spin coated with poly(methyl-methacrylate) (PMMA, A5 950K) at 3000 rpm for 90 seconds to give a 300 nm thick resist. This is followed by a hot plate soft-bake at 170°C for 15 minutes. The Si nano-waveguide patterns are written by electron beam lithography (EBL, Elionix) at 100kV, 1 nA current with dose ranging from 1000 μC/cm^2 to 1200 μC/cm^2. To ensure optimal dose for each type of hard mask, a dose test is done and the dosage chosen is at the point when it comes out of under-dosage. As thermally grown SiO_2 are denser in quality than PECVD SiO_2, it requires higher dose during the EBL writing to ensure that the nano-waveguides sidewalls are not roughened because of under-dosage. After EBL, the nano-waveguides patterns, which are two 1μm wide trenches are developed by methyl-isobutyl-ketone:isopropyl-alcohol (MIBK:IPA)=1:3 for 70s. These patterns are then transferred down to the SiO_2 hard mask using a CHF_3/Ar based Reactive Ion Etching (RIE). As compared to PECVD SiO_2, the denser thermally grown SiO_2 requires around twice the etching time to etch through the SiO_2 layer to the Si layer below. The selectivity of PMMA to PECVD SiO_2 is 1:1 and of PMMA to thermal SiO_2 is 2:1. After the SiO_2 hard mask etch, the remaining PMMA on the SiO_2 hard mask is removed by an organic clean followed by a 3-minute O_2 plasma. The Si nano-waveguides are then formed after ICP etch of around 300 nm thick SOI, leaving a thin layer of SOI on the buried oxide (BOX). This etch process uses a HBr/Cl_2 based chemistry to get an anisotropy sidewall profile. After etching, the samples are lapped down to around a thickness of 200 μm for cleaving before measuring their optical propagation loss.

III. RESULTS AND DISCUSSION

Fig. 1 shows (a) the top-view and (b) oblique angle Scanning Electron Microscopy (SEM) image of the Si nano-waveguide fabricated after SOI ICP etch. Inset in Fig. 1(a) shows the light spot from the Si nano-waveguide. PMMA forms the waveguide patterns by using EBL to define 1 μm trenches next to the waveguide areas. Minimum SOI surfaces are exposed to etching and majority of the unetched SOI areas form a sturdy platform for good bonding.

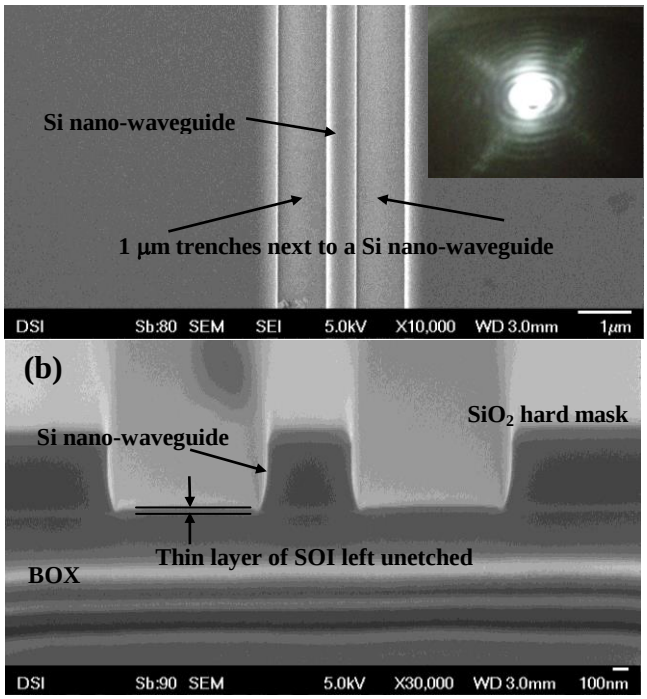

Fig. 1(a) Top-view and (b) Cross-sectional SEM images of a Si nano-waveguide fabricated using PMMA as the ebeam resist to define the SiO_2 etch mask before transferring the pattern onto the SOI using ICP etch. Inset shows the light spot from the Si nano-waveguide.

Propagation loss of a waveguide can be characterized through spectrum measurement of the Fabry-Perot cavity formed by the waveguide and the two facets, which is $\alpha L = \ln\left(\left(\frac{1-\sqrt{\eta}}{1+\sqrt{\eta}}\right)\frac{1}{\sqrt{R_1 R_2}}\right)$, where α is the loss coefficient, L is the length of the waveguide, R_1 and R_2 are the respective reflectance at the two facets, and η is the ratio between the minimal and maximal intensities measured. For the silicon nano-waveguide, one concern is the poor coupling efficiency if we directly apply this method. Therefore, we use a set of waveguides with varying nano-waveguide length to extract the loss coefficient carefully. Fig. 2 shows the design to obtain optical propagation loss of the nano-waveguides. All waveguides are around 4 mm long after cleaving and the micro-waveguides at both ends have a width 4 μm to allow a higher coupling of light into the waveguide. The micro-waveguides are tapered into nano-waveguide along a tapered length of 200 μm. Neglecting the loss of micro-waveguide (which is much smaller as compared to the nano-waveguide), the loss coefficient α_n of nano-waveguide can be obtained from the slope of the fitting line based on the

equation $\ln\left(\left(\frac{1-\sqrt{\eta}}{1+\sqrt{\eta}}\right)\right) = \alpha_n l + \ln\left(\sqrt{R_1 R_2}\right)$, where l is the length of nano-waveguide section. Different from the conventional cut-back method (output power versus length), the present approach does not require the same coupling efficiency for different waveguides.

In the measurement, the wavelength used is around 1550 nm and polarization of light is transverse electric (TE) mode. Although some nano-waveguides e.g., with a width of 650 nm is not a single mode, only the fundamental mode is mainly excited when coupling the light from the objective lens to the micro-waveguide. This can be verified through the detected Guassian beam as shown in the inset of Fig.1a.

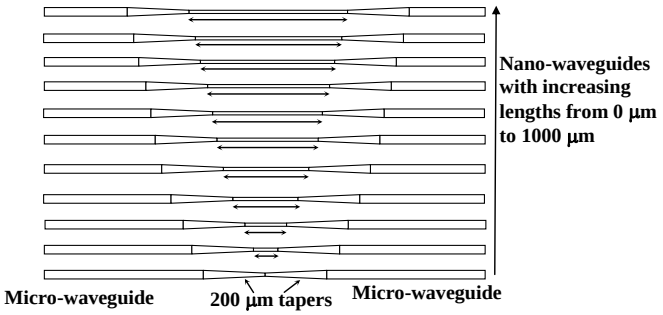

Fig. 2 Design of the Si nano-waveguide fabricated with 4 μm micro-waveguides at both ends tapered to the nano-waveguides with varied lengths from 0 μm to 1000 μm.

Fig. 3 compares the propagation loss measured for Si nano-waveguides using PECVD SiO_2 and thermally grown SiO_2 respectively with increasing lengths of the nano-waveguides at waveguide width of 650 nm.

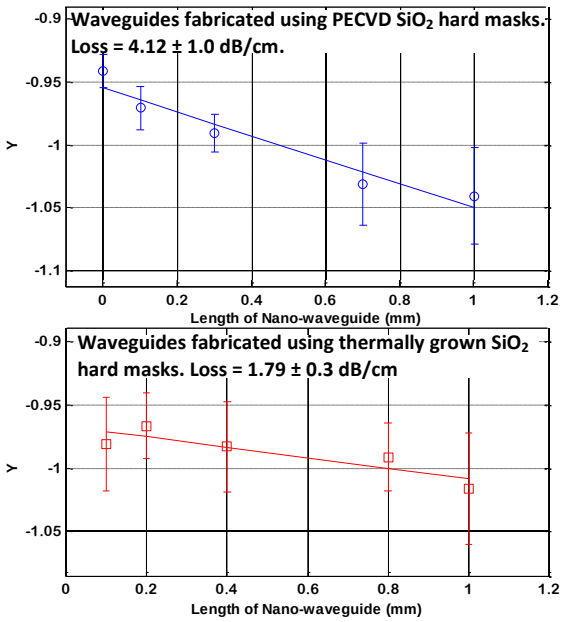

Fig. 3 Plots of Si nano-waveguide loss as the nano-waveguide length increases for waveguide width of 650 nm for both PECVD SiO_2 and thermally grown SiO_2 as hard masks respectively.

Vertical axis: $Y = \ln\left(\frac{1-\sqrt{\eta}}{1+\sqrt{\eta}}\right)$; $\eta = \frac{Power_{min}}{Power_{max}}$

The propagation loss of nano-waveguides fabricated using PECVD SiO_2 as hard mask exhibits a steeper slope compared to those using thermally grown SiO_2. The steeper is the slope, the higher is the propagation loss. The Si nano-waveguides fabricated using thermally grown SiO_2 have a gentler slope, hence a lower propagation loss.

Table 1 shows the summary of propagation loss measured for 550 nm, 650 nm and 700 nm wide Si nano-waveguides using PECVD and thermally grown SiO_2 as hard masks.

The Si nano-waveguides fabricated using thermally grown SiO_2 as an etch mask gives a lower propagation loss, as low as 1.79 dB/cm as compared to those fabricated using PECVD SiO_2 etch masks. As thermally grown SiO_2 are denser than PECVD SiO_2, as evident from the longer time required to etch through the thermally grown SiO_2, it has better selectivity to Si. During Si etch, the denser thermally grown SiO_2 gives a selectivity of ~ 1:20 to Si compared to PECVD SiO_2 to Si (~ 1:5). For every unit of thermally grown SiO_2 etched, Si is etched 4 times more compared to that of PECVD SiO_2. Hence the amount of line edge roughness transferred down from the SiO_2 sidewalls to the Si sidewalls is reduced, resulting in a better sidewall roughness and a lower propagation loss.

TABLE I
SUMMARY OF SI NANO-WAVEGUIDES PROPAGATION LOSS (DB/CM)

Si Nano-waveguides width (nm)	PECVD SiO_2 (300 μm^2 EBL chip size)	Thermally grown SiO_2 (300 μm^2 EBL chip size)
550	6.34 ± 0.1	3.87 ± 0.5
650	4.12 ± 1.0	1.79 ± 0.3
700	3.08 ± 0.6	1.05 ± 0.4

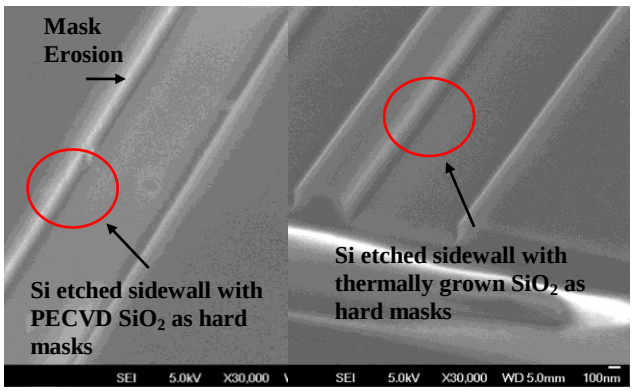

Fig. 4 SEM images of the samples tilted at 45 degrees showing the etched Si sidewall using PECVD SiO_2 and thermally grown SiO_2 as the hard mask.

Fig. 4 shows 45 degrees tilted angle SEM images taken showing the sidewall of the etched Si using PECVD SiO_2 and thermally grown SiO_2 as hard masks. From the image contrast, it seems that the sidewall of the etched Si with PECVD SiO_2 as a hard mask is brighter than that using thermally grown SiO_2. This means that there are more unevenness and hence increased roughness for the sidewall using PECVD SiO_2 as a hard mask. In addition, it can be seen that for the sample using PECVD SiO_2 as a hard mask, there is some mask erosion

occurring at the mask edge. This means that the selectivity for PECVD SiO_2 is lower compared to thermally grown SiO_2, hence resulting in mask erosion on the edge of the mask. Mask erosion signifies more line edge roughness being transferred to the etch Si sidewall during etching and hence a rougher sidewall compared to using thermally grown SiO_2 as a hard mask.

Defects and voids in the SiO_2 hardmasks can also play a part in contributing to the propagation loss. Park et. al. [19] showed that defects and voids in thermally grown SiO_2 and PECVD SiO_2 are negligible, hence this factor is comparable for both type of hard masks in our work.

The actual widths of the fabricated Si nano-waveguides using the two different types of hard masks are also characterized using the SEM. Table II shows the actual widths compared to the designed widths. The actual widths of the nano-waveguides using PECVD SiO_2 as hard mask are 10 – 20 nm wider than design, while those using thermally grown SiO_2 as hard mask are around 1 nm wider. The difference in dimensions for the two actual widths is not significant enough to be the dominating factor to cause a drastic difference in the nano-waveguide propagation loss.

TABLE II
SI NANO-WAVEGUIDES ACTUAL WIDTHS (NM)

Si Nano-waveguides designed width	Si Nano-waveguides actual width with PECVD SiO_2 as hard masks	Si Nano-waveguides actual width with thermally grown SiO_2 as hard masks
550	573.8	551.3
650	665.7	650.6
700	710.6	701.3

IV. CONCLUSION

We have characterized SOI nano-waveguide loss using thermally grown SiO_2 and PECVD SiO_2 as etch hard masks. The SOI nano-waveguides fabricated using thermally grown SiO_2 as etch hard masks give a lower loss compared to that using PECVD SiO_2 as etch hard masks. The propagation loss measured for a 650 nm wide SOI nano-waveguide fabricated using thermally grown SiO_2 as a hard mask can be halved when compared to that fabricated using PECVD SiO_2 hard masks. The propagation loss measured is 1.79 dB/cm, comparable to nano-waveguides fabricated using direct resist masks. The lower propagation loss from thermally grown SiO_2 hard masks will enable applications for III-V semiconductor heterogeneous integration, towards enhanced performance in multifunctional photonic system on chip with sub-micron light confinement.

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