# Co-design for Low Warpage and High Reliability in Advanced Package with TSV-Free Interposer (TFI)

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***Abstract*—TSV-Free Interposer (TFI) technology eliminates TSV fabrication and reduces manufacturing and material cost. Co-design modelling methodology is established for TFI technology with considering wafer process, package assembly and package/board level reliability and thermal performance to optimize structure design, wafer process, assembly process and material selection. Experimental results are used for validating warpage modelling results. Through wafer level modelling, suitable carrier wafer and EMC materials are recommended to control wafer warpage less than 2mm. Effects of package substrate coefficient of thermal expansion (CTE) and stiffener on assembly induced package warpage are simulated to reduce package warpage. The recommended materials and geometry design based on reliability are aligned with that from wafer and package warpage simulation results. The final test vehicle (TV) design and material selection are determined based on co-design modelling results for achieving successful TFI wafer process and package assembly process and long term package/board level reliability.**

*Keywords-co-design modelling; finite element analysis; solder joint reliability; TFI technology; TSV-free interposer; warpage*

## I. INTRODUCTION

Through-silicon interposer (TSI) is a successful application of through-silicon via (TSV) technology [1-3]. The TSI technology realizes the heterogeneous integration of ICs and vias offer vertical connection from the chips with fine pitch I/Os to the substrate with medium pitch I/Os [3]. However, TSV fabrication is facing many challenges, such as void-free filled Cu TSV and low Cu protrusion [4-6], bonding/debonding process [7], thin wafer handling and wafer warpage control [8,9], and long-term reliability of TSVs [10,11]. TSI is not a cost effective technology due to wafer processes, material cost, and yield loss. New technologies have being explored to provide the similar function as TSI interposer but without TSV formation. Different terminologies are used for such technologies, such as Silicon-Less Interconnection Technology (SLIT) [12], Non-TSV Interposer (NTI) [13], Silicon-Less Integrated Module (SLIM) technology [14]. In our previous study, package using SLIT technology results in the comparable solder joint reliability and package warpage compared to TSI technology [15]. In this paper, we call this technology as TSV-Free Interposer (TFI) technology. In TFI technology, the back-end-of-line (BEOL) layers are formed based on a Si/glass carrier, followed by chip-to-wafer bonding, wafer level compression molding, carrier wafer (Si/glass substrate) removal, solder ball attachment and singulation. Therefore, TFI technology eliminates TSV fabrication and reduces manufacturing and material cost.

TFI technology still faces several challenges needed to be addressed, such as wafer warpage during wafer fabrication process, assembly induced package warpage, and package/board level solder joint reliability etc. [12,13]. Finite element analysis (FEA) is a powerful and useful tool and has been widely used in the packaging design stage for virtual prototyping [8,9,15]. Co-design methodology with FEA simulation has been established and applied for TFI technology to optimize structure design, wafer process, assembly process and material selection. Co-design methodology for TFI technology includes TFI wafer process simulation for reducing wafer warpage, TFI package assembly process simulation to minimize package warpage, package level temperature cycling (TC) simulation to improve C4 solder joint reliability, board level temperature cycling (TCOB) simulation to improve board level solder joint reliability, and thermal simulation to evaluate thermal performance of TFI package. Through co-design simulation, cost effective and successful wafer and assembly processes and reliable and high performance package solution can be achieved for the advanced package with a TFI interposer.

## II. TEST VEHICLE DESIGN AND FABRICATION PROCESS

Fig. 1 shows process flow of TFI package test vehicle (TV) fabrication. TFI interposer with 3 levels of 0.4μm/0.4μm fine line/space redistribution layer (RDL) is first fabricated on Si or glass carrier wafer using BEOL process. One 15mm × 15mm larger chip which is supposed to be a Graphics Processing Unit (GPU), and two 5.5mm × 7mm × 0.49mm smaller chips which are supposed to be High Bandwidth Memory (HBM), are mounted onto a TFI interposer (25mm × 18mm) side by side, as shown in Fig. 2. After wafer level compression molding and back grinding, GPU chips are exposed and HBM chips are embedded with 100μm overmold. Si stiffener with 500μm thickness is then attached onto the top of the molded wafer to help reduce wafer warpage and assembly warpage and enhance thermal performance of the package. After carrier wafer removal, under bump metallization (UBM) and C4 bumping with 300μm pitch are conducted. After singulation process, the obtained TFI package with a stiffener is 25mm × 18mm × 1.15mm in size. TFI package is then mounted onto an organic substrate with C4 solder joints and finally attached

onto a FR4 printed circuit board (PCB) through ball grid array (BGA) solder joints, as shown in Fig. 2. The final TV design and material selection are determined based on co-design modelling results for achieving successful TFI wafer process, package assembly process, long term package/board level reliability and desirable thermal performance.

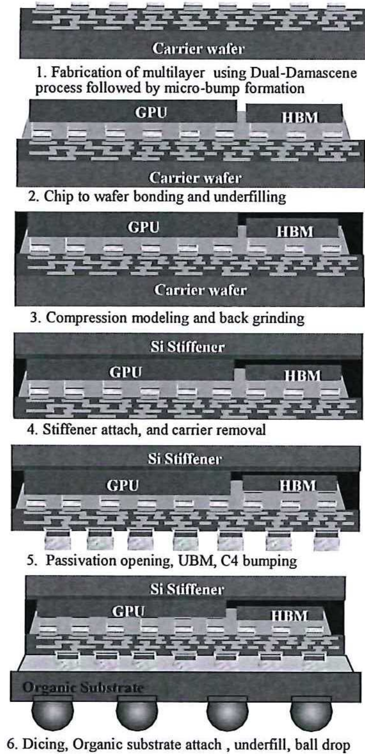


Figure 1. Process flow for TFI package.

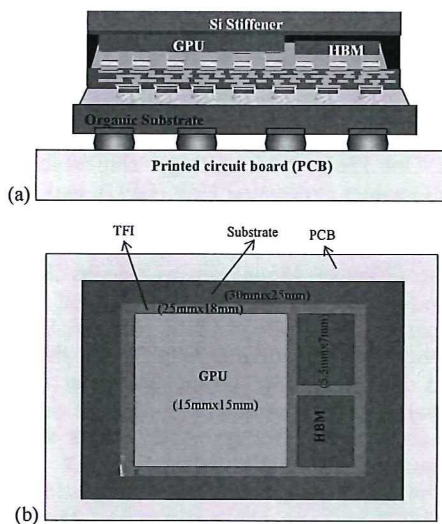


Figure 2. Test vehicle with TFI interposer technology, (a) schematics of cross section of TFI package, (b) layout of IC chips in TFI package.

## III. CO-DESIGN MODELLING METHODOLOGY

FEA simulation is a powerful and useful tool and has been widely used in the packaging design stage for virtual prototyping. Co-design methodology with FEA simulation has been established and applied for TFI technology as shown in Fig. 3 to optimize structure design, wafer process, assembly process, material selection and thermal performance. Co-design modelling method for TFI technology in this study includes wafer level warpage, package assembly process induced package warpage, package/board level solder joint reliability, and thermal simulation. Wafer process sequence simulation using a 3D quarter model of the wafer as shown in Fig. 4a has been established to simulate compression molding, back grinding, stiffener attach, carrier removal and back side RDL processes. First of all, experimental results are obtained and used for validating wafer warpage modelling results. Through wafer level modelling, suitable carrier wafer and EMC materials are recommended to control wafer warpage less than 2mm for 12" wafer, which is a requirement of warpage handling by lithography equipment. Effect of package substrate coefficient of thermal expansion (CTE) and stiffener application on assembly induced package warpage is simulated by a 3D half model of the package as shown in Fig. 4b to reduce package warpage. Long term package level and board level TC reliability are simulated to predict C4 and BGA solder joint lives. Comparison between 3D half model in Fig. 4b and 3D slice model in Fig. 4c is carried out for C4 joint reliability. In order to reduce solving time and computing resource, the validated 3D slice model as shown in Fig. 4d is also used for investigating board level solder joint reliability. Proper boundary conditions are applied for each model. Table I lists material properties used in each model. Stress free temperature is chosen for materials according to their active (process) condition in the actual processes. Temperature range from -40°C to 125°C and cycle duration of 1h are modelled for TC loading. The recommended materials and structure design based on reliability are aligned with that from wafer and package warpage simulation results. The optimized TV structure and materials are finalized based on co-design modelling results and ready for process and fabrication.

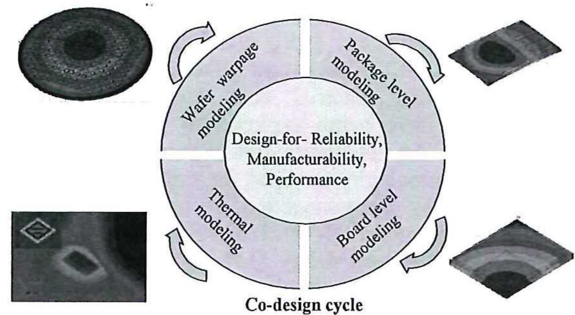


Figure 3. Co-design modelling methodology.

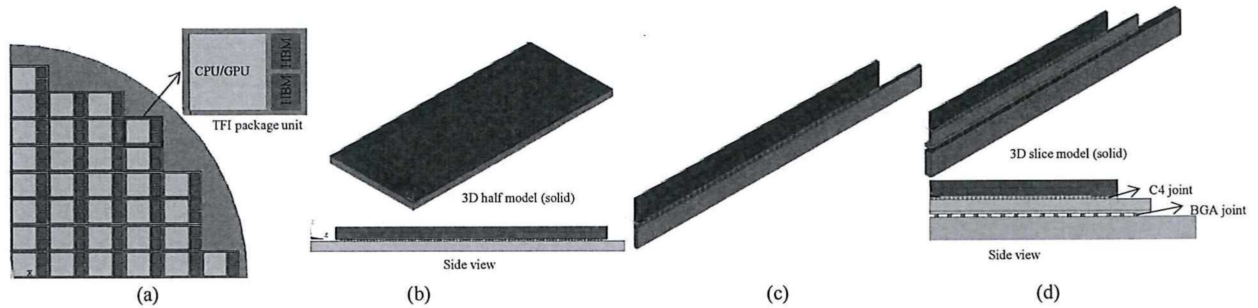


Figure 4. FEA models for different simulation purposes, (a) 3D quarter model for wafer warpage simulation, (b) 3D half model for package level simulation, (c) 3D slice model for package level simulation, and (d) 3D slice model for board level simulation.

TABLE I. MATERIAL PROPERTIES USED IN CO-DESIGN MODELLING

| Materials | Modulus (GPa) | CTE (ppm/°C) | Poisson's ratio | Tg (°C) | Remark | Thermal conductivity (W/mK) |
|---|---|---|---|---|---|---|
| EMC1-ref | 18/1 (E1/E2) | 7/22 (CTE1/2) | 0.3 | 160 | Molding 125°C | 0.8 |
| EMC2 | 34/0.45 | 6/21 | 0.3 | 180 | Molding 135°C | |
| EMC3 | 10/0.5 | 4/12 | 0.3 | 170 | Molding 125°C | |
| Underfill 1-ref | 13/0.5 | 23/80 | 0.3 | 120 | Cure 150°C | 0.8 |
| Underfill 2 | 12/0.5 | 24/75 | 0.3 | 115 | Cure 140°C | |
| Silicon die/stiffener | 131 | 2.8 | 0.28 | | | 130 |
| Passivation | 1.6 | 62 | 0.3 | >250 | Cure 180°C | |
| Bonding material | 2/0.2 | 60/200 | 0.35 | 220 | | 0.2 |
| Dielectric SiO2 | 73 | 0.5 | 0.17 | | | 1.5 |
| Carrier_Si | 130 | 2.8 | 0.278 | | | |
| Substrate /PCB | 25/11 | 15/46 | 0.39/0.11 | | Orthotropic | 0.4/18.9 |
| Solder | 41.7 (25°C) | 22 | 0.35 | | Creep model | 58.7 |
| Cu | 117 | 17 | 0.34 | | elastic-plastic | 386 |
| Solder mask | 2.4 | 50 | 0.3 | 101 | | |

## IV. RESULTS AND DISCUSSION

### A. *Wafer Warpage Modelling and Validation*

Firstly, warpage direction and sign are defined in Fig. 5. Process dependent modelling is conducted for wafer warpage simulation using element birth and death technique provided by software. Fig. 6 shows process dependent wafer warpage data at room temperature for the control model (also called reference model). EMC 1 and underfill 1 materials are used in the reference model. In the reference model, original molding thickness is 720μm and 100μm thick molding compound is removed after back grinding, and 770μm thick Si carrier and 500μm thick Si stiffener are modelled. Two critical processes inducing large warpage are identified by simulation results, i.e. molding process and carrier wafer removal process. Smiling shape warpage (>1mm as shown in Fig. 7a) occurs after wafer level compression molding and reduces slightly after back grinding process. The molded wafer becomes flat after stiffener attach. However, crying shape warpage (>2mm as shown in Fig. 7b) occurs after carrier removal and final RDL process, which arises challenge for final RDL process. In order to control wafer warpage less than 2mm through all processes, optimization needs to be conducted by FEA simulation.

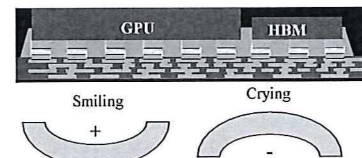


Figure 5. Wafer warpage definition and sign.

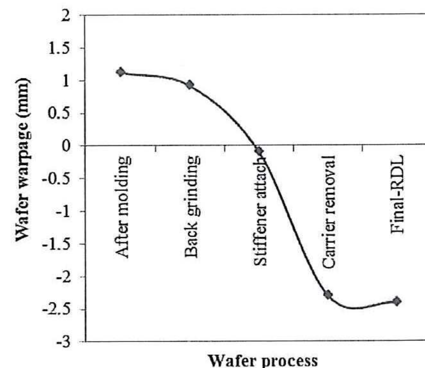


Figure 6. Wafer warpage at different wafer processes.

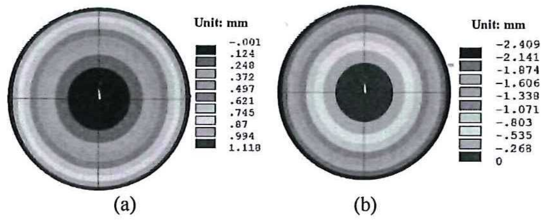


Figure 7. Wafer warpage simulation results, (a) after compression molding, (b) after final RDL process.

In order to validate the wafer warpage modelling method, experiment was conducted by using a simple structure as shown in Fig. 8a, in which 400μm thick mold compound is molded onto 770μm thick Si wafer. Wafer warpage after post mold cure (PMC) was measured by Fogale TMAP IR measurement equipment. Correlation between experimental and simulation results as shown in Fig. 8b indicates that simulation result has a good agreement with warpage measurement data. EMC3 leads to the lowest warpage among 3 EMCs due to the lowest CTE mismatch between EMC3 and Si wafer. The validated modelling methods can be implemented in the real TV fabrication process to analyze and optimize wafer warpage.

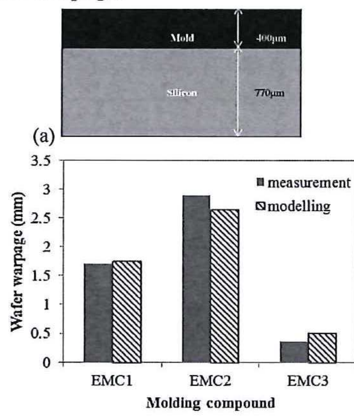


Figure 8. Validation of simulation results, (a) bi-layered simple structure for validation, (b) correlation between experimental and simulation results.

## B. *Wafer Warpage Analysis and Optimization*

The effect of underfill on wafer warpage is not significant, as shown in Fig. 9, because underfill volume is very small compared to Si and EMC materials. Major purpose of underfill application is to improve C4 solder joint reliability, which will be discussed in the subsequent section.

The effect of mold compound on wafer warpage is significant, as shown in Fig. 10, because wafer warpage is mainly induced by CTE mismatch between Si and EMC materials. EMC1 and EMC2 lead to similar wafer warpage, which is different from warpage results for the bi-layered simple structure due to different structures and volume ratios of EMC to Si. EMC3 results in the lowest wafer warpage among 3 EMCs due to low CTE value of 4ppm/K, which is one of candidates to ensure wafer warpage less than 2mm during wafer processes.

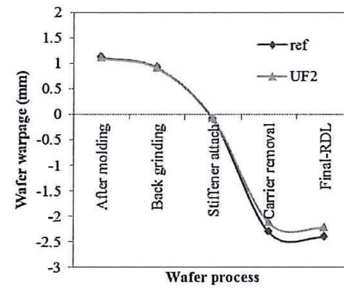


Figure 9. Effect of underfill on wafer warpage.

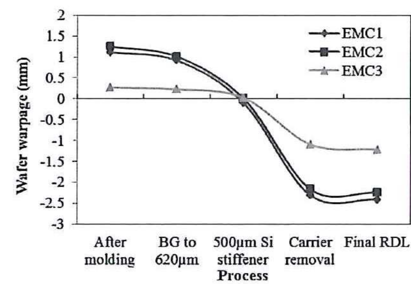


Figure 10. Effect of molding compound on wafer warpage.

Fig. 11 shows the effect of Si stiffener thickness on wafer warpage considering 2 major processes after stiffener attach. Wafer warpage is more than 2mm after carrier removal and final RDL process if stiffener is not applied. Even though EMC3 has low CTE value, wafer with EMC3 still has large warpage when stiffener is not used because EMC3 has low modulus which makes structure much softer and flexible. Stiffener makes structure stiffer and not easy to deform. Wafer warpage decrease with increasing stiffener thickness, especially for wafer with soft EMC material (EMC3 in this study). For the purpose of wafer warpage reduction, 500μm thick Si stiffener and EMC3 material are desirable choice for TFI package fabrication.

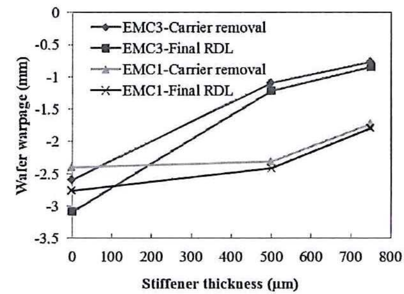


Figure 11. Effect of stiffener thickness on wafer warpage.

Fig. 12 shows the effect of package thickness on wafer warpage when using EMC1 material. When the stiffener is not used, wafer warpage decrease significantly with increasing package thickness after carrier removal and RDL process. Wafer warpage reduces with using the stiffener, especially for the thin package. The effect of package thickness on wafer warpage is not significant when the stiffener is attached.

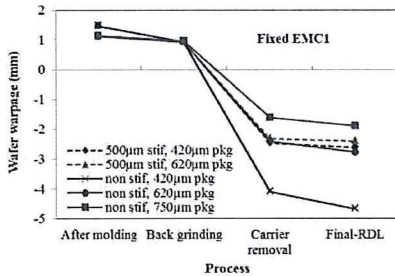


Figure 12. Effect of package thickness on wafer warpage.

### C. *Package Warpage Analysis*

Reflow condition is modelled for package assembly to simulate C4 solder joint reflow process induced package warpage. C4 joints have 300μm pitch and 160μm stand-off height after assembly. The warpage requirement is less than 100μm to ensure the good joint quality of C4 joint after reflow process. After C4 joint reflow process, underfilling process is conducted to protect C4 joints. Fig. 13 shows package warpage at both room temperature (25°C) and solder melting temperature (220°C). Package warpage has a convex or crying shape at 25°C and increases with increasing substrate CTE. Stiffener helps to reduce package warpage by 40~70%. Both EMC1 and EMC3 lead to similar package warpage at 25°C. However, package warpage has a concave or smiling shape at 220°C and also increases with increasing substrate CTE. Effect of stiffener on package warpage becomes not significant at high temperature. Based on simulation results, organic substrate with low CTE (<=10ppm/K) and stiffener on the top of the package are recommended to control package warpage less than 100μm.

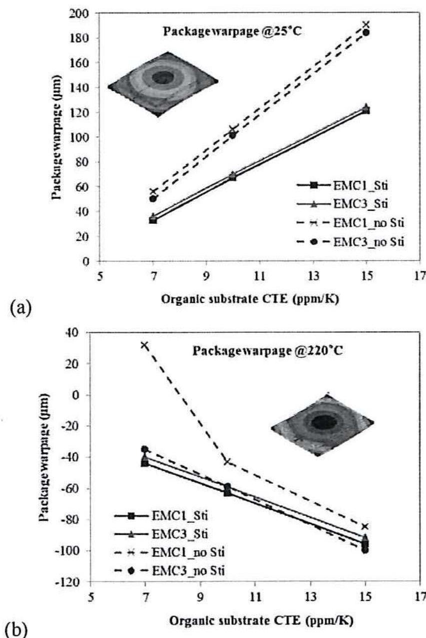


Figure 13. Package warpage at different temperatures, (a) 25°C, (b) 220°C.

Fig. 14 shows the effect of underfill on package warpage. For package with stiffener, underfill influences on warpage at 25°C is not significant. However, using underfill increases warpage by ~15% at high temperature maybe due to high CTE (above Tg) effect of underfill. For package without stiffener, using underfill reduces warpage at 25°C significantly maybe due to underfill enhancing stiffness of package structure. However, using underfill increases warpage significantly at high temperature maybe due to high CTE (above Tg) effect of underfill on thin package. Overall, designing package with stiffener helps to reduce package warpage through whole reflow process.

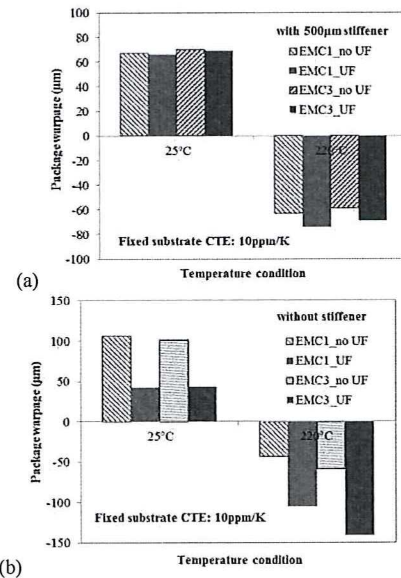


Figure 14. Effect of material on package warpage, (a) with stiffener, (b) without stiffener.

### D. *Package Level C4 Solder Joint Reliability*

Temperature cycling (TC) reliability is modelled for TFI package using the 3D half model (Fig. 4b) and slice model (Fig. 4c) to investigate and predict C4 joint thermal fatigue life. The SnAgCu lead-free solder is modelled for C4 joints using creep constitutive model. Temperature range from -40°C to 125°C and cycle duration of 1h are modelled for TC loading. Fig. 15 shows half model simulation results of creep strain energy density of C4 joints under TC loading for the TFI package with underfill and stiffener. C4 joints under Si die have large creep strain energy density value, which is corresponding to low solder joint life. Underfill is used to improve fatigue life of C4 joints under die area and makes them have much uniform life. Volume averaged creep strain energy density accumulation per cycle based on the interfacial layer of solder and package is used for fatigue life prediction. The energy based life model of SnAgCu solder is expressed below:

$$N_f = 137.6 \times W_{cr}^{-1.112} \quad (1)$$

where $W_{cr}$ is creep strain energy density from simulation results, and then fatigue life, $N_f$, can be predicted.

Fig. 16 shows fatigue life of C4 joints along critical column under GPU die edge from 3D half model (Fig. 4b). C4 joints show much uniform and improved fatigue life when package with underfill, especially for joints at package edge. The effect of stiffener on C4 solder joint life is not significant when underfill is applied in package. Package with stiffener has slightly lower C4 joint fatigue life compared to package without stiffener because Si stiffener makes package not flexible and increases CTE mismatch between package and substrate. The main purpose of stiffener is to help to reduce wafer/package warpage significantly. For package without underfill, C4 solder joint life is sensitive to DNP (distance to neutral point) effect. Therefore, underfill and stiffener are all needed to improve C4 solder joint reliability and reduce package warpage.

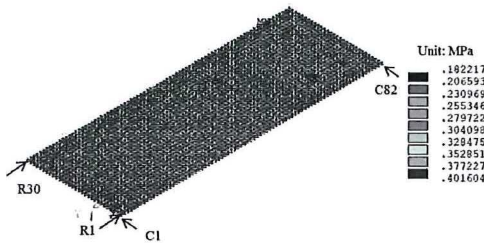


Figure 15. Solder joint creep strain energy density of C4 joints.

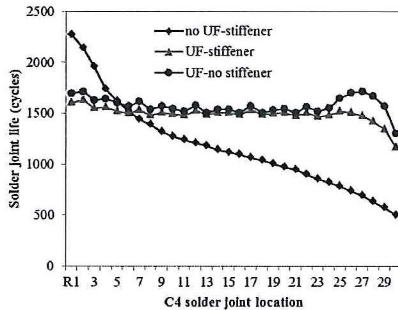


Figure 16. Effect of underfill and stiffener on C4 solder joint life.

3D half model is one very time consuming model, which needs more than 50h to solve TC simulation for each case of TFI package, like results in Fig 15. A simplified 3D slice model cutting along TFI package center to edge with one row C4 joints (Fig. 4c) is adopted for parametric study. In the 3D slice model, only large GPU die is modelled with the same distance from die edge to package as 3D half model. Simulation results show that the critical C4 joint locates at die edge and C4 joints under die have similar life with helping from underfill. Life prediction based on top and bottom interfaces of solder joint is similar. Simulation results from the 3D slice model are compared with those from the 3D half model, as shown in Fig. 17. Similar life prediction from slice and half models indicates that the slice model is one accurate and simple model which can be used to do more parametric studies effectively. In this TFI package TC simulation case, solving time of 3D slice model is just one tenth that of 3D half model.

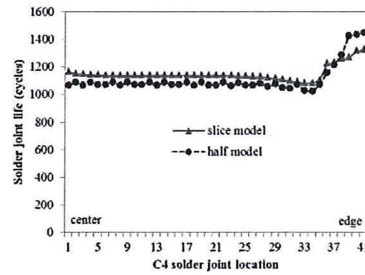


Figure 17. Comparison of C4 joint life predicted by slice and half models.

Underfill is important to improve C4 joint reliability, especially for large package size. However, it is essential and critical to choose suitable underfill to protect C4 joints. Otherwise, underfill may decrease C4 joint reliability [16,17]. Table II lists 4 underfills and their properties. CTE and Young's modulus are two critical mechanical properties affecting C4 joint reliability. Fig. 18 shows the effect of underfill on C4 joint reliability. Underfill 1 and 2 lead to similar results and good protection on C4 joint reliability due to their similar mechanical properties and similar CTE value as lead-free solder. Underfill 3 leads to poor C4 joint reliability due to high CTE and low Tg. Underfill 1 is recommended to improve C4 joint reliability.

TABLE II. MECHANICAL PROPERTIES OF UNDERFILL

| Material | Modulus (GPa) | CTE (ppm/°C) | Poisson's ratio | Tg (°C) |
|---|---|---|---|---|
| Underfill 1 | 13/0.5 | 23/80 | 0.3 | 120 |
| Underfill 2 | 12/0.5 | 24/75 | 0.3 | 115 |
| Underfill 3 | 7/0.5 | 37/101 | 0.3 | 118 |
| Underfill 4 | 6/0.5 | 37/125 | 0.3 | 150 |

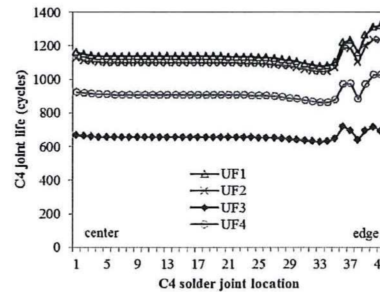


Figure 18. Effect of underfill on package level C4 joint reliability.

Organic substrate is another important material affecting C4 joint reliability. The most important material property of substrate is its CTE. Fig. 19 shows the effect of substrate CTE on C4 joint reliability of TFI package with or without underfill using 3D slice model. Substrate CTE has significant effect on C4 joint reliability of TFI package without underfill and C4 joint life is sensitive to joint location. C4 joint fatigue life increases with decreasing substrate CTE because low substrate CTE leads to low CTE mismatch between substrate and package. The effect of substrate CTE on C4 joint reliability is not significant for TFI package with underfill and C4 joint life is not sensitive to joint location. For package with underfill, low CTE substrate has no

improvement for solder joint reliability but help to reduce package warpage. Considering both reliability and warpage concern, substrate with 10ppm/K CTE is recommended for TFI package.

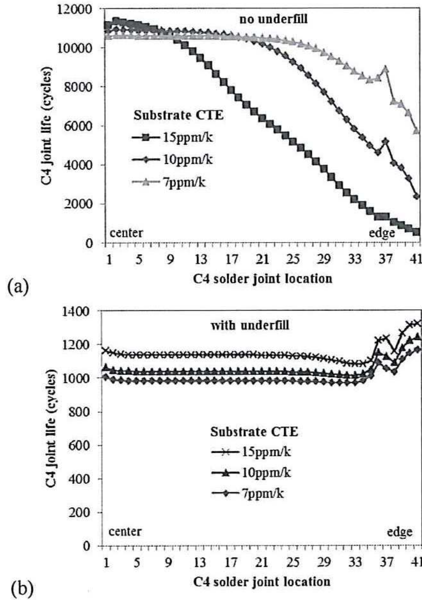


Figure 19. Effect of substrate CTE on package level C4 joint reliability.

## E. *Board Level Solder Joint Reliability*

When TFI package is assembled onto the PCB board, TCOB reliability is another concern for BGA solder joint which is simulated using 3D slice model (Fig. 4d). Organic substrate has the same CTE of 15ppm/K as PCB in TCOB simulation and substrate thickness is 1mm and PCB thickness is 1.6mm. C4 joints have slightly higher life under package level TC test than that under TCOB test for the same temperature cycling test condition due to stiffer structure of board level assembly compared to package level assembly, as shown in Fig. 20. BGA solder joint reliability (Fig. 21) is sensitive to joint location due to DNP effect because underfill is not applied for BGA joints. The BGA bottom interface (PCB side) is slightly more critical than the top interface (package side). The critical BGA joint is adjacent to Si stiffener edge, not package edge. BGA solder joints show higher fatigue life compared to C4 joints.

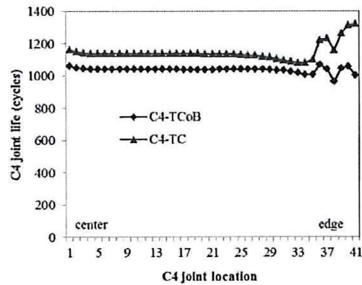


Figure 20. C4 joint reliability comparison between package TC and board level TCOB condition.

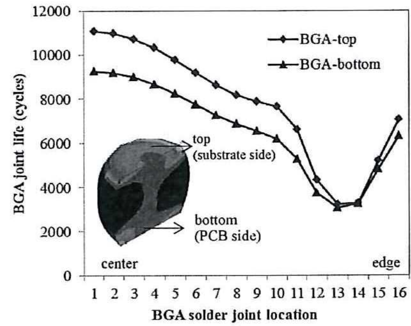


Figure 21. BGA solder joint reliability under TCOB condition.

Fig. 22 shows the effect of substrate CTE on BGA joint reliability, which is different from its effect on C4 joint reliability discussed above. CTE mismatch between chip and substrate is main contribution for C4 joint reliability while CTE mismatch between whole package (including chip and substrate) and PCB is main contribution for BGA joint reliability. Substrate with 10ppm/K CTE leads to high BGA life, which is also recommended for improving package level C4 joint reliability.

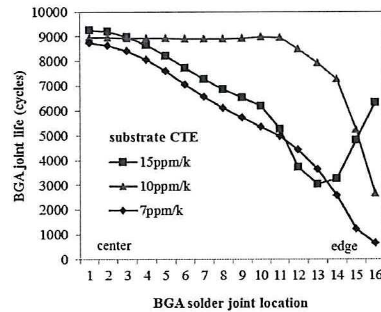


Figure 22. Effect of substrate CTE on BGA joint reliability under TCOB condition.

Fig. 23 shows the effect of substrate thickness on BGA joint reliability. Thin substrate helps to improve BGA solder joint reliability due to more flexible structure. BGA joint life is less sensitive to substrate thickness for package with 10ppm/K CTE substrate compared to 15ppm/K CTE substrate. Simulation results show that C4 joint reliability is not sensitive to substrate thickness under TCOB condition.

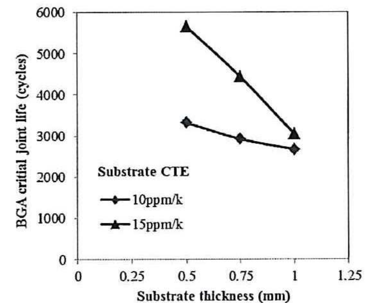


Figure 23. Effect of substrate thickness on BGA joint reliability.

### F. *Thermal Performance Analysis*

Thermal modelling is carried out for TFI package considering 2 power supply cases, i.e. 1W for GPU and 1W for each HBM, and 2W for GPU and 0.7W for each HBM. Fig. 24 shows the effect of Si stiffener on the maximum temperature of GPU and HBM chips. Stiffener helps to reduce HBM temperature and its effect on GPU is not significant. It is recommended to use 500μm chick Si stiffener to control the maximum temperature of HBM less than 85°C.

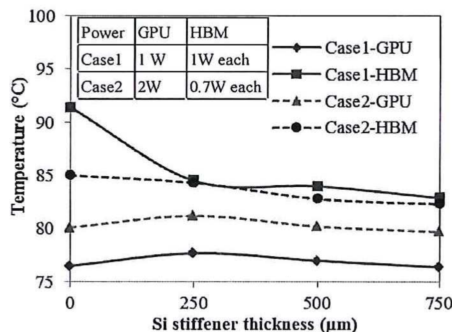


Figure 24. Effect of stiffener on temperature by thermal simulation.

## V. CONCLUSIONS

Co-design modelling methodology has been established for TFI packaging technology considering wafer process, package assembly and package/board level reliability and thermal performance. Low CTE EMC material has good matched properties with Si carrier wafer and helps to reduce wafer warpage. Stiffener is an effective way to reduce wafer warpage after carrier removal and assembly induced package warpage. Package and board level reliability show that C4 joint is more critical than BGA joint for TFI package. Through FEA simulation, the optimal underfill has been recommended for improving C4 solder joint reliability. C4 joints reliability is not sensitive to substrate CTE and thickness for TFI package with using underfill for C4 joints. Thin substrate with medium CTE value helps to improve BGA joint reliability. Stiffener can also help to improve package thermal performance, especially for HBM chip. Based on co-design modelling on warpage, reliability and thermal performance results, geometry and materials are optimized and recommended for final TV design and fabrication: low CTE EMC3 and underfill1, 500μm thick Si stiffener, 0.75mm thick substrate with 10ppm/K CTE.

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