Si Microfluid Cooler With Jet-Slot Array for Server Processor Direct Liquid Cooling

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***Abstract*— With the rapid growth of information technology (IT), the requirement of higher computing performance results in a much higher power density in data center server. A Si microfluid cooler with jet-slot array has been developed for direct liquid cooling of a server processor in a data center to handle increased heating power and maintain stable and uniform thermal performance. To mitigate the energy cost of the cooling system, the developed liquid cooling solution can enable aggressive heat removal capability with a low power consumption requirement. A stacked Si cooler of three plates and four different layer structures has been designed, fabricated, and tested. The novel heat sink includes jet-slot array, drain-slot array, and multiple pin fins. By overcoming the negative cross-flow effect, a high heat transfer rate has been obtained, covering the whole cooling area. With a volume flow rate of 0.5 L/min, 150-W chip heating power can be dissipated while maintaining the maximum chip temperature rise of ∼15 °C. A chip temperature variation of 5% has been realized, suggesting much desirable cooling uniformity for the whole chip. With the Si structure, this liquid cooling solution can be directly implemented onto the chip, and the thermal path can be sharply shortened, which enable a decreased thermal resistance between the cold plate and the heat source. Great agreement has been obtained between the experimental results and the simulation results. The developed direct liquid solution with Si cooler shows guarantee to enable the potential capability of future advanced server processors.**

***Index Terms*— Data center, direct liquid cooling, drain-slot array, jet-slot array, microfluid cooler, server processor.**

I. Introduction

With the rapid growth of information technology (IT), the requirement of higher computing performance results in a much higher power density in data center server [1]–[4]. The equipment operation reliability of a data center, which houses a variety of hardware, becomes utmost significant under extreme thermal conditions. High thermal design power (TDP) has brought a lot of challenges for traditional air cooling technology, which is currently implemented extensively [5]–[7]. In addition, energy efficiency has become a critical concern for data center applications. However, the energy consumption of a cooling system constitutes an important part of the overall energy usage in the data center [8], [9]. The requirement for the cooling solution is not only to achieve high heat dissipation but also to enable high energy efficiency, especially in the places where the weather is hot and humid for most time in a year. During the past decades, cooling strategies have begun to shift from traditional air cooling to newly developed liquid cooling [10]–[13].

Of the ability to achieve a high heat transfer rate with compact structure, microfluid cooling has extensively attained attention worldwide [14], [15]. With more components integrated into modern devices, the processors are crowded in the system, leaving limited space for cooling solution implementation. To achieve sufficient heat removal and energy saving, a microfluid cooler will be a good candidate to be employed to address the severe thermal issue for a high-performance processor in modern data center systems. A direct liquid cooling with a Cu plate has been studied in [16], for a high-density processor and GPU chip thermal management, and a heat sink thermal resistance of 0.5 °C/W was measured with a flow rate of 0.5 L/min. To accommodate a low-profile footprint, a cold plate of V-Groove microchannel with a split-flow technology has been studied for data center liquid cooling. A cold plate thermal resistance of 0.12 °C/W has been measured with a flow rate of 0.55 L/min [17]. Two types of a microchannel cold plate of parallel layout and concentrated layout have been developed for CPU in the data center server, capable of achieving a thermal resistance of >0.2 °Ccm^2/W with 1-L/min flow rate [18].

In this article, a Si microfluid cooler with jet-slot array has been developed for direct liquid cooling of a server processor in the data center to handle increased heating power and maintain stable and uniform thermal performance. To mitigate the energy cost of the cooling system, the developed liquid cooling solution can enable aggressive heat removal capability with a low power consumption requirement. A stacked Si cooler of three plates and four different layer structures has been designed, fabricated, and tested. The novel heat sink includes jet-slot array, drain-slot array, and multiple pin fins. By overcoming the negative cross-flow effect, a high heat transfer rate has been obtained, covering the whole cooling area. As shown in Fig. 1, the stacked Si microfluid cooler will be inserted into a liquid module as the cooling core for heat delivery and will be directly mounted on the bottom Si chip of high heating power. A customized thermal test chip is designed and fabricated to mimic thermal performance of a

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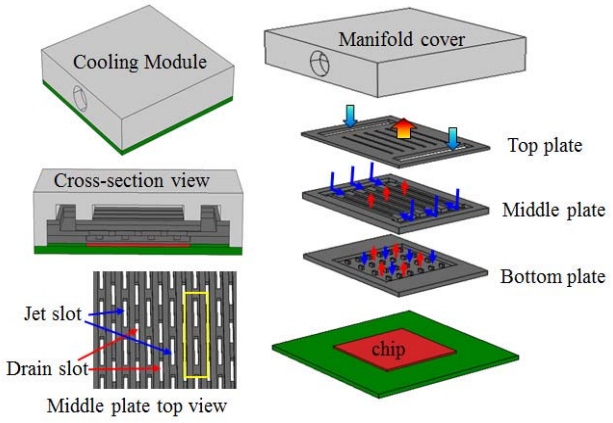

Fig. 1. Schematic of the Si-based microfluid cooler of stacked structures with a cooling module for flow arrangement.

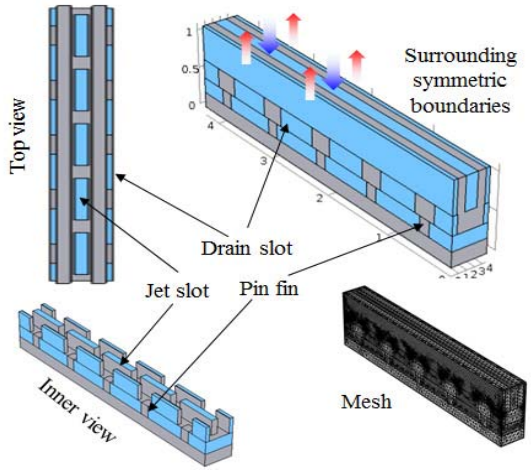

Fig. 2. Simulation model of the part structure and mesh distribution in different views with symmetric boundaries. Blue part: fluid. Gray part: silicon.

server processor. Simulations have been performed to design and optimize the microfluid cooler structure. Experimental characterizations have been conducted, and great agreement has been obtained.

II. Microfluid Structure Analysis

A 3-D thermal/fluid simulation model has been constructed using COMSOL Multiphysics, including heat transfer and fluid flow features. The microscale jet slot is able to enlarge the impinging area while achieving a high heat transfer coefficient (HTC). The microscale drain slot and pin fin are in the same row, next to the row including only jet slots, as shown in Fig. 1. The thermal test chip is of size 25×25 mm^2, with uniform heating. Then, to cover the chip area, a cooling area of 26×26 mm^2 is designed in the microfluid cooler, and a large number of slots will be included.

To obtain accurate analysis results and save computing time, only a part of the whole cooler structure is modeled, as highlighted in Fig. 1 by a yellow rectangle. The tetrahedral element size is set with fluid dynamics calibration for the fluid part and general physics calibration for the solid part. Symmetry boundaries are set at all surrounding surfaces externally. This model includes five jet slots of full-width in one row, and five pin fins of half-width in row with several drain slots of half-width, as shown in Fig. 2. The coolant flows from the top-side module into the cooler through the top plate of the flow separation layer structure. This layer separates the inlet and outlet flows for the below cooler structure. Then, it feeds into the inlet channel, the impinging jet is formed through a jet slot to the bottom surface, and the spent flow goes back to the outlet channel. This happens through the middle plate, which include two layers: inlet/outlet channel layer and jet/drain layer. The bottom plate forms the liquid chamber for heat deliver, and it includes the pin fin array for heat conduction enhancement and also for mechanical support. A mesh independency analysis has been conducted by changing the mesh elements sizes. A different pressure has been applied on the top-side inlet channel and outlet channel surfaces. Uniform heat flux has been loaded at the bottom surface for a heat dissipation investigation. All the other surfaces are set to be no slip.

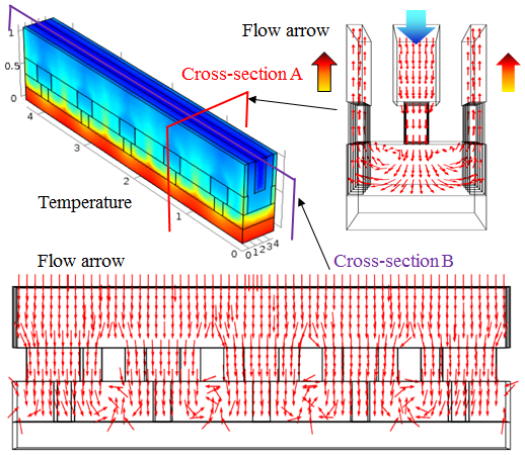

Fig. 3. Temperature distribution of the whole model and flow arrow distribution from different cross-sectional views.

Several simulations have been performed to study the thermal and hydraulic performance of the microfluid cooler with the jet-slot array and the drain-slot array, as shown in Fig. 3. Cross-section A cutting across the jet slot and the drain slot shows the motion of inlet jet flow and outlet drain flow, while Cross-section B cutting along the jet slot row shows the motion of jet impinging flow and its spent flow nearby. The results show that a uniform temperature distribution has been obtained at the heating surface, and each jet slot forms a similar impinging flow without negatively interfering the nearby jet. Parametric studies have been conducted to investigate the effect of some key structures, such as jet slot, drain slot, pin fin, and feeding channel, and to optimize the dimensions considering both performance and fabrication.

According to the simulation analysis, several conclusions have been obtained to design a microfluid cooler of high heat dissipation capability and low power consumption [19]. The main findings are as follows. In view of energy saving,

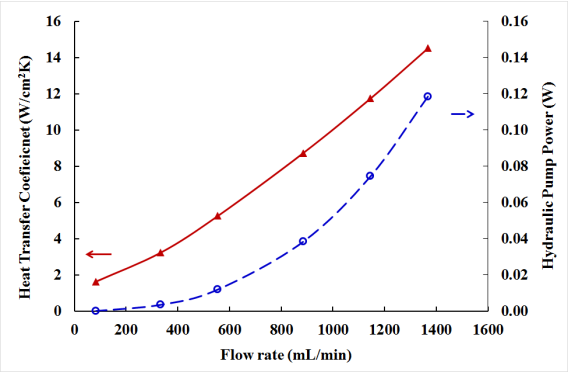

Fig. 4. Performance of the designed microfluid cooler from the simulation analysis.

we intend to provide low driving energy to the cooler. As to the jet-slot width, with the same low pressure drop of 1 kPa, a larger width can enable a smaller thermal resistance. By increasing the width from 80 to 100 μm, the resistance can be reduced by ~20%, and from 100 to 120 μm, only <3%. The thermal performance is quite sensitive to the distance between the jet orifice and the impinging wall; the smaller the distance, the better the cooling. However, a decreased distance also leads to an increased flow resistance in the bottom flow chamber. To balance the thermal and hydraulic performance, a distance of 200 μm has been used in the test vehicle. As to the drain slot, a larger width is better. A proper separation distance between the drain slot and the jet slot should be set, considering the fabrication issue for flow separation. Therefore, the drain-slot width of 120 μm is used. The effect of pin fin is similar to the orifice-to-wall distance. A larger thickness of the rectangular fin can enable better thermal performance and can cause a larger flow resistance in the bottom chamber. In consideration of the Si plate space allocation, three types of inlet/outlet channel width combinations (150/100, 100/150, and 110/120, unit: μm) have been studied. A similar performance has been obtained. To smoothly feed the jet slot, a wider inlet channel will be better for the performance. With the designed structure, the performance evaluation is shown in Fig. 4.

With the designed microfluid cooler, to obtain the flow rates of 0.5 and 1 L/min, the required pumping powers are very low, which are ~0.01 and 0.05 W, respectively. Even with the low volume flow rate, high spatially averaged HTCs can be achieved, which are $\sim 5 \times 10^4$ W/m^{2}K for 0.5 L/min and $\sim 10 \times 10^4$ W/m^{2}K for 1 L/min. In consideration of energy efficiency, the flow rate of 0.5 L/min will be the first choice. Definitely, if it is not sufficient to deliver high heat away, the cooling capability of the microfluid heat sink can be improved by increasing the volume flow rate with a little bit more energy cost. Test vehicles are fabricated based on this simulation analysis and optimization.

III. Si Microfluid Cooler Fabrication

As mentioned in Section II, there will be three Si plates with four structure layers to form the microfluid cooler in this design. The dimensions of the cooler structures are determined according to the simulation. The deep reactive-ion etching (DRIE) process will be conducted on an 8-in wafer of thickness ~700 μm to fabricate each Si plate. Middle plate fabrication is more complex than that of the top plate and the bottom plate since it includes two structure layers. A double-side DRIE process has been performed for the middle plate fabrication with optimized process parameters and modified steps to achieve low error geometry as the design. The layout of masks is shown in Fig. 5.

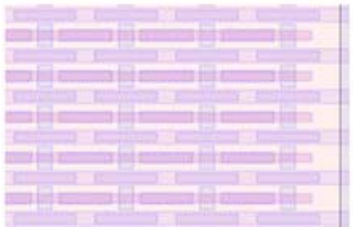

Fig. 5. Heat sink unit layout with jet slots and drain slots in the stacked masks.

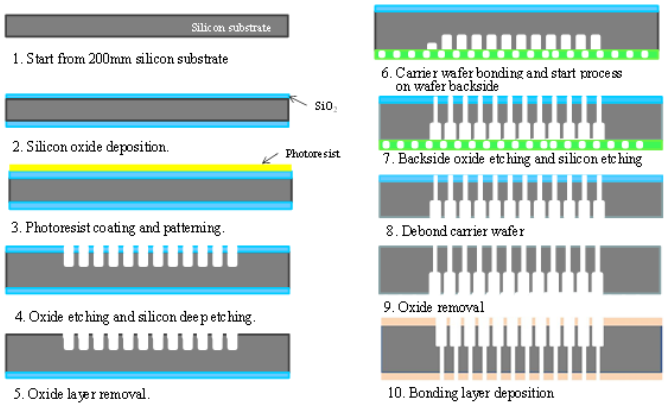

Fig. 6. General process flow of the double-side plate fabrication.

The wafer was brought for thermal-oxide growth on the front and back sides using high-temperature process condition to grow a thin thermal-oxide film. A lithography patterning process was performed to print the desired layer structures. The positive photoresist was selected and coated, and its thickness and hard-baking condition are critical factors to ensure high resistance and selectivity during plasma etching.

Double-side Si microstructure fabrication is the main challenge within the process flow. The process flow for the middle plate is illustrated in Fig. 6. For double-side etching, the jet slots and the drain slots are first opened, and etching stops at Si surface. Subsequently, a Si DRIE process was performed with a cyclical loop of etching and reoxidation. The period of one-cycle loop was optimized to ensure that the etching depth is straight and vertical to the surface level. Buffered oxide etch chemical cleaning and acidic wetbench were performed for oxide removal and photoresist cleaning separately after etching. After wafer one-side etching, a Si substrate as a carrier was temporarily bonded on the etched surface in order to perform the process on the other side of the wafer. Then,

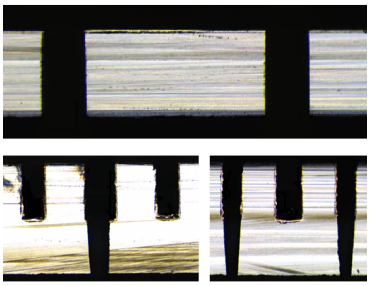

Fig. 7. Microscopic cross-sectional image of the fabricated top plate with channels and middle plate with double-side structures.

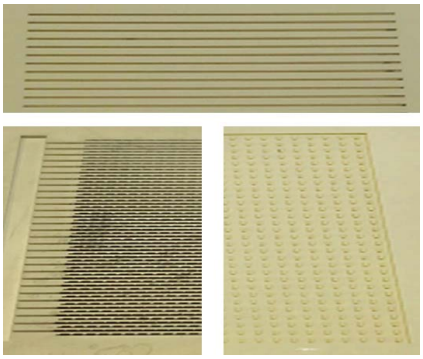

Fig. 8. Zoomed-in view of the solder layer plated and diced Si plates with flow channels, jet slots, drain slots, and pin fins.

backside oxide and silicon etching process were conducted to fabricate the inlet/outlet channels. After carrier wafer debonding, the oxide and photoresist layers were removed to finish the middle-plate fabrication of the double-sided structure layers. Similar processes were carried out to fabricate the top plate and the bottom plate, using single-sided pattern etching. After DRIE etching, both sides of the Si wafer will be deposited with a AuSn solder material for the following bonding process. The dicing mark was patterned during metallization. The prepared structures are shown in Figs. 7 and 8.

Then, the Si plates of size 32×42 mm^2 are diced out for a chip-level thermal compression bonding (TCB) process. The top, middle, and bottom Si plates will be bonded together in one time. To realize a reliable and tight cooler assembly, the process parameters have been properly adjusted. A successful bonding has been achieved without causing any crack, and no water leaking happens in our preliminary test for sealing quality check. The stacked microfluid cooler, as shown in Fig. 9, will work as the key heat delivering structure in the liquid cooling module.

IV. Experimental Characterization

To experimentally characterize the developed microfluid cooler, a thermal test chip is customized to mimic the heating performance of the current server processor. The thermal package size is set to 50×50 mm^2, and the chip size is designed as 25×25 mm^2, mounted at the center of the package substrate. This chip is designed to sustain >150 W and >120 °C for the high-power heat dissipation check of the cooling solution.

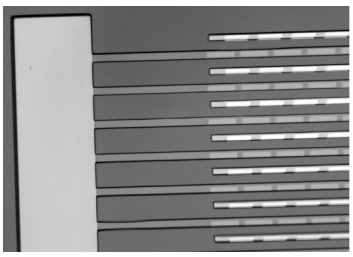

Fig. 9. X-ray image of the bonded Si cooler with multiple stacked layers.

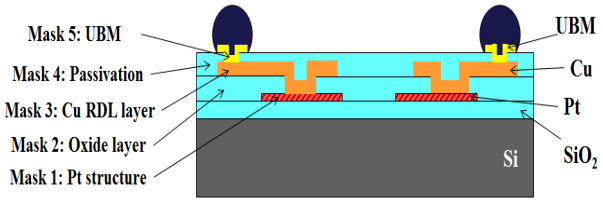

Fig. 10. Five mask layers for the thermal test chip fabrication.

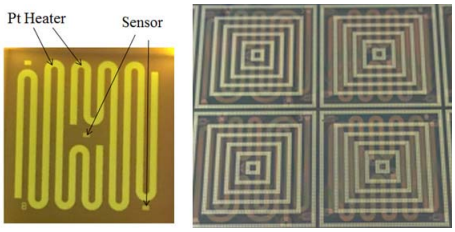

Fig. 11. Photograph of Pt structure and fabricated test chip.

Platinum (Pt) material is normally used for thin-film heater and sensor because of its linear relationship between resistance and temperature and its low-voltage thermal response. The electromigration is one important factor that should be considered for meandered heater and sensor design. The meandered-line cross-sectional area and the material current density will affect the maximum allowable current. Pt heaters are designed to cover $>80\%$ of the chip area, following the JEDEC thermal test standard. Two heaters and three sensors are included in one chip. There will need five masks for Pt structure fabrication, as shown in Fig. 10.

To form the heater and sensor structure, a dc sputtering process is conducted. These two types of structures of different widths, 1 mm for the heater and 0.2 mm for the sensor, are deposited simultaneously. The line thickness of both the heater and the sensor is the same 200 nm. The Pt structures designed are illustrated in Fig. 11. There are three sensors of the same structures located at different positions in the chip. The solder balls will be dropped to the chip for package attachment in the following process.

After the chip fabrication, the resistances of heaters and sensors at different positions in the wafer are measured and compared to check the consistency. As shown in Fig. 12, the averaged sensor resistance is $\sim$1075 Ω, and the averaged heater resistance is $\sim$292 Ω. The resistance variation is within $\pm 5\%$ over the whole fabricated wafer. The Pt sensor is calibrated for the temperature measurement. A quite good

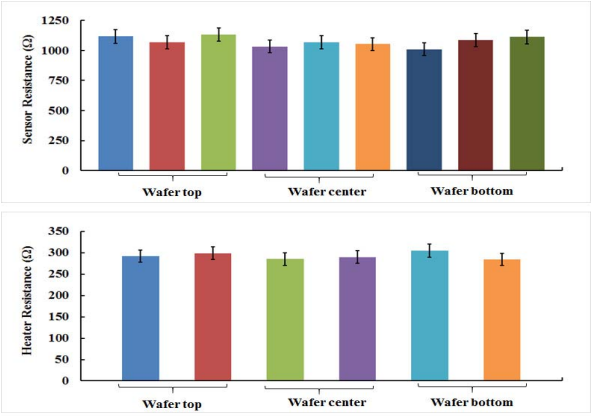

Fig. 12. Measured resistance of the heater and the sensor on an 8-in wafer.

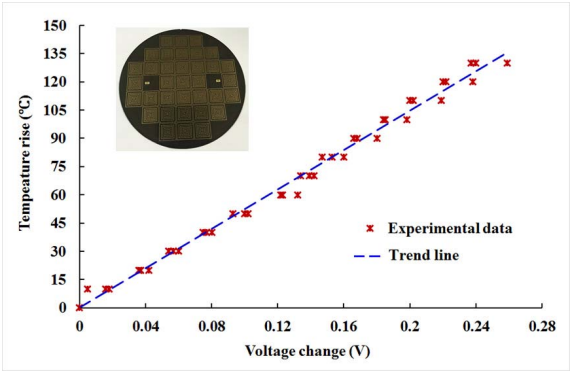

Fig. 13. Measured temperature variation versus voltage change of the fabricated sensors.

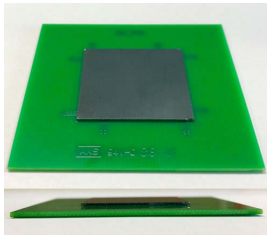

Fig. 14. Photograph of thermal test chip mounted on the test board.

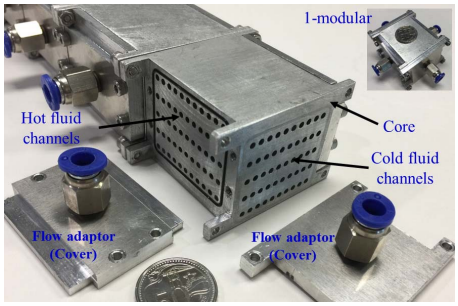

Fig. 15. Photograph of a liquid-to-liquid heat exchanger.

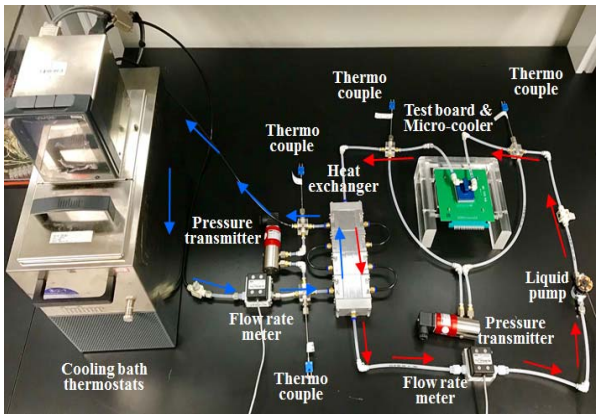

Fig. 16. Experimental test setup for the cooling solution characterization.

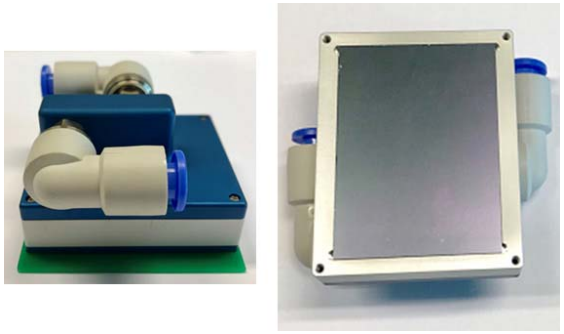

Fig. 17. Photograph of Si cooler sealed inside a cooling module for the test.

linear relationship has been obtained, as shown in Fig. 13. The K-factor for the temperature measurement will be 523 °C/V. To conduct the experimental test, a small current of 1 mA will be sourced to the sensor, and the voltage variation will be monitored and recorded accordingly.

The fabricated Si test chip is mounted onto an organic substrate of thickness 1 mm and size 50 × 50 mm^2, as shown in Fig. 14. To conduct the test, a thermal test printed circuit board (PCB) of size 127 × 139.5 mm^2 has been designed, following the JEDEC standard for a large package thermal characterization. For heating, dc power will be loaded to the chip. Water, as the coolant, will be driven in the flow loop by the microgear pump. The thermal couples and the pressure transmitters are used at two sides of the test vehicle. The room temperature and the water inlet temperature are 25 °C. Heated water from the microfluid cooler, delivering the heat from the thermal test chip, will go to the liquid-to-liquid heat exchanger for cooling down. The heat exchanger of cross-flow internal structure with microchannels has been designed and fabricated, as shown in Fig. 15 [20]. A high energy transfer efficiency can be achieved in this heat exchanger to handle high power dissipation in the system.

As shown in Fig. 16, there are two main loops in our test platform. The loop with a red arrow is the hot loop, including the test chip and the microcooler, for the heat source thermal management. The loop with a blue arrow is the cold loop, including the cooling bath, for heat rejection to the outside.

The bonded Si microfluid cooler is inserted into a cooling module, as shown in Fig. 17 (right). This module is of size 48 × 40 mm^2 and total thickness 20 mm, including two tube

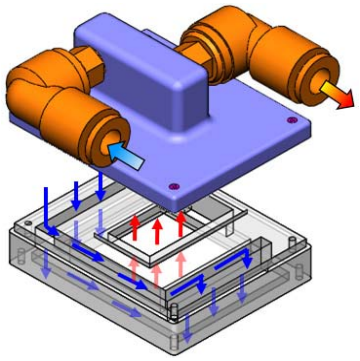

Fig. 18. Transparent view of the cooling module with flow arrows.

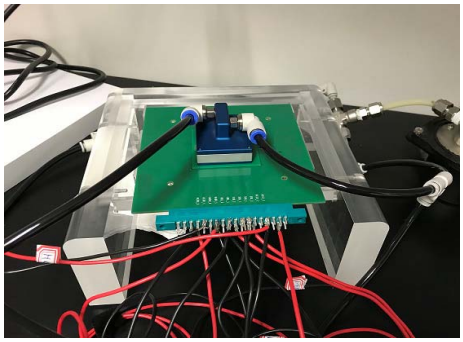

Fig. 19. Photograph of test vehicles with both the liquid loop and the electrical connection.

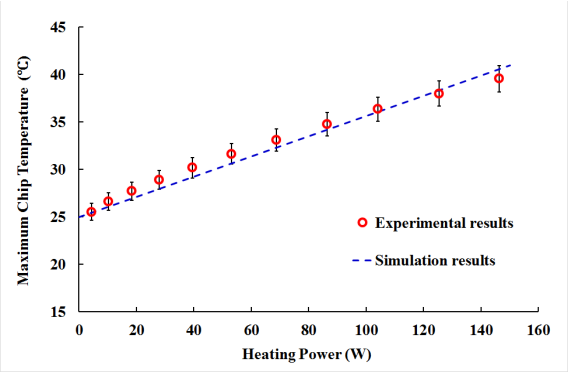

Fig. 20. Performance comparison between the experimental results and simulation results with the designed heat sink.

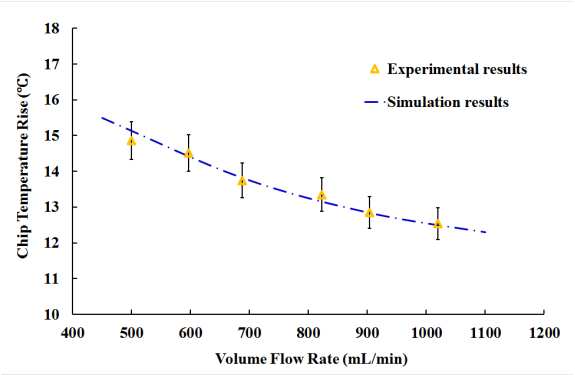

Fig. 21. Flow rate effect on thermal performance with the developed Si microfluid cooler.

fitting ports for the inlet and outlet flow connection. There are flow arrangement structures inside for jet-slot feeding and heated flow draining, as illustrated in Fig. 18.

The Si cooler is sealed inside this module with a thermal adhesive. Liquid leakage is prevented not only externally but also internally. If internal leakage occurs between the inlet and outlet flows, the cooling performance will be influenced, which may sharply drop down. Therefore, after assembly, a hydraulic test was performed to check the sealing quality, no leakage was found during the test, and a stable flow was obtained with the expected flow rate and pressure drop across the Si microfluid cooler. Thus, double leakage preventions have been employed in this design: one prevention for the internal Si cooler and the other one for the external cooling module.

The cooling module with the exposed Si cooler bottom surface is directly attached to the Si thermal test chip. A thin thermal interface pad of relatively a high thermal conductivity has been used at the contact interface between the Si cooler and the Si chip for gap filling. The cooling module is tightly attached to the substrate, covering the whole chip with the surrounding support frame, as shown in Fig. 17 (left). The test vehicle is fixed in a support stand for the experimental test, and the wires are connected for the heat power sourcing and temperature variation measurement, as shown in Fig. 19.

To evaluate the thermal performance of the designed microfluid cooler, the heating power has been increased gradually to monitor the temperature rise of the test chip. First, the flow rate of the microcooler is fixed at 0.5 L/min. Data were recorded after reaching a steady state for every case. During the experimental test, the flow in each loop is quite stable. Compared with the simulation analysis, the experimental results are shown in Fig. 20.

The maximum chip temperature is measured at the center sensor, which is shown in Fig. 20. This is mainly due to the heat sink inlet flow feeding issue. The feeding channel space is limited by the wafer thickness and the surround draining channel distribution. By structure optimization and balance, this effect did not cause obvious temperature gradient. The chip temperature measured through the sensor at both corners is only ∼5% lower. The flow rate for this test is fixed at 0.5 L/min. As observed from the results, to dissipate 100 and 150 W, the maximum chip temperatures are ∼35 °C and ∼40 °C, respectively. Great agreement has been obtained between the simulation results and the experimental results. To further reduce the chip temperature rise, several tests have been conducted with a higher flow rate. By increasing the volume flow rate from 0.5 to 1 L/min, around 16.7% improvement of chip temperature rise can be achieved, as shown in Fig. 21.

The sufficient heat removal capability has been achieved with a low pumping power requirement, suggesting high energy efficiency for thermal management. Of compact size, this developed cooling module integrated with Si microfluid cooler can be easily applied in 1U server chassis for a full liquid cooling system implementation in the high-performance data center.

V. Conclusion

A Si microfluid cooler with a jet-slot array has been fabricated and tested for server processor thermal management. To mitigate the energy cost of the cooling system, the developed liquid cooling solution can enable aggressive heat removal capability with a low power consumption requirement. A stacked Si cooler of three Si plates and four different layer structures has been developed. The novel heat sink includes jet-slot array, drain-slot array, and multiple pin fins. By overcoming the negative cross-flow effect, a high heat transfer rate has been obtained**,** covering the whole cooling area. With a volume flow rate of 0.5 L/min, 100- and 150-W chip heating powers can be dissipated while maintaining the maximum chip temperature rise of ∼10 °C and ∼15 °C, respectively. Uniform cooling has been obtained to maintain quite even temperature distribution over the whole chip. This cooler can be directly mounted on the Si chip, sharply shortening the thermal path for heat dissipation. Great agreement has been obtained between the experimental results and the simulation results. The developed direct liquid solution with the Si cooler shows guarantee to enable the potential capability of future advanced server processors.

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