Parasitic Surface Conduction Effect of TSV on Interconnection Performance in RF SOI for 2.5D Integration

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Abstract

Silicon interposer is being widely used for 2.5D integration due to its advanced performance. However, the resistivity of the silicon can be impacted by the parasitic surface conduction (PSC) near the Si-SiO_2 interface, especially for the space around through silicon vias (TSVs) where trap-rich layer cannot be created to alleviate the PSC effect. In this paper, the PSC effect of the TSV on the interconnection performance in a RF silicon on insulator (SOI) wafer is analyzed. A TSV GSG connection with a thin effective-resistivity layer of different resistivities presenting the low resistivity introduced by the PSC effect is simulated and analyzed. Moreover, a series of test structures is fabricated on a RF SOI wafer. The S parameters are measured and lumped RLGC parameters are analyzed. The simulated and measured results both demonstrate an increased loss of the TSV connection. The results are useful for future high-performance 2.5D integration design.

Introduction

Silicon interposer has become an advanced solution for 2.5D heterogeneous integration due to its advantages of compact form factor, high thermal conductivity, and coefficient of thermal expansion compatible with commercial-off-the-shelf chips [1-4]. Moreover, high resistivity silicon wafer [3, 4] is usually used to achieve good electrical performance, especially for RF or mixed-signal systems.

However, the high resistivity of the silicon can be influenced by the parasitic surface conduction (PSC) effect [5]. During the wafer fabrication, positive fixed charges can be generated near the Si-SiO_2 interface, which can attract the free carriers of the silicon, generating a low-resistivity layer and leading to high loss and poor electrical performance, as shown Fig. 1(a). To alleviate the PSC effect, RF silicon on insulator (SOI) with a trap-rich layer between the Si and SiO_2 was proposed [5], as shown in Fig. 1(b). The trap rich layer can capture the free carriers, ensuring the high resistivity. Our previous study shows that the insertion loss of the coplanar waveguide (CPW) on the RF SOI wafer is much smaller in comparison with the high resistivity silicon wafers [6]. Moreover, the low-temperature process can reduce the PSC effect, which is usually utilized for the backside fabrication. However, the through silicon via (TSV) widely used for vertical interconnections can be influenced the PSC effect as well.

In this paper, the PSC effect of the TSV on the interconnection performance in the RF SOI wafer is studied. First, a classic TSV GSG connection is studied by using full-wave simulations. A thin effective-resistivity silicon layer is built to represent the low resistivity silicon caused by the PSC effect. Lumped RLGC parameters are derived based on the simulation results to show the effect. After that, test structures including open-circuit TSV GSG connection, short-circuit TSV GSG connection, frontside CPW, frontside coplanar waveguide with ground (CPWG), backside CPW, backside CPWG, and front-back-front interconnection are designed and fabricated in a RF SOI wafer with the BEOL process on the front side and the low-temperature RDL process on the back side. RF measurements of S parameters are conducted on these test structures for characterization and analysis.

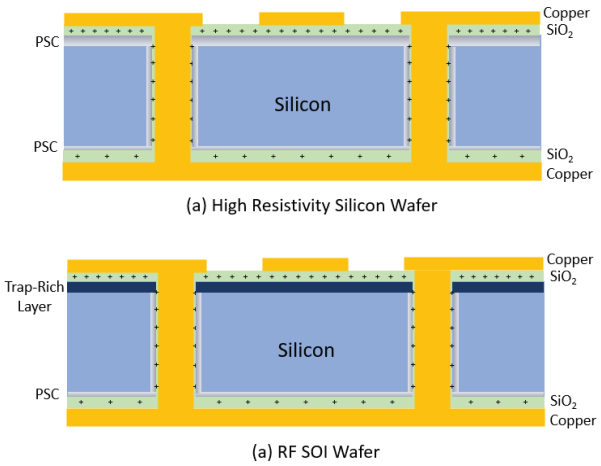


Fig. 1. Cross-section schematic of high resistivity silicon wafer and RF SOI wafer with the PSC.

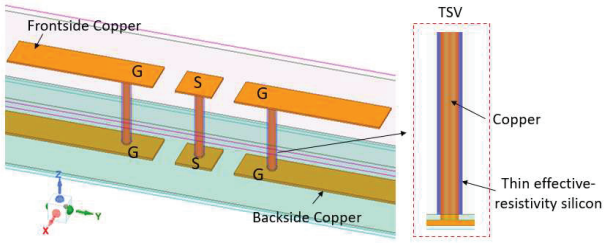


Fig. 2. Simulation model of the TSV GSG connection.

TSV GSG Connection

A classic TSV GSG connection is shown in Fig. 2, where one TSV is utilized for each connection from the frontside to backside copper trace. The ground trace is relatively large for matching the impedance and reducing the RF loss. To study the influence, full wave simulations of the TSV GSG connection is conducted. The thickness of the silicon is 100 um and the resistivity is 10 kΩ.cm. The thickness of the SiO_2 at the front and back sides is 5um. A thin effective-resistivity silicon layer with a thickness of 2 um is inserted around the

TSV to represent the low resistivity introduced by the PSC effect, as shown in Fig. 2.

The S21 performance of the TSV GSG connection with different resistivities of the effective-resistivity silicon layer is simulated and shown in Fig. 3. The resistivity of the effective-resistivity silicon layer varies from 10000 to 5 Ω.cm. It is observed that the S21 is stable with a resistivity larger than 100 Ω.cm, while the S21 decreases obviously with a resistivity lower than 20 Ω.cm. But the increment is not huge due to the short length of the TSV.

The TSV GSG connection can be equivalent to lumped RLGC parameters when its length is much smaller than the wavelength. Based on the simulated S parameters, the lumped RLGC parameters of the TSV GSG connection are calculated, and the results are shown in Fig. 4. It is found that the L and R representing the series inductance and resistance are relatively stable with different resistivities. While the C representing the shunt capacitance between the signal and ground has small variation at low frequency. The G representing the shunt conductance significantly changes with different resistivities.

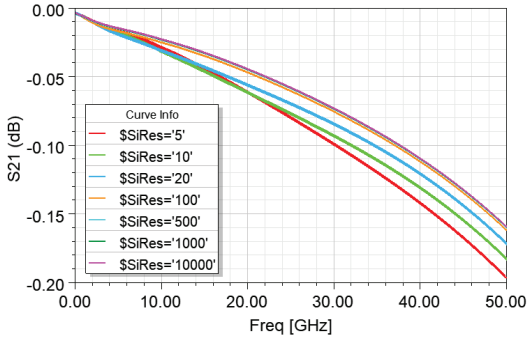
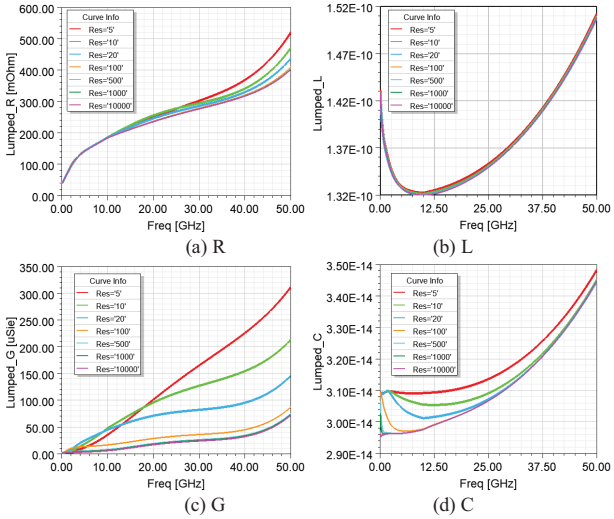


Fig. 3. Simulated S21 of the TSV GSG connection with different resistivities of the thin effective-resistivity silicon layer.



(a) R (b) L

(c) G (d) C

Fig. 4. Calculated lumped RLGC parameters of the TSV GSG connection with different resistivities of the thin effective-resistivity silicon layer.

Test Structures on RF SOI Wafer

A series of test structures is fabricated on a RF SOI wafer for the further study. The cross-section schematic of the RF SOI wafer is shown in Fig. 5. The wafer thickness is 100 um. The front side of the wafer has three metal layers fabricated by using the BEOL process [7]. The thicknesses of M1 and M2 are 1 um, while the thickness of M3 is 2 um. The M3 is designed for routing the RF signal, and the thicker copper layer provides higher conductivity and lower loss. The back side of the wafer has one metal layer fabricated by the low-temperature RDL process [7]. The thickness of RDL is 3 um. The front and back sides are connected through TSVs.

The wafer fabrication process mainly includes TSV formation, frontside BEOL, frontside UBM, wafer thinning, backside RDL, and backside UBM. The TSV's diameter is 10 um, and the pitch is 40 um. A thin silicon dioxide layer is deposited to isolate the TSV and silicon substrate. Fig. 6 shows the X ray image of the TSV after copper filling, where no abnormalities are observed. The fabrication process of the frontside BEOL mainly includes SiO_2/Si_3N_4 deposition, etching, copper plating, annealing, and CMP. The backside RDL process mainly has SiO_2/polymer deposition and Copper plating. Different from the BEOL, the backside RDL uses low temperature process for the deposition and annealing. Therefore, the PSC effect introduced by the backside RDL process is small [8].

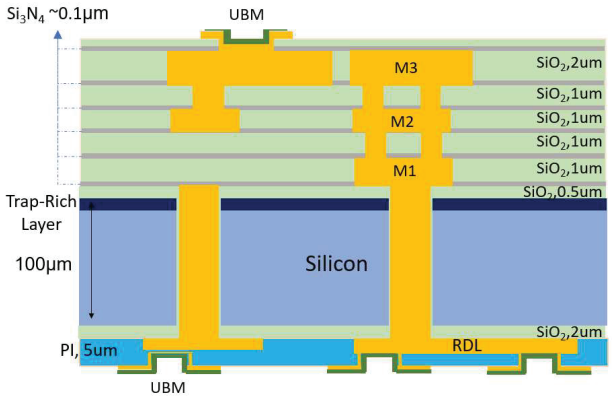


Fig. 5. Cross-section schematic of the fabricated RF SOI wafer.

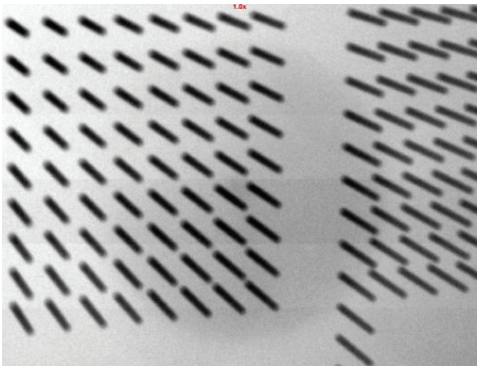


Fig. 6. X-ray imaging of the copper filled TSVs.

The fabricated test structures have open-circuit TSV GSG connection, short-circuit TSV GSG connection, frontside CPW, frontside CPWG, backside CPW, backside CPWG, and front-back-front interconnection. The structure schematics of the open-circuit TSV GSG connection, short-circuit TSV GSG connection, frontside CPWG, and front-back-front interconnection are shown in Fig. 7. The frontside CPWG uses M3 for the GSG signal traces and RDL for the additional ground. The width of the signal trace is 50 um, and the gap between the signal and ground traces is 31 um. The ground signals are connected by the TSVs.

On the other hand, the frontside CPW only has the GSG signal traces on M3 with identical dimensions but does not have the additional ground on RDL. While the backside CPW and CPWG are the flip version of the frontside CPW and CPWG. The backside CPW and CPWG use RDL for the GSG signal traces and M3 for the additional ground. Moreover, the front-back-front interconnection is a combination of the frontside CPWG, backside CPW, and TSV GSG connection. Fig. 8 shows the front view of the fabricated front-back-front interconnection.

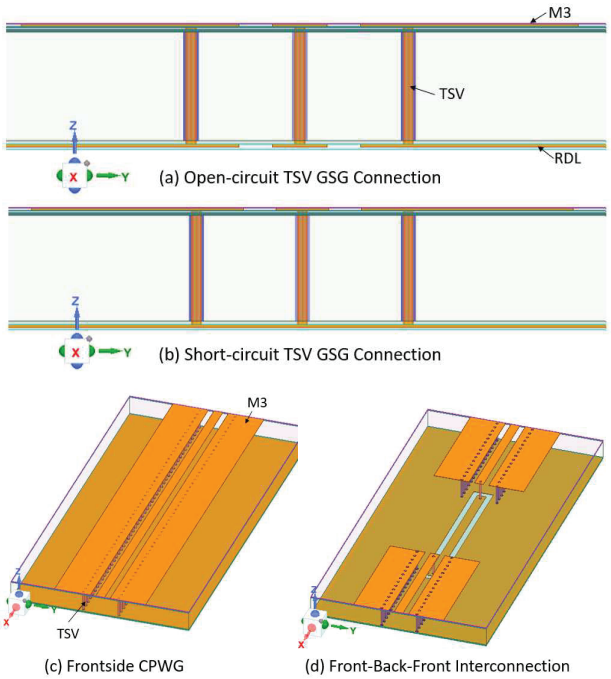


Fig. 7. Structure schematics of the (a) open-circuit TSV GSG connection, (b) short-circuit TSV GSG connection, (c) frontside CPWG, and (d) front-back-front interconnection.

Fig. 8. Photographs of the fabricated front-back-front interconnection on the RF SOI wafer.

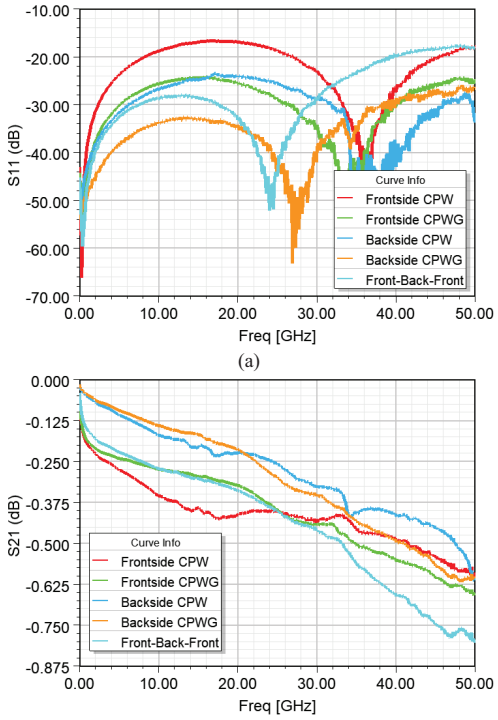


Fig. 9. Measured (a) S11 and (b) S21 of the CPW, CPWG, and front-back-front interconnection with a length of 2 mm.

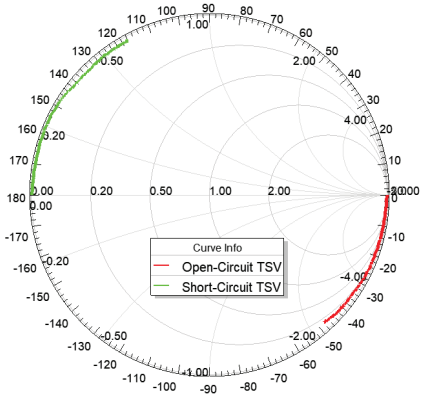
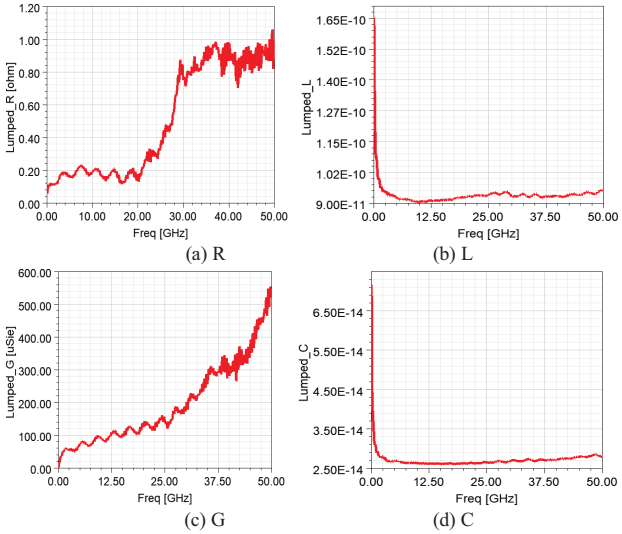


Fig. 10. Measured smith chart (S11) of the open-circuit TSV and short-circuit TSV GSG connections.

Experimental Results and Analysis

RF measurements of S parameters are conducted on the fabricated test structures by using a probe station. Fig. 9 shows the measured S11 and S21 of the frontside CPW and CPWG with 2 mm, the backside CPW and CPWG with 2 mm, and the front-back-front interconnection with a total length of 2 mm. All the five interconnections have good matching performance, and the S11 is less than -15 dB at the frequency smaller than 50 GHz. Moreover, the insertion losses of the interconnections are small. Comparing to the backside CPW and CPWG, the frontside CPW and CPWG have higher loss. The S21 of the CPW and CPWG are very close and the small difference is caused by the matching. The S21 of the frontside CPWG, backside CPW, and front-back-front interconnection

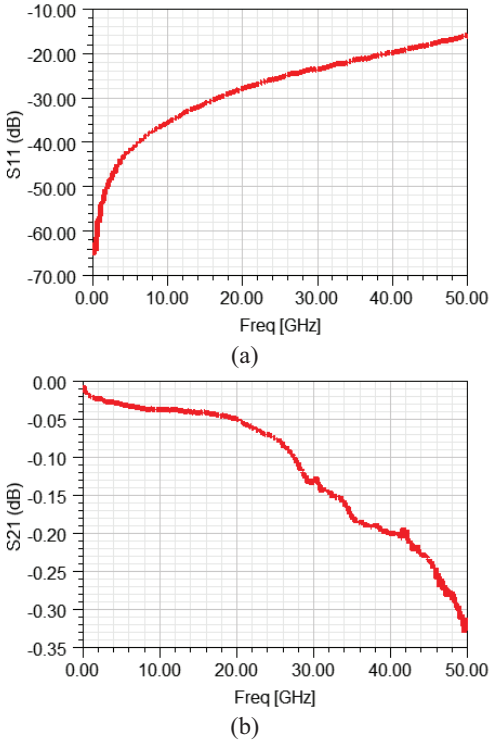
at 30 GHz are -0.442 dB, -0.328 dB, and -0.463 dB, respectively.



(a) R (b) L

(c) G (d) C

Fig. 11. Lumped RLGC parameters of the fabricated TSV GSG connection.



(a)

(b)

Fig. 12. Calculated (a) S11 and (b) S21 of the fabricated TSV GSG connection according to the lumped RLGC parameters.

The measured smith chart (S11) of the open-circuit and short-circuit TSV GSG connections is shown in Fig. 10. Based on the measured S11 of the open-circuit and short-circuit TSV GSG connections, the lumped RLGC parameters and the S21 of the TSV GSG connection can be calculated. The results are shown in Fig. 11 and Fig. 12, respectively. From the RLGC results, a large G is observed for the TSV GSG connection, indicating the low resistivity introduced by the PSC effect. While the matching performance and insertion loss of the TSV GSG connection are good. The S11 is smaller than -25 dB and the S21 is -0.05 dB at 20 GHz.

Conclusion

This paper has studied the PSC effect of the TSV on the interconnection performance in the RF SOI wafer. Full-wave simulations of a TSV GSG connection with a thin effective-resistivity layer of different resistivities presenting the low resistivity introduced by the PSC effect have been conducted. A series of test structures has been fabricated and measured. Lumped RLGC parameters have been derived for analysis. The simulated and measured results show that the PSC effect mainly changes the shunt conductance of the TSV and, therefore, increases the insertion loss.

Acknowledgments

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