A 18-22GHz, 13.2mW, 0.22mm^2, 5 bit VGA with 15.5dB linear in dB gain control in 130nm SiGe for Satcom on the Move (SOTM) applications

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***Abstract*—This paper proposes a linear in dB variable gain amplifier (VGA) employing a compact topology obtained by modifying the Gillbert Cell. The difference between the quiescent currents of the differential switches stacked over the main transconductor is made to vary exponentially with the controlled current to ensure linear-in-dB control. Single stage is able to provide 15.5dB gain control by biasing the switching transistors through a current DAC exploiting the exponential I-V relationship in BJTs. The presented VGA operating from 18-22GHz outperforms state of the art digitally controlled VGAs in terms of low power consumption (13.2mW) and wide dynamic range (15.5dB, 5-Control bits + 3 Calibration bits) while all other performance metrics like chip area are comparable.**

Keywords—linear-in-dB VGA, phased arrays, SatCom, Beam tapering

I. INTRODUCTION

In order to serve the ever-increasing demand on data rate and latency, 3GPP has extended the RF frequency band to mmWave (28GHz) and proposes to integrate SatCom networks called non-terrestrial networks (NTN) in 5G (5G NTN). mmWave bands typically employ phased arrays (active-antennas) to increase the antenna gain exploiting the lowering dimensions of antennas with frequency and thus compensate for the increased path loss which is proportional to frequency. Phased arrays generate well-defined beams in space (beam forming) by vectorially adding the signals with gain and beam-width directly and inversely proportional to the number of elements respectively. NTNs with narrow multiple beams reusing the same frequency spectrum but separated in space (space domain multiplexing) results in improved spectral efficiency and throughput as well. SatCom on the Move (SOTM) belongs to NTN employing phased arrays and the proposed VGA is employed in Ka/K band (29GHz uplink and 19GHz downlink) SOTM applications. Also, since the beams radiate in the well-defined zones, they help wirelessly powering sensor nodes (SNs) without interfering the other wireless links at the same frequency.

In the phased array multitude of identical, transmit/receive signal paths (channels), whose individual gain and phase are controllable, are combined in space [1]. This enables manipulation of the overall antenna beam pattern, such as electronic steering of the beam, creating multiple antenna beams, suppressing the antenna side lobes (beam tapering), nulling interfering signals in a specific direction etc. The variable gain amplifier (VGA), in addition to controlling the gain of each channel appropriately for beam tapering, also need to compensate for varying signal losses of each channel such as interconnect to antennas, phase dependent insertion loss etc. Thus, VGA must have sufficiently wide gain dynamic range. Lower area and power consumption are also paramount importance since the number of channels per array is very large, for example a SOTM array employs >100 channels (typically 1000) to meet the narrow beam requirements.

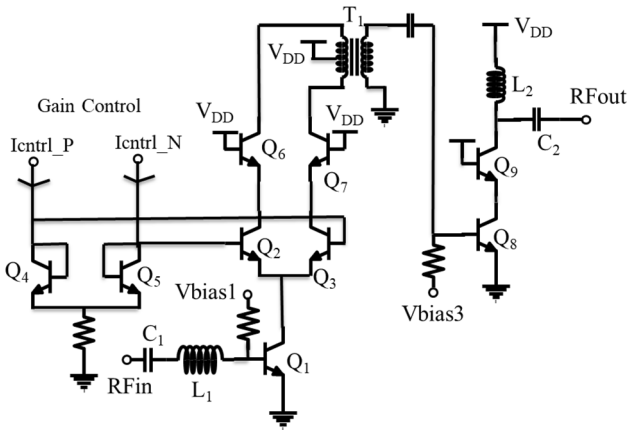

Fig. 1. Circuit schematics of the VGA. The differential control current (IQ4-IQ5) varies the current in the differential switching pair (IQ2-IQ3) in the signal path to vary the gain

In [2], a two stage VGA varied its gain by changing the base biasing of the input BJTs with degenerative resistors at the emitter resulting in narrow gain control range, demanding two stages for achieving required gain dynamic range. In [3], effective size of the MOSFETs were varied by turning them on and off and vary the gain however, the gain variation is limited demanding multiple stages compromising power, bandwidth & linearity like [2]. Controlling gate bias to vary the gain as in [4] eliminates the parasitic capacitor by adding another transistor whose signal flows with an opposite polarity. The linear in dB gain control is dependent on process parameters like mobility μ_n causing increased sensitivity of gain errors to PVT [4]. Wideband designs such as [5] employ bleeding currents, consuming as high as 104mW. Simpler VGA topology so that it occupies low silicon area, while consuming least current, with linear in dB gain control desired for SOTM applications, is still not published. Proposed Gilbert cell like VGA topology exploits the exponential dependence of I_C with V_{BE} in BJTs to obtain wide linear in dB gain range of 15.5dB (5-bits excluding calibration bits, LSB 0.5dB), consuming only 13.2mW, and occupying 0.22mm^2 silicon area.

II. VARIABLE GAIN AMPLIFIER

A. Phase and Input Impedance invariant Gain Control

The schematic of VGA employing bipolar npn transistors is shown in Fig. 1. Q_1 forms the first stage with C_1 and L_1 to match the input impedance to 50Ω. The collector current of the Q_1 is injected into the emitter of Q_2 and Q_3, thus the signal current is divided into two branches. Since the dc biasing of Q_1 is fixed and does not change with the gain of the VGA, the input matching of the VGA do not vary with gain setting. Gain settings changes the difference in the quiescent currents of Q_2 and Q_3 (I_{Q2}-I_{Q3}), as given below (1), while the sum I_{Q2}+I_{Q3} is

equal to I_{Q1}. BJTs Q_2-Q_5 forms a translinear circuit that determines I_{Q2} and I_{Q3} [6].

$$I_{Q2} - I_{Q3} = (I_{Q4} - I_{Q5}) * I_{Q1}/(2 * (I_{Q4} + I_{Q5})) \quad (1)$$

I_{Q2}-I_{Q3} is the differential collector currents and is proportional to the collector currents of I_{Q4}-I_{Q5}. Keeping I_{Q4}+I_{Q5} constant, changing I_{Q4}-I_{Q5} thus determines the gain. It may be noted that I_{Q4}+I_{Q5} is mirrored to form total current of the differential pair Q_2 and Q_3, which is equal to I_{Q1} set by vbias1. The cascodes Q_6 and Q_7 (Common Base) provides the isolation that serves two purposes: (i) it isolates the parasitics of Q_2 and Q_3 that varies when gain is tuned thus reducing the phase errors and (ii) it improves overall stability.

The transformer T_1 will convert the differential outputs back to single ended. Q_8 and Q_9 acts as a buffer with fixed gain and matches to 50Ω. It may be noted that Vbias3 can be varied to increase the gain control range further with similar tradeoffs as in [2], however it is fixed in our test chip as it only serves as a buffer.

III. LINEAR IN DB GAIN CONTROL

The gain control transfer function (Gain in dB Vs. control word) in phased array have to be linear in dB so that tapering is straightforward for the digital signal processor (DSP) in base band. The gain is proportional to g_m, which in a BJT is proportional to I_C (g_m= I_C/V_T). If the differential quiescent current (I_{Q4}-I_{Q5}) of equation (1) is made to vary exponentially with control current, say, (I_{Q4}-I_{Q5}) is equal to $A * \exp[I_{linear}]$, where A is a constant and I_{linear} is a linearly varying current, then we are able to vary the gain of the VGA to be linear in dB with the current I_{linear}. One of the method to generate differential gain control currents (I_{Q4}-I_{Q5}) is to use a high-resolution current steering digital analog converter (DAC) that mimics an exponential relationship. For example to meet a gain range of 15.5dB (5-bits, LSB 0.5dB), the DAC must be generate a differential gain control currents, (I_{Q4}-I_{Q5}), that is $Ae^{15.5}$, with steps of 0.5. The exponential relationship means the step values I_{Q4}-I_{Q5} need to be very small near LSB and larger near MSB demanding very high resolution of DAC demanding significant additional power consumption and area.

BJTs offer the intrinsically exhibit an exponential dependance of I_C with V_{BE}. Fig. 2 shows the schematics of exponential current generation. Assuming that the base currents are negligible and applying KCL and KVL for the current through and voltage across R (Ibias1-Iset), the collector currents of Q_{11} and Q_{12} are given by

$$I_{Q11} = I_{Q12} = I_s \exp\left[\frac{(I_{bias1} - I_{set}) * R}{V_T}\right] \quad (2).$$

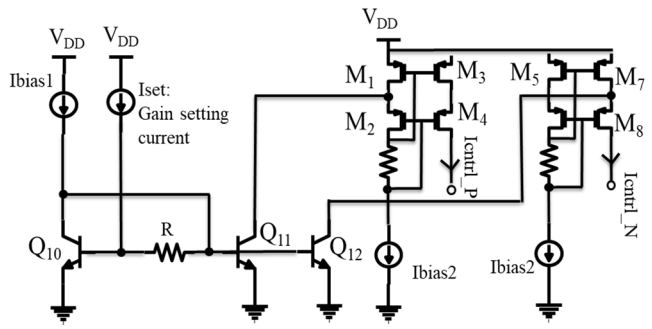

Fig. 2 Control current (Icntrl_P - Icntrl_N) generation circuit. V_{BE} of Q_{11} and Q_{12} vary linearly with current through R (Ibias1-Iset) making I_{Q11} and I_{Q12} exponential function of [R*(Ibias1-Iset)]

From (2), if we manage to vary I_{set} linearly, the collector currents of I_{Q11} and I_{Q12} is able to generate control currents that varies exponentially. This will then cause the VGA to have linear in dB gain control. Value of I_{set} is programmed through a simple linear current steering DAC not shown in the schematics. M1-M4 and M5-M8 are modified current mirrors that will generate currents I_{bias2}+I_{Q11} (Icntrl_Ip) and I_{bias2}-I_{Q12} (Icntrl_In) respectively. It may be noted that the collector current of Q_{11} (I_{CQ11}) is connected to the primary side of current mirrors M_1 and M_2 so that they add, whereas I_{CQ12} is connected to the mirrored M_7 and M_8 so that it is subtracted respectively to the bias currents. The differential control current (Icntrl_P - Icntrl_N) is proportional to I_{Q11} or I_{Q12}. The exponential current generator is sensitive to temperature but it is mitigated by making the currents (I_{bias1} and I_{set}) to track V_T.

IV. EXPERIMENTAL RESULTS

The VGA chip was fabricated in SiGe 130nm BiCMOS and measures 550µm x 400µm (=0.22mm^2) excluding the control pads as shown in Fig. 3. V_{DD} and control pins were bonded to a FR4 PCB and RF performance was characterized by wafer probing. Total power consumption is 13.2mW.

A. Small Signal Measurements

Fig. 4 shows the measured gain of the VGA with different gain settings across the frequencies. The maximum gain of VGA is 8.7dB centered at 19.5GHz with a 15.5dB gain control range. Corresponding phase is also plotted in the right Y-axis. The 3dB bandwidth of the VGA is 3.77GHz

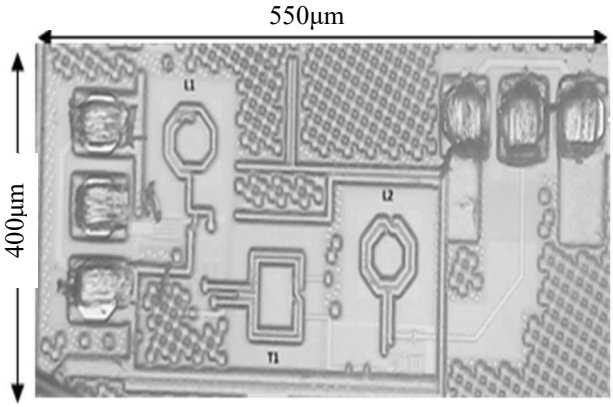

Fig. 3 Chip photo of the VGA. RF input pads in left. The symmetrical rectangular structure in the bottom is the transformer T_1. L_1 (left top) & L_2 are input matching and buffer load inductor respectively.

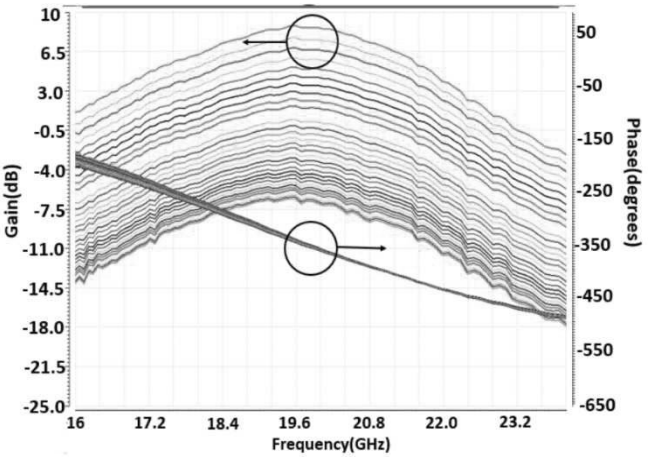

Fig. 4 Measured Gain of the VGA and its phase shifts vs. frequency for different gain settings. Phase plot is linear across the gain settings and phase errors are minimum.

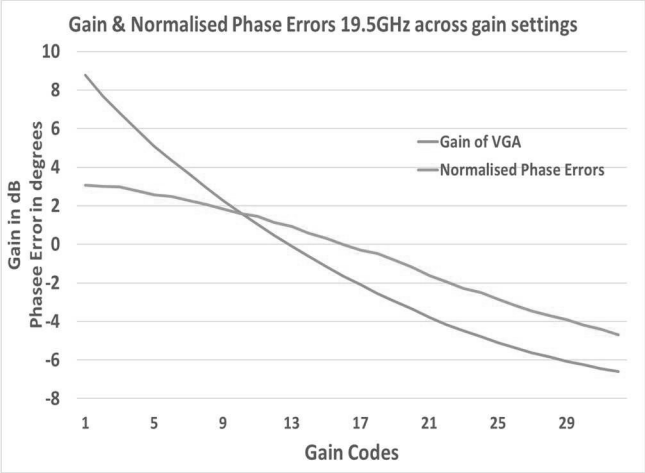

Fig. 5 Gain and normalized phase errors of theVGA at 19.5GHz Vs Gain Control Word

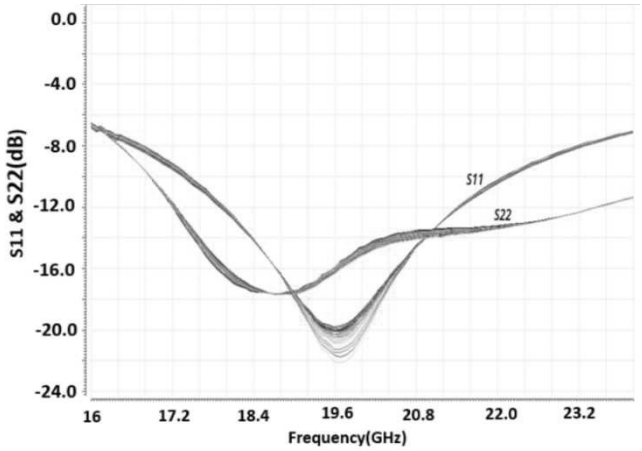

Fig. 6 Input and output return loss across all gain settings. S_{11} & S_{22} is better than -10dB for the 18-22GHz band providing 50-Ω matching.

Fig. 5 shows the gain of the VGA at 19.5GHz as gain control codes were swept. The calculated RMS gain error for VGA is 0.92dB. Fig. 5 also shows the normalized phase errors of the VGA as the gain setting is changed. The RMS phase error at 19.5GHz is 2.5º. Since the phase errors are systematic with gain control word, the calibration bits of phase shifter correct them in the full Rx chain. In a similar manner the VGA caters additional finer gain control bits (3 bits each <0.5dB) to calibrate the phase dependent gain errors of phase shifter in the Rx chain for each channel. These 3-bits also calibrate out the process related variation in the interconnection to antenna.

Fig. 6 shows the input and output matching of the VGA across all the gain states. It illustrates that the VGA matching did not change much across all the gain states and is better than 10dB for wide frequency range. Thus the input and output amplifier (Q_1 and Q_8) effectively isolate the VGA parasitic when the gain is adjusted, which confirms with the reduced phase errors observed in Fig. 5.

B. Modulated Measurements

Fig. 7 shows the VGA output when a modulated signal, 256QAM, with a bandwidth of 200MHz is injected. The EVM at the output of the VGA with the maximum gain setting is 2.44%. Measured adjacent channel power leakage (ACPR) is 30dBc, confirming that the linearity is good enough to meet EVM and carrier aggregation if needed.

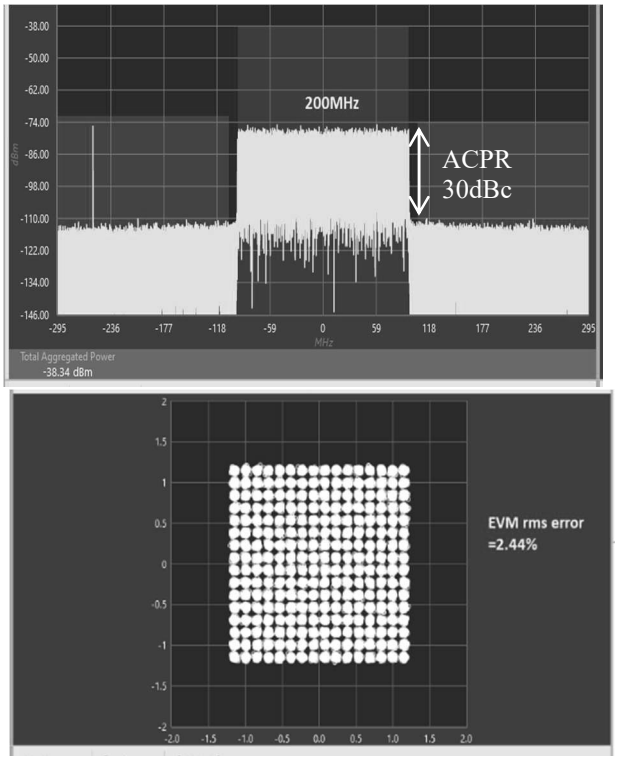

Fig. 7 Spectrum and EVM measurements with a 256 QAM modulated signal at 19.5GHz with 200MHz bandwidth. EVM =2.44%, ACPR 30dBc.

Reference	*This Work*	RFIC 2016 [2]	RFIC 2018 [3]	RFIC 2019 [4]	ESSCIRC 2016 [5]
Technology	*130nm SiGe*	130nm SiGe	65nm CMOS	65nm CMOS	130nm SiGe
Frequency (GHz)	*18-22*	28	27-42	20-43	15-39
Gain Control Range (dB)	*15.5*	18	7.5	21.5	23
Phase Error (degrees)	*<4*	<5	0.7-3.5 #	0.6-2	<3*
IP_{1dB} (dBm)	*-9.5*	-	-5.3	-16*	-
Power (mW)	*13.2*	35	15.6	30.8	104
Digital (# of bits) /Analog Control	*5bits+3 Cal. bits*	Analog	4-bits	Analog	Analog
Area (mm^2)	*0.22*	-	0.08	0.34	0.33

rms errors
* for frequencies <30GHz
[2] & [4] employs analog gain control (a DAC will be needed)

Table 1. Performance benchmarked with recently published VGAs

Table 1 compares the performance of the VGA with recently published mmWave VGAs. Proposed 18-22GHz VGA offers the lowest power consumption, highest number of control bits (5-Control bits + 3 Calibration bits) among the digitally controlled VGAs with a very comparable chip area and wide dynamic gain control range that makes it favorable for large phased arrays compared to the state of the art.

V. CONCLUSION

This paper presented a VGA operating at 18-22GHz. It had a linear in dB gain control giving it a 15.5dB control range. Consuming at a low power of 13.2mW, this VGA compares very favorably with other leading state of the art VGA designs and is being integrated with full Rx chain for SOTM phased array applications.

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