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Effect of Electrical Contact Resistance in a Silicon Nanowire Thermoelectric Cooler and a Design Guideline for On-Chip Cooling Applications

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Contact resistance gains prominence as feature size reduces to the nanometer length scale. This work studies the effects of electrical contact resistance on the performance of silicon nanowire-based thermoelectric coolers using COMSOL Multiphysics. The values of the contact resistance used to simulate the impact are experimentally extracted from a pair of thermoelectric legs with each leg made of top-down-fabricated 100 silicon nanowires having diameter of 100 nm. Analytical models agreeing well with the simulation results are provided. Lastly, a design methodology is proposed for optimum performance in on-chip cooling applications.

Key words: Silicon nanowires, thermoelectric, on-chip cooling, design

INTRODUCTION

Transistor scaling has brought about uneven heat fluxes and thermal maps along with the technical advances. In today's 32-nm technology node localized heat fluxes can surpass 300 W cm^{-2}, while for optoelectronics devices the intensity can even exceed 1000 W cm^{-2}.[1–3] High heat flux, if not removed quickly, degrades circuit performance and reliability. Thus, there is an increasing need for better, localized cooling solutions such as embedded thermoelectric coolers (eTEC). Silicon nanowire (SiNW), with its material merits and improved thermoelectric properties over bulk silicon, is a potential candidate for use in active cooling solutions.[4–6]

Recently, Zhang et al.[7,8] investigated the thermoelectric performance of SiNW using numerical simulation. However, the reported results were based on zero contact resistance (ideal case) and do not fully the scenario in the real world. While contact resistance is less of a concern for bulk material TEC (mm^2-sized contact per thermoelectric leg[9]), its impact in nanostructures cannot be underestimated.[10] Furthermore, current studies of SiNW as a good thermoelectric material are limited to the fundamental level of individual SiNW.[4–6,11] More work on SiNW-based thermoelectric devices needs to be done for the benefit of further development.

In this work, we address the effect of contact resistance in a SiNW TEC system simulated using numerical simulation software (COMSOL Multiphysics) and propose a methodology to design a SiNW eTEC. We provide analytical models incorporating the effect of contact resistance that match well with the maximum cooling and maximum heat removed characteristics. Considering its good accuracy at the micrometer length scale,[12] which is the typical SiNW length required for effective cooling, the macroscale classical heat transfer model is utilized for simulating the thermoelectric performance of SiNW. Prior to the simulation process, the electrical resistivity values of the SiNW are experimentally extracted from a SiNW-TaN/Al system fabricated using the complementary metal–oxide–semiconductor (CMOS) process, while the thermal conductivity and Seebeck coefficients are taken from acknowledged literature reported values.[5]

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EXPERIMENTAL PROCEDURES

Fabrication

Experimentally, SiNW test structures were fabricated on 8-inch silicon wafers using a top-down CMOS process.[13] To briefly describe the fabrication process, SiNWs of diameter 100 nm and pitch 400 nm were first formed via nanodot lithography and dry etch methods using SF_6. For the purpose of extracting the SiNW resistivity, two sets of test structures with SiNW length of 0.6 μm and 1.1 μm were fabricated. Corresponding scanning electron microscope (SEM) images are shown in Fig. 1a and b. Subsequently, the SiNWs were doped n-type to a concentration of $\sim 10^{19}$ cm^{-3} using phosphorus ion implantation (verified with process simulation). Thereafter, a filler material (SiO_2) was deposited between the gaps between the SiNWs, and etched back (Fig. 1c) to exposed the SiNW tips; the filler material acts as a support for the final metallization. Finally, the exposed tips were contacted with TaN/Al metallization and metal etch was performed to form contact pads with size 100 μm $\times$ 100 μm and pitch of 200 μm. A schematic of the completed test structure is shown in Fig. 1d, where two groups of SiNWs (100 SiNWs each) are electrically connected in series through the silicon substrate at the bottom, and through TaN/Al on the top.

Electrical Characterization

Next, we extracted the electrical resistivity (ρ) of the SiNW and the electrical contact resistivity (ρ_{con}) between SiNW and Al. The measured data are presented in Fig. 2. From our data, we assumed that the contacts on both sets of SiNWs were identical due to their similar geometry and processing conditions. Hence, it can be deduced that the difference in the resistance values of the two sets of SiNWs (with two different lengths) will provide the resistance of 200 SiNWs (100 SiNWs $\times$2) of length 0.5 μm (difference in SiNW length). It should be noted that the resistance of the SiNWs obtained in this manner excludes the contact resistance. A mean value of ρ was obtained as 4.7×10^{-3} Ω cm, agreeing with reported values of bulk silicon at similar doping concentration.[14] It has been presented that, at the dimensions of the SiNW fabricated in this work, the electrical properties are not affected much as compared with the thermal conductivity.[5,6] To extract the ρ_{con} of the SiNW/metal system, we next measured test structures without the SiNW on the same wafer. It was found that the substrate contribution to the total resistance presented in Fig. 2b is less than 3%. The dominant resistance comes from ρ_{con} and the SiNW; hence, a mean value of ρ_{con} of 6.1×10^{-2} $\mu\Omega$ cm^2 is extracted. It is widely agreed that the quality of a contact is a result of the control that can be achieved over the flow of charge carriers. Generally, to achieve a good contact at a metal/nanostructure semiconductor interface, heavy doping is used to ensure that the depletion width is smaller than the SiNW diameter for effective tunneling. Consequently, the doping concentration will have to be increased as the diameter of the nanowire decreases.[15] In our fabrication process, the SiNW were doped to a high level of 10^{19} cm^{-3}, and it is worth pointing out that the extracted ρ_{con} is lower than vapor–liquid–solid (VLS)-grown SiNW as reported in literature, i.e., 1.3×10^{-1} $\mu\Omega$ cm^2 to 5×10^{2} $\mu\Omega$ cm^2.[16,17] This is an indication that one could achieve better SiNW systems with the top-down approach. Nevertheless, it should be noted that the doping level in this work has not been optimized.

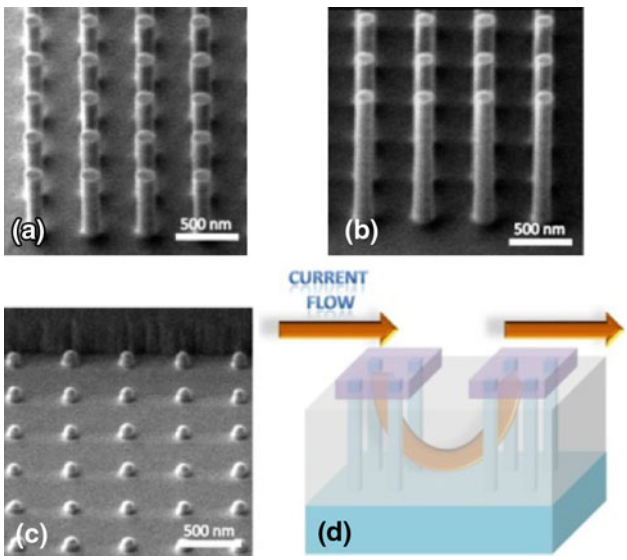

Fig. 1. (a) SEM image of SiNWs with length 1.1 μm. (b) SEM image of SiNWs with length 0.6 μm. (c) SEM image of SiNW tips exposed after SiO_2 etch back. (d) Schematic of the fabricated test structure. The two groups of SiNWs (100 SiNWs each) are electrically connected in series through the silicon substrate at the bottom, and through TaN/Al on the top; hence, the current flow direction is as indicated by the arrow.

Simulation

Based on the availability of thermoelectric properties in literature,[5,7] we designed a SiNW TEC with SiNW cross-section of 50 nm $\times$ 50 nm contacted by Al at two ends. At the SiNW-Al junction, an interface material of negligible thermal resistance was introduced to represent ρ_{con}. The values of ρ and ρ_{con} were taken from our experimental results, while the Seebeck coefficient (S = 245 μV/K) and thermal conductivity (κ = 1.6 W mK^{-1}) were taken from reported data.[5] Heat flow between the SiNW and surrounding air was considered to be through natural convection and radiation.[7,8] In addition, the hot-junction temperature was fixed at 300 K, while the cold-junction temperature (initial 300 K) was allowed to vary during operation so as

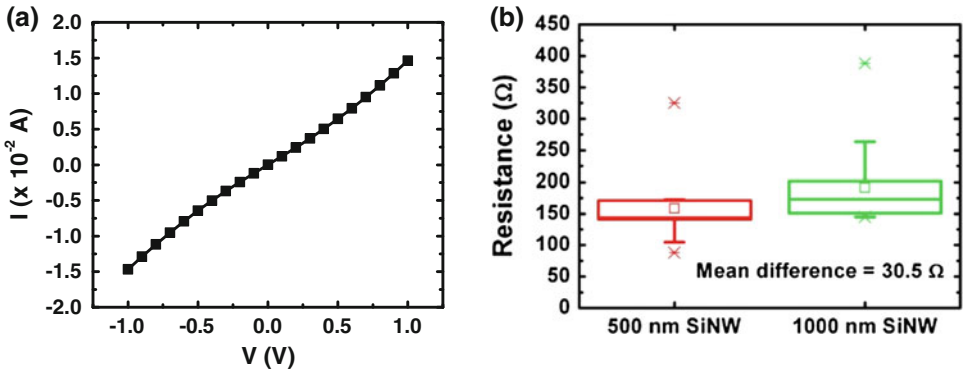

Fig. 2. (a) *I–V* measurements of a 0.5-μm-tall SiNW test structure indicating ohmic contact, and (b) box plot of the resistances obtained for SiNW test structures of two different effective lengths: 0.5 μm and 1 μm, measured over 30 dies.

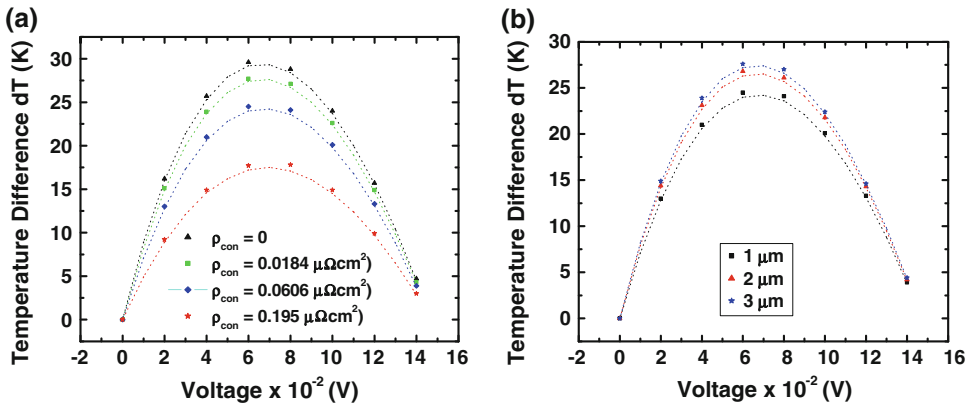

Fig. 3. Steady-state thermoelectric performance simulation: dT across SiNW versus $V_{operating}$ for: (a) varying ρ_{con} with fixed length of 1 μm and (b) varying lengths as indicated in the legend with fixed mean contact resistivity of 6.1 $\times$ 10^{-2} $\mu\Omega$ cm^2. In both cases, the optimum $V_{operating}$ to provide maximum achievable dT is 0.07 V. Symbols represent simulated data, while dotted line indicates the analytical model.

to obtain the final temperature difference (dT) between the two ends. COMSOL Multiphysics[18] was used to simulate the steady-state thermoelectric effect which is governed by Eq. (1):[7,8]

$$\nabla(-\kappa\nabla T + STJ) = J(-\nabla V), \qquad (1)$$

where J is the electrical current density and V is the electrostatic potential. In the simulation, the heat transfer module and the electromagnetic module were used to simulate the thermoelectric cooling of the SiNW. Extensive iterations in the simulation ensure the accuracy of the results obtained.[7,8] In addition, we would like to point out that the software also allows for the geometry of the SiNW and of the surrounding environment to be tailored according to the individual fabrication process scheme, thus offering flexibility. Figure 3a and b show the temperature difference (dT) across the SiNW versus the operating voltage ($V_{operating}$), with varying ρ_{con} (minimum -1.8×10^{-2} $\mu\Omega$ cm^2, mean -6.1×10^{-2} $\mu\Omega$ cm^2, maximum -1.9×10^{-1} $\mu\Omega$ cm^2) and length (1 μm, 2 μm, 3 μm), respectively.

RESULTS AND DISCUSSION

It is observed from Fig. 3a that an increase in ρ_{con} from zero (ideal case) to 1.9×10^{-1} $\mu\Omega$ cm^2 (maximum measured value) reduced the maximum dT by 35%. On the other hand, the maximum dT is found to increase with SiNW length (Fig. 3b) and thus can be used to partially mitigate the impact of high contact resistance. It is also observed that, regardless of ρ_{con} or SiNW length, the optimum $V_{operating}$ for maximum dT remained constant, which in this case is 0.07 V. We modeled the simulated results by incorporating the contact resistance term at the cold junction into the thermoelectric equation.[7,10] The modified analytical equation with electrical contact resistance can thus be written as (2)

$$dT = \frac{ST_H I - \frac{1}{2}I^2R_{leg} - I^2R_{con}}{SI + \kappa\frac{A}{l}}, \qquad (2)$$

where R_{con} is the contact resistance at the cold end, R_{leg} is the resistance of the thermoelectric leg, and T_H is the hot-junction temperature. Other symbols

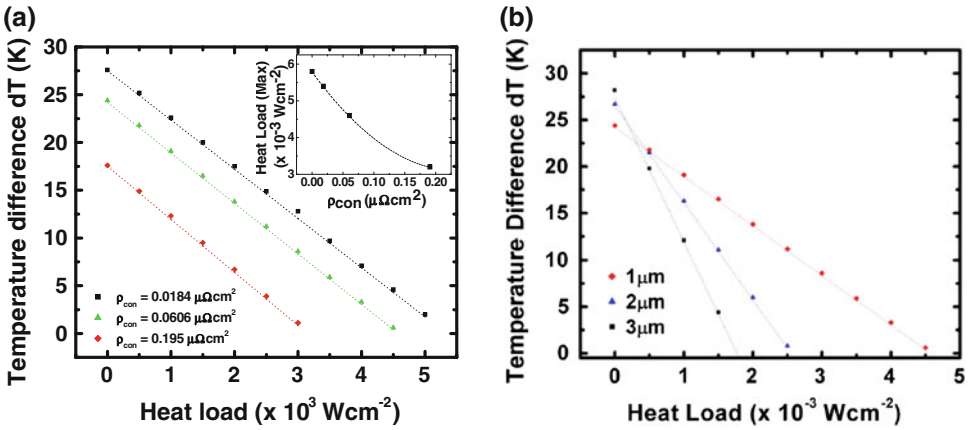

Fig. 4. dT across the SiNW versus heat load applied to the cold junction of the SiNW while operating at 0.07 V (optimum $V_{operating}$) for: (a) varying ρ_{con} as indicated in the legend with fixed length of 1 μm, and (b) varying length as indicated in the legend with fixed mean contact resistivity of 6.1 $\times$ 10^{-2} $\mu\Omega$ cm^2. Inset of both graphs shows the corresponding maximum removable heat load (reducing the maximum dT to 0 K). Symbols represent simulated data, while dotted line indicates the analytical model.

have their usual meaning, defined earlier. The term I^2R_{con} is the result of localized Joule heating caused by nonzero contact resistance. This analytical model matches very well with the simulation results, as indicated by the dotted lines (calculated from equation) in both Fig. 3a and b.

Shown in Fig. 4a and b is the cooling temperature difference per SiNW created by a single SiNW TEC versus varying heat load. Both graphs were plotted with varying ρ_{con} and length as indicated in the legend, while the optimum $V_{operating}$ used is 0.07 V. The inset of the graphs shows the maximum removable heat load (the heat load causing a maximum dT of 0 K) with respective variations (ρ_{con} and length). From the results, it is clear that the heat load removal capability is a function of ρ_{con} and SiNW length. ρ_{con} contributes to unwanted Joule heating and reduces the heat load capability; the impact is in line with the observation in Fig. 3a. It can be observed that, even though a larger maximum dT resulted from a longer SiNW, the benefits of a shorter SiNW in handling larger heat loads outweigh this. Equation (3) provides an analytical model for the heat removal capability (including ρ_{con}), agreeing well with the simulations.

$$dT = \frac{-Q}{SI + \kappa\frac{A}{l}} + \frac{ST_HI - \frac{1}{2}I^2R_{leg} - I^2R_{con}}{SI + \kappa\frac{A}{l}}, \quad (3)$$

where Q is the heat load applied to the cold side. Other symbols have their usual meanings, defined earlier. It should be noted that Eqs. (2) and (3) offer a quick estimation of the performance of a SiNW thermoelectric cooler with the inclusion of electrical contact resistance. However, to study different and/or more complicated SiNW systems, the simulation approach is a much preferred way to obtain more accurate design parameters.

In the following section, these analytical models are incorporated into a design methodology for a SiNW-based eTEC. The parameters that can be designed with flexibility are the heat load to be removed (Q), the number of thermoelectric legs, the fill factor [pitch (P) and number of SiNW (N)], and the hot spot size, The remaining parameters (S, κ, and ρ) are determined through material selection and fabrication technology. ρ_{con} is included in the design by choosing a maximum value to be on the safe side. However, considering the large statistical variation (Fig. 2b), we propose to use the central limit theorem (CLT) and select an appropriate ρ_{con} value to achieve a certain probability of success. Using the CLT, for a given probability, a suitable ρ_{con} value can be calculated using (4)

$$\rho_{con}(\text{to be used}) = z \times \sigma_{\rho_{con}}(\text{measured}) + \overline{\rho_{con}}(\text{measured}), \quad (4)$$

where the z value is related to probability and can be obtained from a Z-table. In our experiments, $\overline{\rho_{con}}$ is 6.1 $\times$ 10^{-2} $\mu\Omega$ cm^2, while the standard deviation $\sigma_{\rho_{con}}$ is 7.7 $\times$ 10^{-3} $\mu\Omega$ cm^2. With ρ_{con} (to be used) known, the corresponding maximum heat load removable per SiNW (SiNW Q_{max}) can be obtained from a heat load-ρ_{con} graph as in Fig. 4a.

Our design aims for an eTEC to handle high heat fluxes of $\sim$300 W cm^{-2}, which are typical of hotspots. Hence, for demonstration, we chose a 50-nm-wide, 1-μm-long SiNW as the material. Three critical SiNW TEC parameters are then designed: the optimum number of thermoelectric legs (No. legs$_{optimum}$), the optimum number of SiNW ($N_{optimum}$), and the optimum pitch of the SiNW array ($P_{optimum}$). They are obtained from the following Eqs. (5–7):

Table I. Calculation of parameters using the described design methodology

Selected Probability	ρ_{con} ($\mu\Omega$ cm^2) [Eq. 4]	SiNW Q_{max} (W cm^{-2}) [from Fig. 4]	Q (W cm^{-2}) [as design]	$N_{optimum}$ [Eq. 6]	$P_{optimum}$ (nm) [Eq. 7]
0.99	7.86×10^{-2}	4.15×10^3	1×10^2	1.54×10^6	321
			2×10^2	3.08×10^6	228
			3×10^2	4.63×10^6	186
0.95	7.32×10^{-2}	4.25×10^3	1×10^2	1.51×10^6	326
			2×10^2	3.01×10^6	230
			3×10^2	4.52×10^6	188
0.90	7.05×10^{-2}	4.40×10^3	1×10^2	1.45×10^6	331
			2×10^2	2.91×10^6	234
			3×10^2	4.36×10^6	192

A chip with $V_{operating}$ of 5 V and a hot spot size of 400 μm $\times$ 400 μm were considered. In all cases, the number of thermoelectric legs is fixed at 72 and thus not shown.

$$\text{No. legs}_{\text{optimum}} = \frac{V_{\text{operating}}(\text{V})}{V_{\text{optimum}}(\text{V})}, \tag{5}$$

$$N_{\text{optimum}} = \frac{Q(\text{W})}{\text{SiNW } Q_{\max}(\rho, \rho_{\text{con}})\left(\text{W/cm}^2\right) \times \text{area}_{\text{SiNW}}(\text{cm}^2)}, \tag{6}$$

$$P_{\text{optimum}}(\text{m}) = \text{hotspot length (m)} \Bigg/ \left(\sqrt{\frac{Q(\text{W})}{\text{SiNW } Q_{\max}(\rho, \rho_{\text{con}})\left(\text{W/cm}^2\right) \times \text{area}_{\text{SiNW}}(\text{cm}^2)} - 1} \right). \tag{7}$$

To better explain the methodology, in Table I we present the design parameters of a TEC operating at 5 V to cool a hot spot of fixed size (400 μm $\times$ 400 μm). The design is demonstrated with the selection of three different probabilities correlating to three different heat flux specifications (Q). Equations (4–7) are used to calculate the parameters required for the design. In all cases, No. legs$_{optimum}$ is 72. A general rule of thumb is to design for a maximum heat load Q, but operate at a lower Q in real applications.

CONCLUSIONS

We fabricated and extracted the electrical characteristics of n-doped SiNW. Through numerical simulations and analytical modeling, systematic analysis on the effect of ρ_{con} in a SiNW TEC was provided. This effect is critical to performance and needs to be considered during device design. Finally, a design methodology applicable to SiNW TEC was proposed. The design model is reasonable, offers flexibility, and provides a clear framework of operation for SiNW TEC. The use of a top-down approach allows precise control over the SiNW geometry for specific applications. With further work and verification, the issue of hot spot removal on microchips can definitely be addressed more appropriately.

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