Title
An ultrafast logic device driven by melting processes

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Abstract

The ultra-high demand for *faster* computers is currently tackled by traditional methods such as size-scaling (for increasing the number of devices), but this is rapidly becoming almost impossible, due to physical and lithographic limitations. To boost the speed of computers without increasing the number of logic devices, the only feasible solution is to increase the *number of operations* performed by a device, which is impossible to achieve using current silicon-based logic devices. Multiple operations in phase-change-based logic devices have been achieved using crystallization; however, they can achieve only the best (or fastest) speeds of several *10's of nanoseconds*. A difficulty also arises from the trade-off between the speed of crystallization and long-term stability of the amorphous phase. We overcome here the contradictory nature between the crystallization speed and long-term stability by instead controlling the process of *melting* through pre-melting disordering effects, while maintaining the superior advantage of phase-change-based logic devices over silicon-based logic devices. Multiple and low power Boolean algebraic operations, NOR and NAND, were achieved with a melting speed of just *900 picoseconds*. *Ab initio* molecular-dynamics simulations and *in situ* electrical characterization revealed the origin (i.e. bond-buckling of atoms) and kinetics (e.g. discontinuous-like behavior) of melting through pre-melting disordering, which were key to increasing the melting speeds. By a subtle investigation of the well-characterized phase-transition behavior, this simple method provides an elegant solution to boost significantly the speed of phase-change-based logic devices, thus paving the way for achieving computers that can perform computations towards *terahertz* processing rates.

Keywords
Computing, logic devices, melting, phase-change materials

Main text/body

The extremely high and ever-increasing demand for *faster* computers is currently addressed by traditional methods, such as miniaturization (in order to increase the number of devices), but this is rapidly becoming almost impossible, due to physical and lithographic constraints (1-4). The speed of computers is known to be determined almost solely by the performance of logic devices, i.e. their *speed* and *number*, which control all computations (or processes) in computers (5). The logic devices are mostly required to operate below 1 ns for achieving fast computations, and transfer information between alternate devices, such as random access memories without delays (5). To increase the speed of computers without increasing the number of logic devices, the only feasible method is to increase the *number of operations* performed by a device, which is all but unachievable using current silicon-based logic devices (6,7).

Multiple operations in a logic device are currently best achieved using devices comprised of phase-change materials – based on the reversible and multi-level switching of a phase-change material between crystalline and glassy states having a contrast in physical properties, e.g. electrical resistivity (8,9) – which can perform more than *three times* the number of operations than silicon-based logic devices (10,11). Multiple operations in phase-change-based logic devices have been achieved using crystallization; however, they can achieve only the best (or fastest) speeds of several *tens of nanoseconds* (10,11). A difficulty arises from the trade-off between increasing the speed of crystallization, and extending the long-term stability of the glassy state (12).

We overcome, here, this trade-off between the crystallization speed and long-term stability by instead controlling the processes in *melting* via "pre-melting disordering" phenomena, while maintaining the superior advantage of the phase-change-based logic devices over silicon-based logic devices. Multiple and low-power Boolean algebraic operations were achieved with ultrafast melting speeds. *Ab initio* molecular-dynamics simulations and *in situ* electrical characterization revealed the microscopic origin and transient kinetics of melting through pre-melting disordering phenomena, respectively, which were observed to be key to enhancing the melting speed, and also the melting controllability and power.

We find that Ge-Sb-Te alloys (e.g. $Ge_2Sb_2Te_5$ or GST), which are technologically important for phase-change non-volatile information storage, provide a nearly ideal system for achieving Boolean algebraic operations, and tracking transient behavior of melting or solid-to-liquid (*s*-to-*l*) transitions. This allows for the precise and systematic control of disorder in a crystalline solid via the use of a weak electric field/electrical 'priming' pulse, which is applied to a test cell, comprising a 90-nm wide cylinder of GST sandwiched between two TiW electrodes (see Methods and SI Appendix: Fig. S1). Such "priming" effects are difficult to detect through conventional material characterization, for instance electron diffraction of the gradual changes in the structure of GST caused using multiple-electrical pulses (13), but is evidenced in this study via a simple approach comprising *in situ* electrical-conductivity measurements of both pronounced and fast variations in the GST structure upon applying a single electrical pulse. Such high electrical sensitivity is the key to revealing the microscopic origin of an *s*-to-*l* transition in this material.

We have shown that a GST cell shows multiple Boolean algebraic operations via investigating its electrical conductance after the application of a "double" electrical-pulse sequence. The cell, initially in the crystalline state, was excited with the LO-LO, LO-HI, HI-LO and HI-HI pulses with and with no separation of t = 100 ns, wherein LO and HI denotes 15-ns voltage pulses of V = 0 or 1.55 V (that induces little/no change in the cell resistance through "priming") and 1.70 V (which causes moderate changes in the cell resistance via "disordering"), respectively (Figs. 1a,b, SI Appendix: Fig. S15). In an archetypical "unprimed" excitation scheme, wherein the LO pulses of V = 0 V is utilized, a single cell can exhibit only the *L-L-L-H* resistance combination resulting from the set of pulses with and with no separation (Figs. 1c,d). *L* and *H* refer to low- and high-resistance levels, which are below and above a reference resistance level, here taken to be R = 0.7 MΩ. By representing the *L* and *H* resistance levels, and the causative HI and LO pulses, as the binary numbers '1' and '0', only $\neg(x \wedge y)$/NAND operation is demonstrated (Figs. 1c, d). The single LO/HI pulses and their corresponding resulting *L*- and *H*-resistance levels can generate a $\neg x$/NOT operation (Fig. 1e). By contrast, in the "primed" excitation scheme, wherein the LO pulses of V = 1.55 V is utilized, a single cell can exhibit instead not only the *L-L-L-H* resistance combinations, but also the *L-H-H-H* resistance combinations from the same set of pulses with and with no separation, respectively, and therefore, not

only NAND operations, but also ¬(x∨y)/NOR operations are demonstrated (Figs. 1f,g), which are 100 % more than the "unprimed" excitation scheme. The single LO/HI pulses and their corresponding resulting *L*- and *H*-resistance levels can also generate the NOT operation (Fig. 1h). Such control seems to be enabled through interplay between the priming and disordering effects generated by the two distinct (LO and HI) pulses, which can produce large and diverse outcomes, that may be unachievable through archetypical means via a single (HI) pulse (see SI Appendix: Figs. S16).

The GST cells have been shown to exhibit ultra-fast and tunable Boolean algebraic operations through bolstering and controlling the interplay between priming and disordering effects. Generally, a fast crystal-to-glass transition/switching is realized through utilizing a high input energy, which promotes rapid structural disordering in GST (14-16). As predicted, in the "unprimed" excitation scheme, by increasing the HI pulses to V = 5.0 V, the GST cell can exhibit switching with minimum pulses of 1 ns (e.g. LO-HI pulses), and demonstrate the NOR and NOT operations (Figs. 1i,j and SI Appendix: Fig. S17). The reference resistance level, here is taken to be R = 0.8 MΩ. By contrast, in the "prime" excitation scheme, by increasing not only the HI pulses to the same voltage, but also the LO pulses to V = 4.6 V, the GST cell can exhibit switching instead with combined pulses of 900 ps (e.g. 400ps-500ps for the LO-HI pulses) for the same operations (Figs. 1i,j). This is not only *10 %* faster than the fastest speed achieved by the "unprimed" excitation scheme, but also *two orders* of magnitude shorter than those required to manipulate the alternative glass-to-crystal dynamics method previously used for Boolean algebraic operations in GST, and with the use of the total length of pulses as the measure of speed (10,11). Furthermore, by decreasing only the amplitude of the LO pulses, the GST cell can show a completely different NAND operation, which means that interplay between the priming and disordering effects can be controlled further through altering just the priming effects.

In addition, the energy needed to perform Boolean algebraic operations can be estimated by a simple calculation of the area under the pulse waveforms used. In the "unprimed" excitation scheme, the energy needed to switch the cell for NOR operation is given by 5.0 × 0.001t_p = 0.005t_p (e.g. LO-HI pulses), wherein t_p is defined as the time period of 1 μs. In contrast, in the "primed" excitation scheme, the

energy needed to switch the cell for the same set of pulses is given instead by (4.6 × $0.0004t_p$) + (5.0 × $0.0005t_p$) = $0.004t_p$ – *20 %* lower than the "unprimed" excitation scheme. These demonstrate the potential utility of "priming" for low power logic applications, although the device performance and (Boolean algebraic) implementation of a GST cell, such as the overall energy consumption, temporal resistance drift and sequential operation, need to be enhanced/optimized further (see Supporting Information).

We investigated the transient characteristics of an *s*-to-*l* transition occurring during the Boolean algebraic operations by evaluating the *in situ* electrical conductance of a GST cell upon electrical-pulse excitation. The cell, initially in the crystalline state, was excited with an onset voltage, e.g. V_{on} ~ 1.5 V (similar to the amplitudes of the low-voltage pulses that were key to achieving the Boolean algebraic operations in Figs. 1c and d), which induces the onset of an *s*-to-*l* transition by locally heating the material above its melting temperature, T_m, via Joule heating (17); the V_{on} value was determined via the dependence of the current flow on the constant voltage applied to the cell (Fig. 2a, top right). In general, most metals or materials exhibit a transition from the solid to liquid/melt states that yields an increase in the electrical conductivity (18,19). By applying an electrical pulse with an amplitude of around V_{on} (e.g. V = 1.47 or 1.50 V), we find that the GST cell exhibits a similar transition (as manifested by a pronounced rise in the current flow or electrical conductivity), which is mostly discontinuous-like – it does not occur instantly, but rather at longer time scales (t = 1.3 μs or 1.8 μs) (Fig. 2a, left). In addition, such a 'delay' or 'growth of disorder' prior to an *s*-to-*l* transition is not observed when either a low- or high-voltage pulse is applied (e.g. V = 1.10 or 1.90 V), i.e. the transition has not occurred or has taken place almost immediately, respectively, meaning that such phenomena occur only around T_m.

To investigate the origin of the growth of disorder, the structural disordering of a crystalline GST model at varying temperatures was examined. Recently, we have investigated such disordering essentially at and after an *s*-to-*l* transition in GST using AIMD simulations, which has provided new structural and functional insights into the microscopic processes involved (16). We illustrate the power of this approach by examining the structural changes prior to an *s*-to-*l* transition in a GST model, comprising twenty-two Ge, twenty-two Sb, and fifty-five Te atoms, heated between T

= 800 and 900 K (see Methods); these parameters were chosen based on a correlation between the temperature, size and time scale of the simulational studies (see Supporting Information). Generally, during an *s*-to-*l* transition, a sharp decrease would occur in the number of ordered structural units, *viz.* fourfold rings (which are a structural motif of the metastable rocksalt crystal structure of GST), due to the high level of structural disordering characteristic of the liquid/melt phase (19) (Fig. 2b, right). Indeed, the time evolution of the decay in the number of fourfold rings in the GST models at intermediate temperatures (e.g. T = 825 and 850 K) exhibits such transitional characteristics, but only after a (growth of disorder) time of around t = 50 ps (Fig. 2b, left), similar to those observed experimentally, although the time scale is shorter due to the small GST model employed (Fig. 2a, see also Supporting Information). Moreover, pronounced fluctuations in the number of fourfold rings are observed during the growth of disorder, suggesting the emergence of a premonitory structural disordering.

During the growth of disorder, we found that the GST model exhibits a repeated stretching or "buckling" of the bonds within clusters of atoms, *viz.* the formation and annihilation of fourfold rings (Fig. 2c), while preserving the essence of crystalline order, which is mostly independent of the model size, structural definition and starting configuration employed (see Supporting Information). We thus refer to this process as 'pre-melting disordering' (PD). Such disordering seems to be enabled by the intrinsic ability of the constituent atoms to occupy lower-coordinated sites in the liquid/melt phase than in the solid phase (20,21) (see Supporting Information). It should be noted that the PD phenomenon can be affected by the intrinsic disorder generated by thermal excitations, e.g. vibrational modes and point defects, or grain boundaries, although they should yield similar changes in the material properties that accelerate the approach to an *s*-to-*l* transition, regardless of the crystalline structure that remains until the transition itself (22,23).

The PD phenomenon allows for the precise control of an *s*-to-*l* transition in a GST model/cell. In the simulations, the preheated GST model shows a much faster onset of such a transition (t ~ 10 ps) than a non-preheated GST model when melted at T = 875 K (t ~ 40 ps); the former is preheated at T = 825 K for ~ 35 ps prior to the melting at T = 875 K, while the latter is melted solely at T = 875 K (Fig. 3a). In addition, including the preheating time, the preheated model requires an overall time

of t ~ 40 ps to complete an *s*-to-*l* transition, which is almost identical to that required by the non-preheated model, meaning that a similar transitional behavior (or outcome) can be achieved via two different excitation schemes (Fig. 3a, top right) – this can not only allow the Boolean algebraic operations, but also save energy (during preheating). The same phenomena are observed experimentally for the electrically primed and non-primed GST cells – they exhibit switching from the crystal to glass states using electrical pulses with lengths of t = 22 (7) ns including (excluding) the priming pulse, and t = 25 ns, respectively (Fig. 3b). That is, the switching speed of the cells can be altered, which confirms that such schemes could be applied to practical device operations. In addition, Figs. 3a and b show that, by preheating the models/cells using a simple priming method, the melting times can be reduced by more than *3.5 times* compared to not preheating the models/cells. Furthermore, the switching voltage (in the range V = 3.00 V to 1.55 V) and time (in the range t = 25 ns to 5 ns) decrease with an increase in the amplitude (V = 1.35 V to 1.75 V) and length (t = 5 ns to 20 ns) of a priming pulse (Figs. 3c, d). This indicates that the degree of PD can be controlled and tuned for achieving the multiple Boolean algebraic operations, and possibly even completely new applications.

Both experimental and simulational results suggest that the fast, multiple, and low power Boolean algebraic operations may stem from the cooperative movement of atoms during growth of disorder/priming, leading to a rapid, tunable, and low-energy formation of different glassy structures. At intermediate (high) temperatures, a large (much larger) buckling of bonds of clusters of atoms, evident from the AIMD simulations, will promote (boost) atomic diffusion, which is required for structural disordering. This phenomenon would explain both the observed fast switching, and also the multiple electrical-resistance levels and low power consumption seen in the GST cells.

In general, apart from the input energy, the melting kinetics of a solid depend strongly on the strength of bonds between the atoms (24), and thus one interesting avenue for future investigation might be to examine the transient behavior during an *s*-to-*l* transition of alternative solid-state or phase-change materials with different structural characteristics, which could display varying PD phenomena. Indeed, it may be fruitful to study the glassy forms of a phase-change material, where local structural variability, particularly in the strength of bonds, could yield a less pronounced T_m.

These future studies would facilitate the use of various types of materials/device structures, in isolation and in combination, to open up new opportunities for optimizing the performance of phase-change-based logic devices.

Methods

a. Cell structure

SI Appendix: Fig. S1 shows the structure of a test cell in the lateral or cross-sectional plane, wherein the cell is deposited on an SiO_2-on-Si substrate. The cell has a pore-like structure comprising a 35 nm thick phase-change (PC) material layer ($Ge_2Sb_2Te_5$ or GST), which is sandwiched between the top and bottom electrodes (TiW) with thicknesses of 200 nm. The phase-change material is confined in a 90 nm-wide via formed by an insulating layer (SiO_2) with a thickness of 35 nm. The electrodes are used to connect the cell to the external circuitry for the electrical measurements, while the insulating layer provides the electrical and thermal insulation.

b. Device fabrication

The cells were fabricated using an integrative conventional lithography and nanopatterning technique. Each patterning step was accomplished using 365 nm photolithography (Cannon) or electron-beam lithography (JEOL), followed by the material-deposition and lift-off processes. All of the materials were deposited using composite targets in a DC magnetron sputtering system (Balzers Cube). A 4-inch Si wafer with a 1 μm thick SiO_2 layer was used as the starting structure, on which a 200 nm thick TiW bottom electrode was deposited and patterned. An insulating layer, comprising a 35 nm thick layer of SiO_2, was deposited and etched to form vias with diameters of 90 nm. The vias were filled with 35 nm thick GST to form the active phase-change region. Finally, a 200 nm thick TiW top electrode was deposited to complete the structure.

c. Electrical characterization

The electrical performance of the cells was investigated using an in-house-built PC device-testing system (25) comprising a picosecond (Picosecond Pulse Labs) or nanosecond (Tektronix) pulse generator, a digital oscilloscope (Agilent

Technologies), and a probe station, as shown in SI Appendix: Fig. S2. The picosecond-pulse generator has the specifications of pulse durations ranging from 100 ps to 10 ns, rise time of 65 ps, and amplitude of 7.5 V, while the nanosecond-pulse generator has the specifications of pulse durations ranging from 5 ns to 900 ns, a rise time of less than 3 ns, and amplitude of 5 V. The cell is connected to the pulse generator and oscilloscope via low-capacitance cables (~0.2-3 pF) and a load resistor of R_l = 50 Ω. The upper limit of the time constant of the RC circuit is estimated to be ~several 10 ps.

The full-width, half-maximum (FWHM) time duration of the pulse was measured at V_{in}, and this was used to characterize the speed of switching in the PC cells. We have previously investigated and reported the waveform of the voltage pulses obtained at V_{in} and V_{out} (26). Identical to those studies, the waveform of the pulse obtained at V_{in} also reflects the exact voltage pulse that is applied to the cell, taking into account the capacitance or inductance of the probe, circuitry and connectors. The FWHMs of the waveforms measured at V_{in} and V_{out} are almost the same. In addition, as the signal measured at V_{out} has passed through the cell, the duration of the pulse experienced by the cell is almost identical to that of the pulse entering the cell. Furthermore, a comparison of the shapes of the pulses measured at V_{in} and V_{out} also show that parasitic-capacitance effects in the circuit or cell are negligible (Figs. 3a, b, S3), and in the case where they exist near the end of the pulses, they dissipate in a time with an upper limit of a few ns, consistent with those reported by other groups (27-29).

We have used one of the conventional cell structures employed by many other research groups (30,31). The pulse width needed to switch the cells via a single pulse using our present cell was found to be several tens of ns (depending on the voltage applied, see SI Appendix: Fig. S15), which is about the same as those achieved with other cells (32,33). This means that the effect of heat retention in our cells is similar to the other cells, and thereby confirms that the shorter pulse achieved via priming in this study is not affected arbitrarily by the cell structure employed, nor by its heat-retention properties.

The current flow in a cell is calculated via the voltage V_{out} probed at the bottom of the cell, and is defined by $I = V_{\text{out}}/R_l$. The length and amplitude of the electrical pulses were varied from several 100 ps to several 10 ns, and from 0 to 7 V, respectively. To ensure good functionality, the cells were switched reversibly more

than 100 times between the low- and high-resistance levels of 0.05 and 1 MΩ before the experimental study.

d. Simulational procedure

The molecular-dynamics simulations were performed using the Vienna Ab initio Simulation Package (VASP) (34). The projector augmented-wave (PAW) method (35), with the Perdew-Burke-Ernzerhof (PBE) exchange-correlation functional (36), was used. The GST models were simulated in cubic supercells with periodic boundary conditions. The plane-wave energy cutoff was 174.98 eV. All the outer *s* and *p* electrons were treated as valence electrons. The time step in the simulation was fixed at 5 fs, and the temperature was controlled via a velocity-rescaling algorithm. The density used was 6.11 g/cm^3, chosen to be between the experimental amorphous- and crystalline-phase densities of GST (37). Initial random atomic configurations were mixed at 3000 K, maintained at 1200 K for tens of ps, and then quenched to 300 K at a rate dT/dt = -15 K/ps to generate the amorphous configurations. The amorphous models were then annealed at 600 K for 500 ps to generate the crystalline configurations. To study the melting kinetics, the crystalline models were subjected to varying temperatures between 800 K and 900 K.

e. Structural characterization of the models

Based on structural motifs characteristic of the metastable rocksalt structure of crystalline GST, we studied the time evolution of structural units based on the number of fourfold rings in the model. Fourfold rings were defined when four atoms form a closed ring, with an average bond angle of 90°. A maximum deviation of +/-20° was allowed in the bond angle and in the plane angle between two parallel triangles (consisting of three atoms) that share a diagonal in the fourfold rings. Each ring, in principle, shares its four edges with four adjacent fourfold rings with an average inter-plane angle of 90°. A cut-off distance of R_{cut} = 3.5 Å between atoms was used to define these structural units.

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Author contributions

D.L., T.C.C., and S.R.E. designed the research; D.L., J.M.S., and W.J.W. performed the research; D.L., J.M.S., W.J.W., R.Z., and T.H.L. analyzed the data; and D.L., T.C.C., and S.R.E. wrote the paper, which incorporates critical inputs from all authors.

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Figure captions

Figure 1. Examples of the use of *s*-to-*l* transitions for achieving fast, low power and multiple Boolean algebraic (logic) operations in the GST cell. Waveforms for the double electrical-pulse sequence: **a)** with and **b)** without a time separation between the pulses. The dependence of the electrical resistance on the "unprimed" excitation scheme applied to the cells used to demonstrate: ¬(x∧y)/NAND operations **c)** with and **d)** without (′) a separation between the pulses, respectively. **e)** Correlation between the electrical-resistance level and the single-pulse excitation employed to achieve the ¬x/NOT operation. Using the same set of pulses, the "primed" excitation scheme can demonstrate: **f)** NAND, **g)** ¬(x∨y)/NOR and **h)** NOT operations. HI and LO refer to the voltage pulses with amplitudes of V = 1.70 V and 0 (unprimed)/1.55 (primed) V, respectively. The length of the pulses was kept constant at 15 ns, while the time separation between them, where required, was maintained to be the same at 100 ns. The reference resistance levels, R_{ref}, for the NAND and NOR, and NOT operations were chosen to be R = 0.7 MΩ and 0.3 MΩ, respectively. Truth tables for the Boolean algebraic operations are demonstrated (right of **c-h**). The HI and LO electrical pulses represent the binary numbers '1' and '0' for both inputs x and y of the Boolean algebraic operations, while the cell resistances below and above the R_{ref} values define the binary numbers '1' and '0' for the output of such operations, respectively. The error bars show the range of values obtained from experiments performed on three different cells. **i)** Plots showing the switching times achievable with different pulse voltages for the "unprimed" and "primed" excitation schemes. **j)** The tables show the electrical-resistance values of the cells measured after applying picosecond-range pulses to perform NOR (top) and NOT (bottom) operations with a time separation between the pulses. The similar **K)** plots and **L)** tables showing the switching parameters for, and electrical-resistance values measured after performing NAND (top) and NOT (below) operation via the advanced "primed" excitation scheme, respectively. The R_{ref} values for the NOR and NAND, and NOT operations were chosen to be R = 0.8 MΩ and 0.3 MΩ, respectively. The cells were switched between the low- and high-resistance levels of R = 0.05 and 1.00 MΩ, respectively.

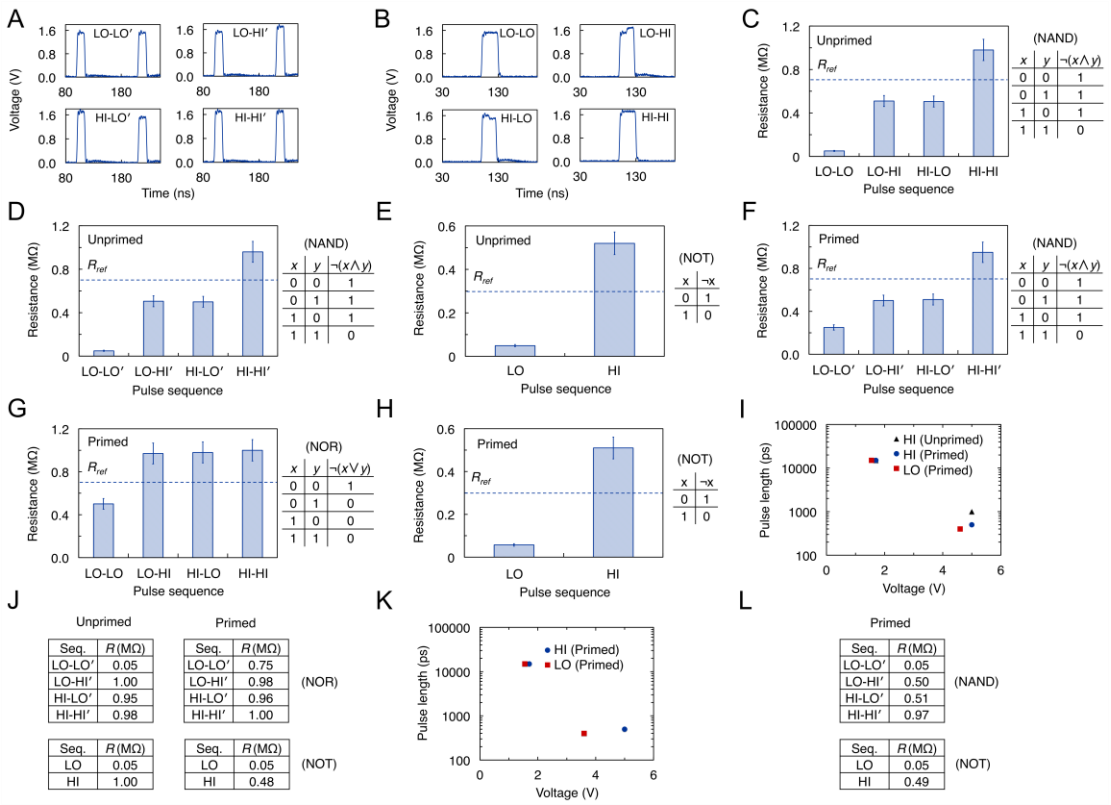
Figure 2. Experimental and simulational investigations of the origin and transience of the *s*-to-*l* transition in $Ge_2Sb_2Te_5$ (GST). a) Electrical-stimulus

excitation of a GST cell. (Left) waveforms of the current flow, I, through the cell during pulsed excitation with V_0 = 1.10, 1.47, 1.50 and 1.90 V, and t = 2 μs. (Top right) DC current-voltage (I-V) characteristics of two different cells (C′ and C″). (Bottom right) schematics of the experimental set-up employed. I is calculated as the ratio between V_1 and R_l, with the former being the voltage measured at the bottom of the cell, and the latter being the resistance of the load resistor (50 Ω). V_0 is the voltage measured at the top of the cell. The cell exhibits an initial electrical-resistance level of R = 0.05 MΩ, while the final-resistance levels shown by the cell after the pulse excitations with the V_0 values listed above are R = 0.05, 0.30, 0.50 and 1.00 MΩ, respectively. **b)** *Ab initio* molecular-dynamics simulation of a GST model. (Left) time evolution of the number of fourfold rings in the model at T = 800, 825, 850 and 900 K. (Right) snapshots of the model at T = 850 K at the positions marked x_1 and x_2. **c)** Snapshots of the GST model at the positions marked x_3 and x_4 in (**b)**. Color coding of atoms: Ge, blue; Sb, red; Te, yellow. Bonds are shown between the atoms within a range of 3.5 Å. Snapshots of the GST model at configurations marked x_5 and x_6 are given in SI Appendix: Fig. S4, and those for configurations x_7 and x_8 in SI Appendix: Fig. S5.

Figure 3. Control and tuning of the *s*-to-*l* transition via the pre-melting disordering (PD) phenomenon in GST. a) Computer simulation of the PD phenomenon in a GST model. (Left) time evolution of the number of fourfold rings in the preheated and non-preheated GST models melted at T = 875 K. The preheated model was heated at T = 825 K for two different times of t = 30 and 40 ps prior to the melting at T = 875 K, while the latter model was melted solely at T = 875 K from two different starting configurations. (Top right) overall melting process, including the evolution of rings during the initial thermal treatment of the preheated models (at T = 825 K for the two different times). (Bottom right) schematics of the heating profiles employed in the simulations. **b)** Electrical characterization of the PD phenomenon in a GST cell. (Left) Dependence of the electrical-resistance level of the primed and non-primed GST cells on the length of a switching pulse at V = 1.70 V. (Top right) complete switching scheme, but including the initial electrical stimulation applied to the primed cells with an electrical pulse of V = 1.55 V and t = 15 ns. (Bottom right) schematics of the electrical-pulse waveforms employed. Dependence of the pulse amplitude V_s and length t_s required to switch the cells on: **c)** the amplitude V_p and **d)**

the length t_p of a priming pulse. V_p and V_s were kept constant at 1.55 V and 1.70 V, respectively, when the voltage dependence was not being investigated, while t_p and t_s were both maintained to be the same at t = 15 ns when not being employed as a variable. The error bars show the range of values obtained from the experiments performed on three different cells.

Figure 1.



x	y	¬(x∧y)
0	0	1
0	1	1
1	0	1
1	1	0

x	¬x
0	1
1	0

x	y	¬(x∨y)
0	0	1
0	1	0
1	0	0
1	1	0

Unprimed

Seq.	R (MΩ)
LO-LO′	0.05
LO-HI′	1.00
HI-LO′	0.95
HI-HI′	0.98

Primed

Seq.	R (MΩ)
LO-LO′	0.75
LO-HI′	0.98
HI-LO′	0.96
HI-HI′	1.00

(NOR)

Seq.	R (MΩ)
LO	0.05
HI	1.00

Primed

Seq.	R (MΩ)
LO	0.05
HI	0.48

(NOT)

Primed

Seq.	R (MΩ)
LO-LO′	0.05
LO-HI′	0.50
HI-LO′	0.51
HI-HI′	0.97

(NAND)

Seq.	R (MΩ)
LO	0.05
HI	0.49

(NOT)

Figure 2.

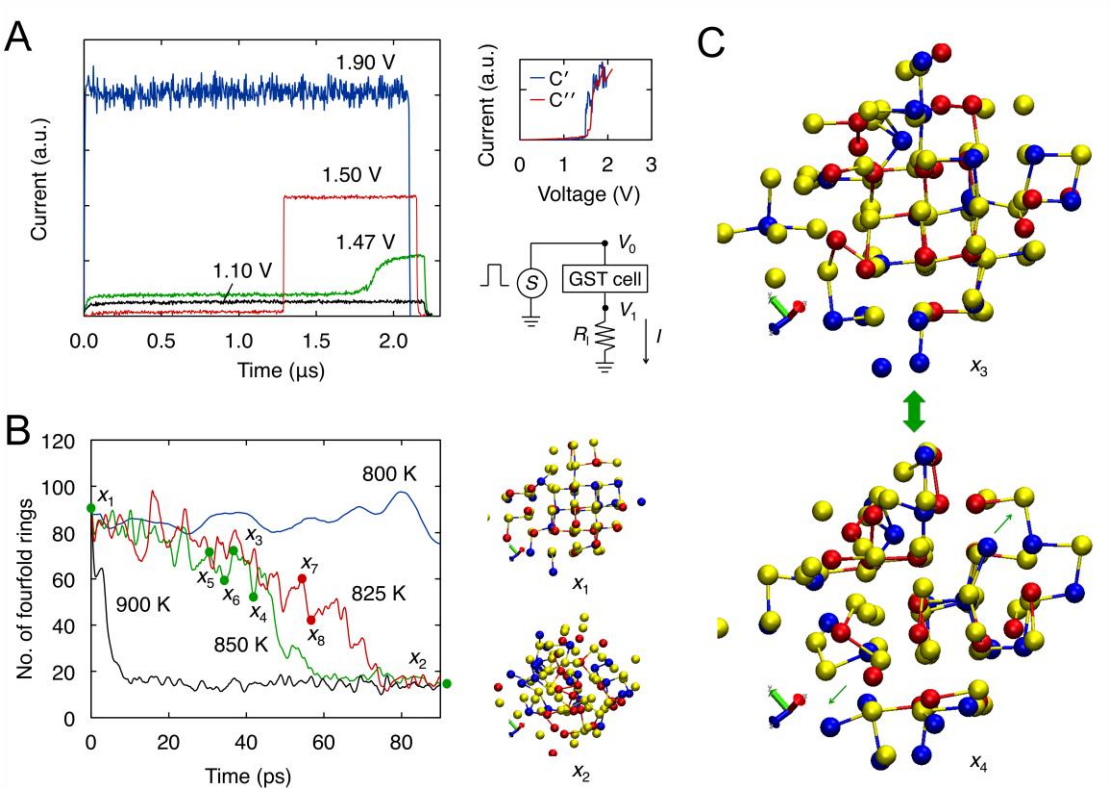
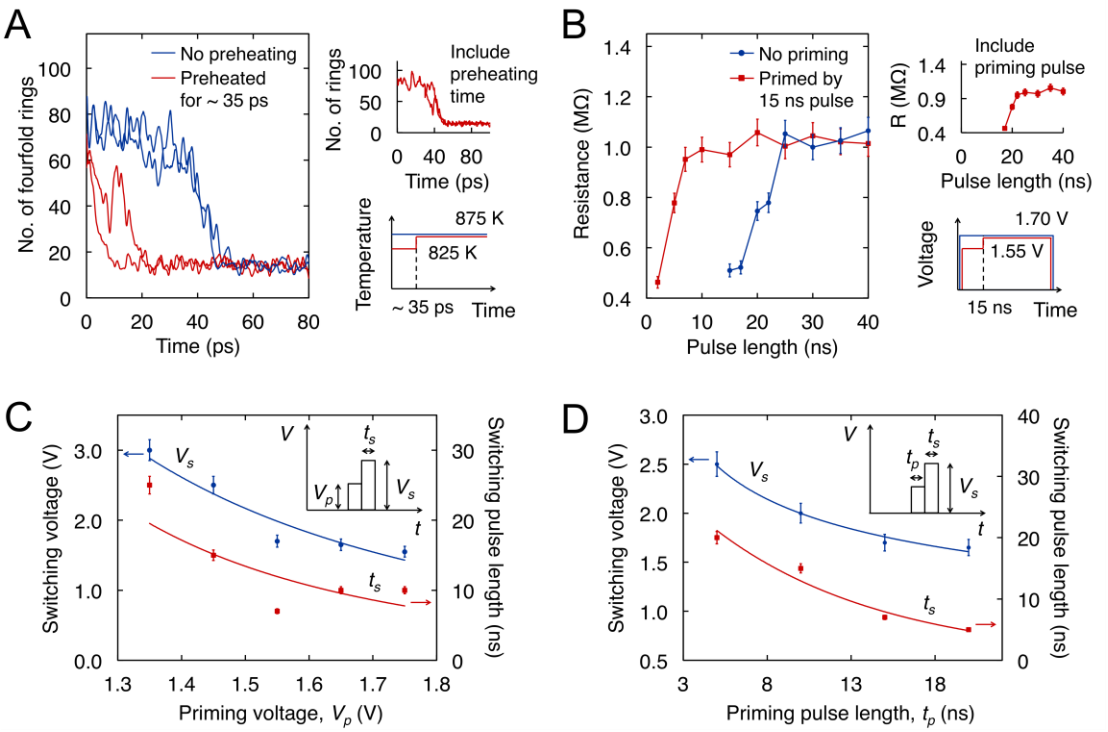

A
1.90 V
1.50 V
1.47 V
1.10 V
Current (a.u.)
0.0 0.5 1.0 1.5 2.0
Time (μs)
Current (a.u.)
C′
C″
0 1 2 3
Voltage (V)
V_0
S
GST cell
V_1
R_l
I
B
No. of fourfold rings
120 100 80 60 40 20 0
800 K
825 K
850 K
900 K
x_1 x_2 x_3 x_4 x_5 x_6 x_7 x_8
0 20 40 60 80
Time (ps)
x_1
x_2
C
x_3
x_4

Figure 3.


A
No. of fourfold rings
No preheating
Preheated
for ~ 35 ps
Time (ps)
No. of rings
Include
preheating
time
Time (ps)
Temperature
875 K
825 K
~ 35 ps
Time
B
Resistance (MΩ)
No priming
Primed by
15 ns pulse
Pulse length (ns)
R (MΩ)
Include
priming pulse
Pulse length (ns)
Voltage
1.70 V
1.55 V
15 ns
Time
C
Switching voltage (V)
Switching pulse length (ns)
Priming voltage, V_p (V)
D
Switching voltage (V)
Switching pulse length (ns)
Priming pulse length, t_p (ns)

Supporting discussion

1) Pre-melting disordering effects

Due to present limitations in the experimental studies, the information that we can obtain regarding structural distortions of crystalline clusters in $Ge_2Sb_2Te_5$ (GST) is limited. In an experimental study, it is very challenging to probe the clusters in a phase-change (PC) material, especially when their sizes are smaller than a few nanometers, e.g. via using high-resolution transmission electron microscopy (HRTEM) [S1]. The fluctuation transmission electron microscopy (FTEM) method, which employs a statistical approach to address such a problem, is also unable to provide any information on such clusters, as their actual atomic structure or distortion behavior cannot be obtained directly [S2]. Such difficulties with experimental studies are one of the key obstacles in treating appropriately pre-melting disordering phenomena in a PC material.

In a simulational study, an investigation of pre-melting disordering effects in GST is similarly a challenging task, mainly due to the simulational time involved. According to our experiments, the expected time scale of such disordering is on the order of several hundreds of ns to several μs, which is much longer compared to currently available *ab initio* molecular-dynamics (AIMD) simulation times of up to around 1 ns. Since only AIMD simulations are expected to reproduce correctly the pre-melting disordering phenomena in a PC material, faster methods, such as simulations using empirical interatomic potentials, would not help particularly in the investigation of such effects.

We have investigated the dynamical behaviour of crystalline clusters in GST during growth of disorder/priming on varying the temperatures, times, sizes, and starting

configurations of a GST model using AIMD simulations. To investigate such behavior of GST, the model was heated at $T \sim 900$ K. Because the switching effects at low temperatures were too slow to be observed, the simulations were carried out using a small GST model, comprising 22 Ge, 22 Sb, and 55 Te atoms, at temperatures between $T = 800$ and 900 K, as well as a larger GST model comprising 40 Ge, 40 Sb, and 100 Te atoms at temperatures between $T = 900$ and 1000 K. The models were further examined by varying the criteria employed for structural characterization, while the structural properties for different configurations of a model were evaluated. These are discussed and explained in the following:

a. Dependence of both time and temperature on pre-melting disordering

We studied the dynamical behavior of atoms in the GST model during the growth of disorder at different times, as shown in Fig. S4. Similar to the model for $T = 850$ K at $t \sim 40$ ps (Fig. 2b), a pronounced distortion of the structure of GST prior to an *s*-to-*l* transition is observed, as manifested by the repeated formation and annihilation of cubic clusters of atoms for the same model at $t \sim 30$ ps.

Figure S5 shows the dynamical behavior of atoms in the GST model during the growth of disorder at a different temperature ($T = 825$K). Almost the same as for the model at $T = 850$ K in Fig. 2b, a pronounced distortion of the structure for the GST model before an *s*-to-*l* transition is seen, as is evident from the repeated formation and annihilation of cubic clusters of atoms for the model at this temperature.

In Fig. S6, we studied the time evolution of the number of fourfold rings for the GST model at $T = 300$ K. Little or no distortion of the crystalline structure of GST was observed, as manifested by a relatively constant and high number of fourfold rings during the annealing of the model from $t = 0$ to 30 ps. Snapshots of the models at

regular time intervals during the annealing further show that the structure of GST is largely unchanged, and it exists mostly in a cubic-like configuration (see Fig. S7).

b. Correlation between the size of model and pre-melting disordering

Figure S8 shows the time evolution of the number of fourfold rings in a large GST model between T = 900 K and 1000 K. Such a model has been employed previously to reproduce successfully the nucleation-and-growth physics observed experimentally in GST [S3,S4]. Almost identically to the results for the small model in Fig. 2b, the model exhibits a fluctuation in the number of fourfold rings (for t = 0 to 100 ps) prior to the switching from solid to liquid configurations at an intermediate temperature (T = 975 K), although it shows both a higher initial number of fourfold rings and a longer onset time before the *s*-to-*l* transition due to the large number of atoms in the clusters.

c. Dependence of the criteria employed for structural characterization on pre-melting disordering

In Fig. S9, we investigate the time evolution of the number of fourfold rings in the model at T = 850 K as defined for different maximum deviations allowed in the bond angle and in the plane angle between two parallel triangles that share a diagonal in a fourfold ring. Similar to the model at T = 850 K with fourfold rings defined with a maximum deviation of 20° (Fig. 2b), a pronounced structural distortion of the GST model was observed prior to the *s*-to-*l* transition, as manifested by a large fluctuation in the number of fourfold rings, defined with maximum deviations of 25° and 30°, for both models at T = 850 K between t = 0 and 40 ps.

Figure S10 shows the time evolution of the number of fourfold rings for the model at T = 850 K for different maximum distances between the atoms allowed to form a fourfold ring. Almost identically to the model at T = 850 K with rings defined for a maximum distance of 3.5 Å in Fig. 2b, a large structural distortion of the GST model was observed before the *s*-to-*l* transition, as shown by a pronounced fluctuation in the number of fourfold rings for both models at T = 850 K defined with the larger maximum distances of 3.8 and 4.0 Å between t = 0 and 40 ps, although the overall ring count tends to be higher due to an increase in the number of rings formed by adjacent atoms that are located a further distance apart.

d. Correlation between the starting configuration of a model and pre-melting disordering

In Fig. S11, we investigated the time evolution of the number of fourfold rings for two GST models at T = 875 K with different initial structural configurations, M_1 and M_2, obtained via annealing two independently-quenched amorphous models for t = 500 ps. Both models show a pronounced distortion of the structure of GST prior to an *s*-to-*l* transition, as manifested by a large fluctuation in the number of fourfold rings for the GST models between t = 0 and 40 ps (Fig. S11), consistent with the ones shown by the model at T = 825 K and 850 K in Fig. 2b.

e. Dependence of the structural properties on the configuration of a model

We have investigated the structural characteristics of the GST model via calculating the average bond-angle distribution (BAD) and partial radial-distribution function $g(r)$ of the constituent atoms in the solid and liquid phases. In GST, the constituent atoms occupy mostly lower-coordinated sites in the liquid phase than in the solid phase,

characterized by a shift in the position of the first peaks in both the BAD and $g(r)$ to a larger bond angle, θ, and a shorter interatomic separation, r, respectively [S5-S8]. Similarly, the GST model exhibits such characteristics via a shift in the first peaks in the BAD and $g(r)$ to a higher θ value (θ = 90° to ~92°) and a lower r value (r = 2.96 to 2.85 Å) (Figs. S12-S13), respectively, consistent with those values reported by other research groups.

Overall, these findings confirm that the pre-melting disordering observed in the simulations is robust both to the parameters used in the simulations, and those used to characterize the models, although advanced experimental characterization tools, such as extended X-ray absorption fine structure (EXAFS) or nuclear-resonance vibrational spectroscopy (NRVS), would be helpful further to investigate pre-melting disordering phenomena in PC materials.

2) Switching characteristics

We have studied the dependence of the electrical characteristics of the GST cells on the electrical-pulse excitations applied for a fast and multilevel switching, which is described and explained as follows:

a. Constant-voltage phase transition

Figure S14 shows the dependence of the electrical-resistance level on the continuous voltage applied to the GST cells. The cells exhibit a switching from the crystal to glass states, as manifested by a pronounced increase in the resistance level from R = 50 kΩ to 1000 kΩ at V ~1.50 V.

b. Nanosecond switching

In Fig. S15, we show the correlation between the electrical-resistance level and the length of an electrical pulse applied to the GST cells at different voltages. The cells show a faster speed of crystal-to-glass transition for a higher input energy, as shown by the shorter onset pulse length (t = 20 ns to 5 ns) required to switch the cell from the low to high-resistance levels as the voltage is increased from V = 1.55 to 1.70 V.

c. Pulse-separation-dependent phase transition

The PC material exhibits structural relaxation upon melting during a crystal-to-glass transition. For an optical-pulse excitation, the final glass mark on such a material tends to be smaller than the initial melting region [S9], while its reflectivity increases with time upon melting [S10]; these observations have been attributed to the subsequent growth from the unmelted edge of the melting region and/or structural relaxation of the PC material [S9,S11]. Figure S16 shows the dependence of the electrical-resistance level of the GST cells on the separation between two electrical-pulse excitations. The cells are initially at a low-resistance level of R = 50 kΩ. In the experiments, the cells show an increase in the resistance level (from R = 50 to 200-1000 kΩ) after the application of the voltage pulses. Similar to the observations from the optical experiments, the cells show a higher structural ordering with time, as manifested by a smaller increment in the resistance level when the separation between the pulses is increased. It should be noted that the cells exhibit a lower resistance level after an excitation using the pulse sequence comprising two 1.55 V pulses than other pulse sequences, as the former sequence provides less energy to induce a crystal-to-glass transition compared to the latter sequences.

d. Picosecond switching

Figure S17 shows the correlation between the electrical-resistance level and the length of an electrical pulse applied to the GST cells at varying voltages. The cells exhibit a faster speed of crystal-to-glass transition with higher input energy, as shown by the shorter onset pulse-length (t = 800 ps to 200 ps) needed for switching from the low- to high-resistance levels as the voltage is increased from V= 3.6 V to 5.0 V.

The above studies show the electrical properties of a GST cell can be controlled and tuned to achieve fast and multilevel switching.

3) Device performance

The phase-change cell shows excellent switching performance, such as high switching speed and high read/write endurance, although one would need to reduce further the power consumption and resistance drift of the glassy state for practical device applications, which are explained and discussed in the following:

a. Power consumption

The power consumption of a PC cell tends to be high for a crystal-to-glass transition. This is due to the large energy required to melt (and then quench) the PC material in the cell. The power consumption of such cell is typically estimated by measuring the current I required to switch it from the crystalline (low-resistance) to glassy (high-resistance) states. Such a switching process is known as ‘reset’, while the reverse process of switching the cell from the glassy to crystalline states is known as ‘set’. During a cell operation, the current for reset is much higher than set, and it determines the overall power consumption. Reducing the reset current is important. This would enable the integration of a PC cell with a small Si transistor.

The reset current of a PC cell can be reduced by enhancing its thermal properties. This is achieved mostly via: i) increasing Joule heating; or ii) improving the thermal confinement of a cell.

The Joule heating in a PC cell can be increased by injecting the current through a small cross-sectional area by reducing the contact area between the PC material and electrode/heater to obtain a high current density. This has been achieved via minimizing the diameter of the electrode in a cell [S12]. The use of carbon-nanotube-based electrodes with diameters between 1 and 6 nm, for instance, has been shown to be an effective method to reduce the reset current to 5 μA [S13], sufficient for the integration of a PC cell with a sub-30 nm Si transistor [S12]. Another approach to increase Joule heating is to structure the PC material into a narrow cross section in a cell. By confining the PC material to a pillar-like structure with a diameter of 20 nm, for example, a reset current of less than 100 μA was achieved [S14]. Further improvements could be achieved by increasing the resistivity of the PC material through nitrogen or oxygen doping [S15,S16]. A highly resistive layer, such as TiON, can also be inserted between the PC material and the bottom heater to increase Joule heating in the resistive layer [S17].

The thermal confinement of a PC cell can be enhanced via increasing the thickness of the PC material. This would reduce the heat flow from the bottom electrode/heater to the top-electrode heat sink [S18], although this tends to increase the threshold voltage of a cell. In addition, a lateral-type cell structure can also be used to improve the thermal confinement of a PC cell [S19]. It benefits from having a heating zone that is separated from the electrode contacts, and a capping layer comprising a thermally-insulating dielectric. Finally, material modifications can be employed to improve the thermal-confinement of a cell. The use of alternative insulating materials, for

instance, a superlattice-like dielectric, could be used to reduce heat dissipation from the active region to the surrounding environment [S20]. It should be noted that the improved thermal isolation should not prevent the rapid quenching of the melt, and thereby inhibit the crystal-to-glass transition.

b. Resistance drift

Resistance drift is the phenomenon whereby the resistivity of the glass/ amorphous phase of a PC material increases with time. For the operation of the PC cell, the resistivity of the amorphous material is a key factor that determines its reliability [S21]. An increase in the resistivity of such material leads to a drift in the electrical-resistance level of the cell in the glass state. This problem is particularly important when groups of PC cells with multiple-resistance levels are employed, as a drift in their resistance level would lead to their states being overwritten, thus causing read errors. The origin of the resistance drift in a PC cell has been attributed to varying effects that includes the stress relaxation [S22], relaxation processes which anneal the electronic defects [S23], and the formation of valence-alternation pairs (VAPs) [S24], all of which can increase the mobility gap causing a drift in the resistivity of an amorphous PC material.

The drift of the resistance level for a PC cell is described by a power law, whereby the drift coefficient v employed as a measure of the degree of increase in resistance level is given by:

$$R = R_0(\frac{t}{t_0})^v ,$$

where R and t are the resistance and time, respectively, t_0 is an arbitrarily chosen zero time, and R_0 is the resistance at $t = t_0$.

In a PC-array implementation, a group of PC cells with multiple-resistance levels are typically employed to store information. However, resistance-drift effects tend to cause the distributions of the resistance levels or v values of the cells to shift from their initial positions after writing, and also to move further apart, thus increasing the average margin between the adjacent resistance levels over time. In addition, the spread of each distribution does not change appreciably with time. Although a reliable reading of the stored resistance levels for such PC cells can be achieved by using an adaptive writing scheme [S25], through placing appropriate reference thresholds between the distributions of the adjacent resistance levels, and adjusting such thresholds over time according to the shift of the resistance levels due to drift effects, the bit-error rate in the cells deteriorates over time. This is because the resistance-drift effect is a random process, and hence the increase in the resistance levels of each cell evolves in a stochastic manner. Hence, upon the writing of information, although the initial resistance levels of the cells are separated, some of the levels may shift closer together, and cross each other at some point in time.

To minimize the resistance-drift effects, a modular writing scheme for PC cells has been demonstrated. The concept underlying such a scheme lies in the fact that, in the majority of the cases, the relative order of the cells switched to different resistance levels does not change due to the drift behavior of a cell [S25]. In the modified writing scheme, information is written in the relative order of the resistance levels for the cells in a group that forms a so-called 'codeword'. In most cases, resistance-drift effects do not affect this ordering, and therefore information could be read correctly. By employing such a scheme, 4 levels per cell storage with a raw bit-error rate of the order of 10^{-5} was achieved in an array of 200,000 cells and maintained for over 30 days after writing at room temperature, which is more than one order of magnitude

lower than by using the former adaptive writing scheme [S25]. It should be noted that a reading error occurs when two *R* levels corresponding to two cells of the same codeword cross each other in the course of time, but as the codewords needed are usually short, i.e. a small number of cells in a group, such events are quite rare, giving rise to a low bit-error rate, although at the expense of some capacity loss. The present development of a low-redundancy, error-correction code is expected to reduce further the overall error rate towards 10^{-15}, which is required for practical device applications.

The resistance-drift effects can be further minimized via reducing the size of the PC material. Nanowire-based PC cells, for instance, show an extremely low v value due to the efficient stress relaxation from a larger exposed free surface compared with thin-film-based cells, although it would be more difficult to synthesis or fabricate these devices [S26].

Overall, it has been shown that both power consumption and resistance drift of a PC cell can be controlled and minimized accordingly, which would enable the integration of such a cell with a Si transistor or a similar switching device, and the reliable reading of the information stored in a cell, respectively.

4) Logic implementation

The PC logic devices offer new functionalities that can be exploited for next-generation semiconductor logic technologies, although it currently employs a set of operations that varies from those used in a complementary-metal-oxide-semiconductor (CMOS) logic gate, which are discussed and explained in the following:

a. Non-volatile storage

PC logic devices employ non-volatile electrical-resistance states that can be exploited to build high-density, high-speed and low-power logic chips. Such behavior would enable the development of a so-called 'universal' logic-in-memory technology, whereby a single building block could be employed for both computing *and* memory, depending on their initial configuration [S27]. This would be beneficial to achieve a standard logic circuit, whereby computing and memory are integrated in a single chip to reduce both chip footprint and interconnect delay, i.e. the area occupied by separate logic and memory circuits, and the time delay incurred in transferring information between logic and memory circuits, respectively [S28]. In addition, the non-volatile nature of a PC cell can address the issue of static power dissipation, which is one of the key concerns in complementary-metal-oxide-semiconductor (CMOS) logic. This occurs due to the sub-threshold leakage of a Si transistor when it is in an off state. To reduce the off-leakage in computing circuits, advanced technologies, such as transistors with enhanced sub-threshold slopes [S29], nano-electromechanical switches (NEMS) [S30], and tunnel field-effect transistors (TFET) [S31], are being investigated. In contrast, by being non-volatile, PC logic devices would allow the normally off (static) logic circuits to dissipate very little/no power, thus enabling ultra-low-power logic.

b. Sequential operation

PC logic devices use a sequential operation that can be exploited for complex arithmetic functions. Such operation is in contrast to the parallel operation used typically in CMOS logic gates, whereby one or more inputs are applied to a logic gate within the same clock pulse. The sequential operation is employed in PC logic

devices due mainly to the two-terminal device structure of memristors [S32]. In a worst-case operation, for instance, the NAND operation illustrated in Figs. 1b,d would require three clock pulses (prime, relax and switch), while it would need just one clock pulse in a CMOS logic gate. Although a longer time is required for PC logic devices to perform such an operation compared with CMOS logic gates, the former would occupy a much smaller chip area, since one PC cell, as opposed to four CMOS transistors, would be required.

It should be noted that PC logic devices could be employed to perform 'sequential cascading' [S33], whereby a sequence of logic operations is carried out initially from one or more binary inputs, and subsequently to one or more binary outputs. In conventional CMOS logic gates, direct cascading can be employed by connecting directly an output of a logic gate to the input of another logic gate. In contrast, PC logic devices can employ sequential cascading, whereby an output of a logic operation is used as one of the inputs of a second logic operation. This would enable the computation of complex functions, such as binary addition [S33]. It should be noted that the varying voltage levels possibly employed in such operations can be controlled via a memory controller, although it will be more complicated to program as more voltage levels are required.

c. Memristive switching

PC logic devices exhibit memristive properties that can be exploited for reconfigurable circuits. Such properties enable the realization of multiple logic functionalities, depending on its initial configuration [S33]. While CMOS logic gates depend on the topology of a gate to yield a particular functionality, i.e. the n/p-MOS layout of a NOT gate or the 4-transistor layout of NAND or NOR gates, PC logic

devices are based on memristive properties, i.e. the accumulative behavior of a PC material or cell, as shown in Figs. 1c,d, which can controlled and modified to achieve varying starting configurations, although it has a tendency to be stochastic, which can be minimized by employing a PC material/cell with a high stability of the crystalline and glassy states [S15,S16].

In addition, there is a need to increase the read/write endurance of a PC cell. During a cell operation, extensive application of electrical pulses to switch a cell between crystalline and glassy states tends to deteriorate its switching property, which leads to an eventual failure of the cell [S34]. The typical read/write endurance of a PC cell is about 10^8 to 10^{12} [S12]. Research in material and cell modifications is currently being carried out to increase the read/write endurance of such cells towards 10^{15} or more, which will be more comparable to CMOS technology.

Hence, the above discussion shows that PC logic devices form a promising basis for high-density, high-speed, low-power, reconfigurable logic circuits, which offer significant advantages over existing CMOS technologies, not least in-memory computing. Complex logic operations can also be performed via a memory controller, although they would require likely more complicated programming.

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Supporting figures

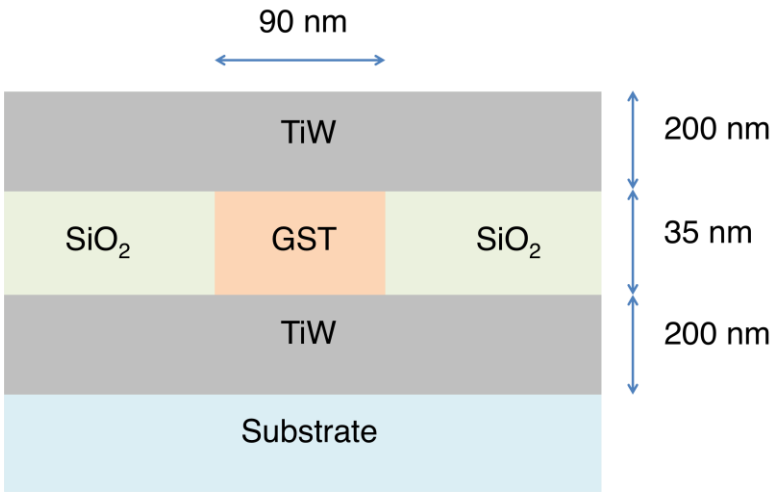

Fig. S1. Schematic of the PC cell structure. The cell was fabricated via an integrative conventional lithography and nanopatterning technique (see Methods).

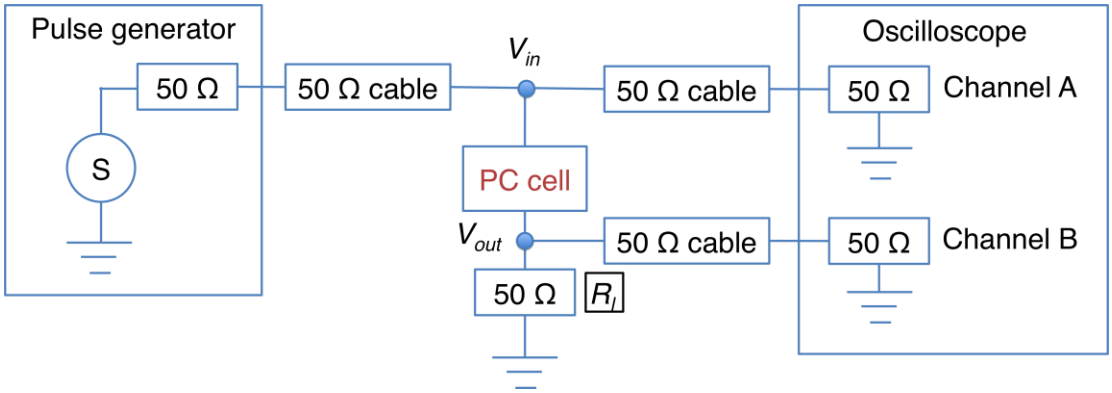

Fig. S2. Schematic of the PC device measurement setup. V_{in} and V_{out} are probed at the top and bottom of the cell, respectively.

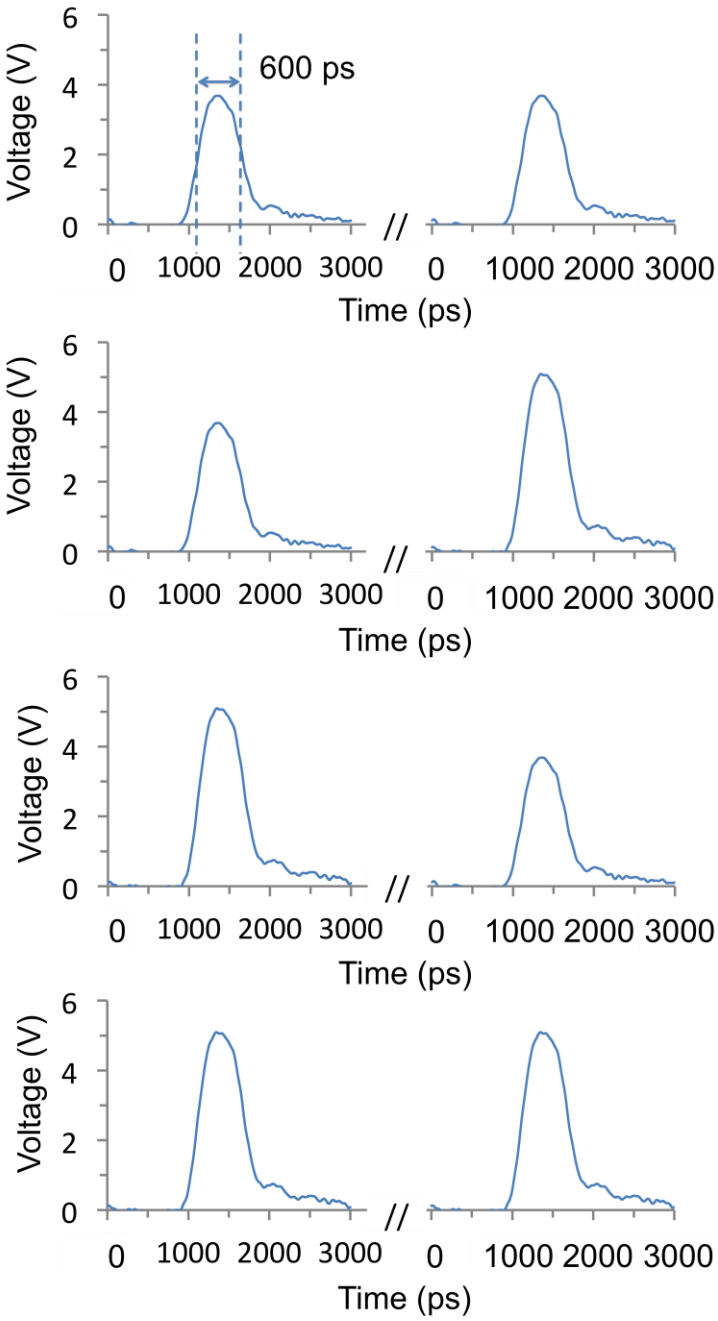

Fig. S3. Waveforms of the double-electrical pulses applied to the PC cells in the picosecond switching experiments. The break in the x-axis corresponds to a separation between the pulses that is kept constant at t = 100 ns.

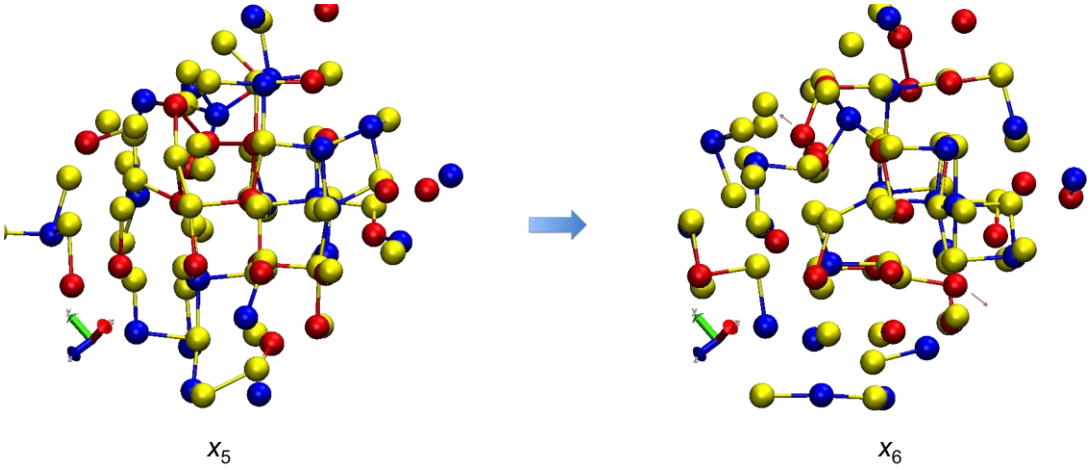

Fig. S4. Snapshot of the GST model at T = 850 K corresponding to the positions x_5 and x_6 in Fig. 2b. Bonds are shown between the atoms within a range of 3.5 Å.

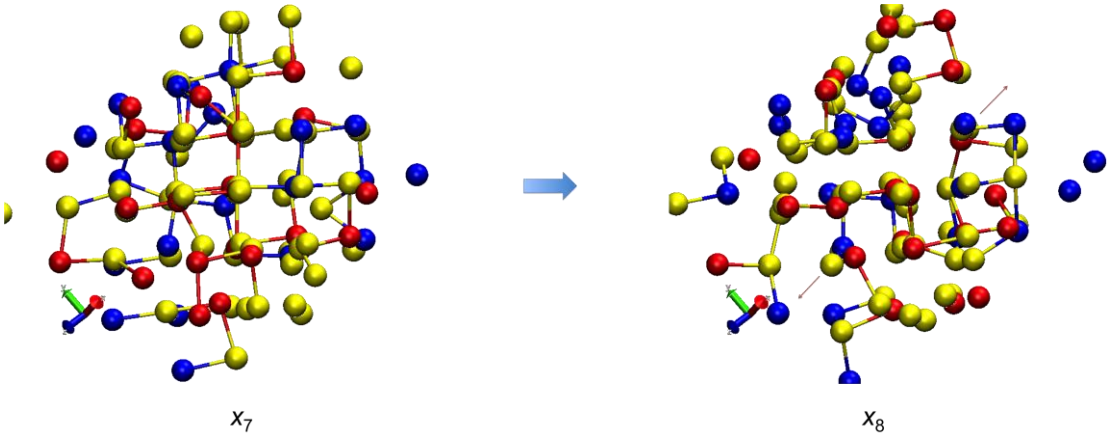

Fig. S5. Snapshots of the GST model at T = 825 K corresponding to the positions x_7 and x_8 in Fig. 2b. Bonds are shown between the atoms within a range of 3.5 Å.

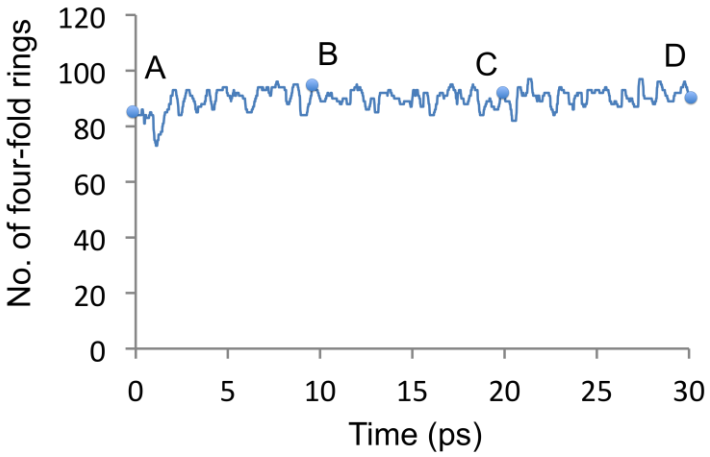

Fig. S6. Time evolution of the number of fourfold rings for the GST model at T = 300 K.

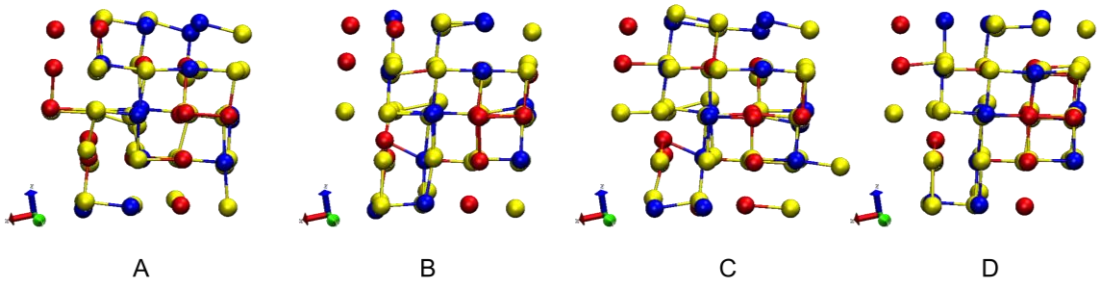

Fig. S7. Snapshots of the GST model at T = 300 K corresponding to the positions A, B, C and D in Fig. S6. Bonds are shown between the atoms within a range of 3.5 Å.

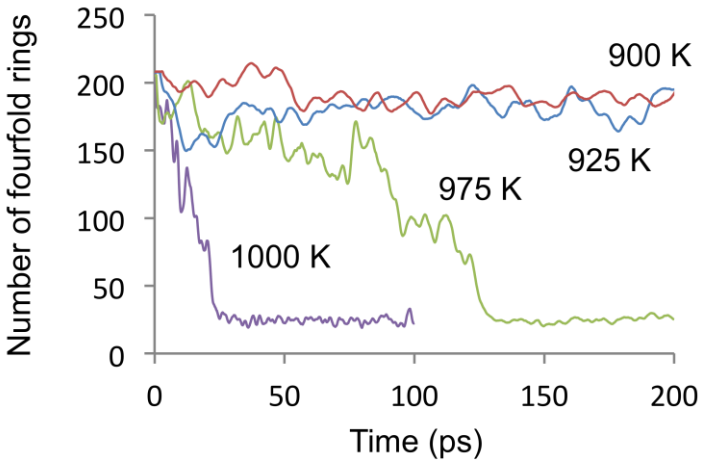

Fig. S8. Time evolution of the number of fourfold rings in the large GST model at varying temperatures.

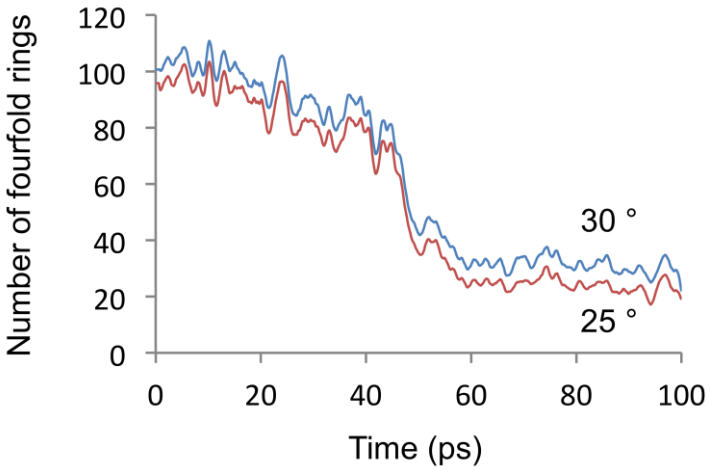

Fig. S9. Time evolution of the number of fourfold rings in the GST model at T = 850 K, calculated with varying maximum deviations allowable in the bond angle and in the plane angle between two parallel triangles (consisting of three atoms) that share a diagonal in a fourfold ring (see Methods).

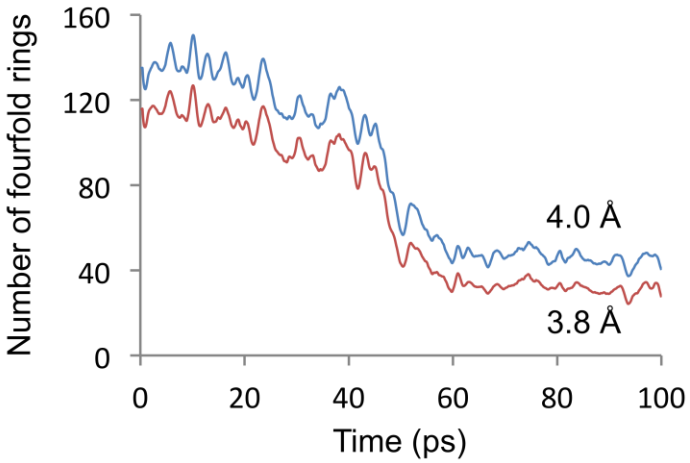

Fig. S10. Time evolution of the number of fourfold rings in the GST model at T = 850 K, calculated with varying bond cut-off distances.

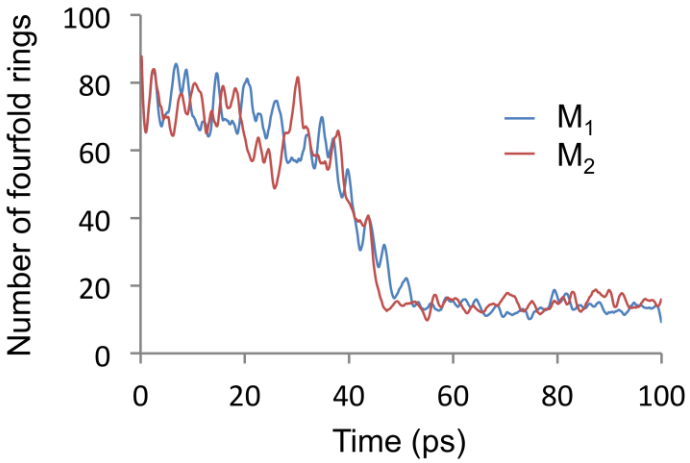

Fig. S11. Time evolution of the number of fourfold rings for the GST model at T = 875 K with varying starting configurations.

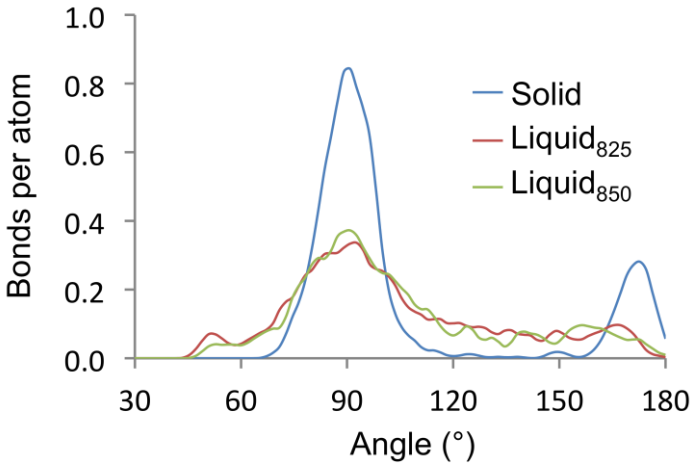

Fig. S12. Average bond-angle distribution for the constituent atoms in the GST model in the crystal and liquid configurations (T = 825 K and 850 K). Bonds are calculated between atoms within a range of 3.5 Å. The model was relaxed at T = 0 K prior to the calculations.

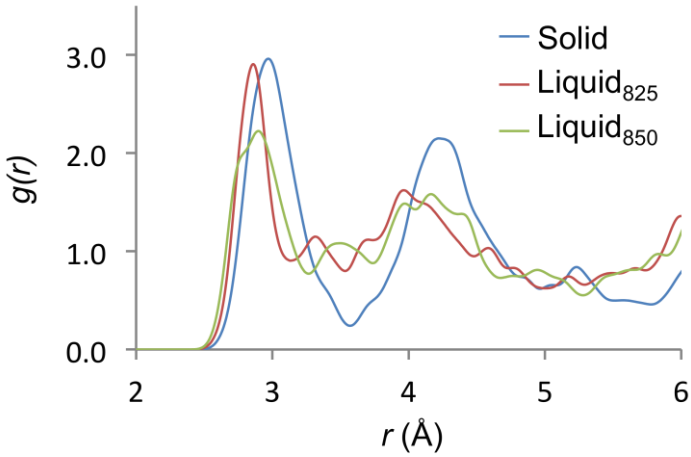

Fig. S13. Total partial-radial distribution functions for the constituent atoms in the GST model in the crystal and liquid configurations (T = 825 K and 850 K). The model was relaxed at T = 0 K prior to the calculations.

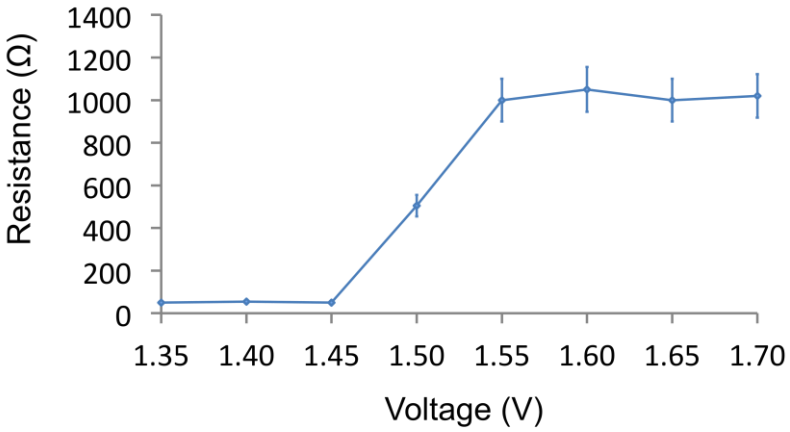

Fig. S14. Dependence of the electrical-resistance level on the constant voltage applied to switch the PC cells. The error bars show the range of values obtained from the experiments performed on three different cells.

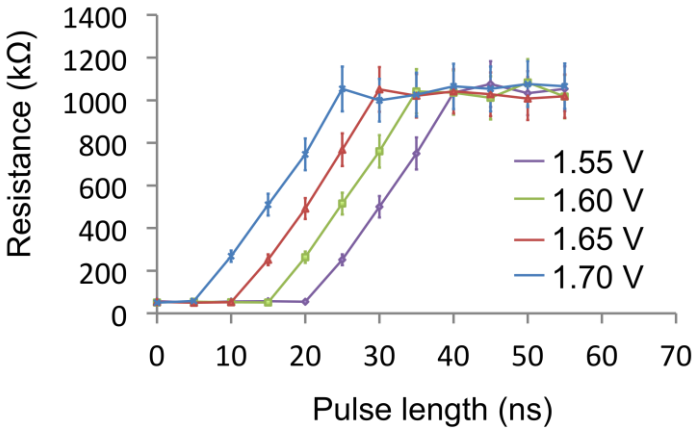

Fig. S15. Correlation between the electrical-resistance level and the pulse length applied to switch the PC cells for varying switching voltages. The error bars show the range of values obtained from the experiments performed on three different cells.

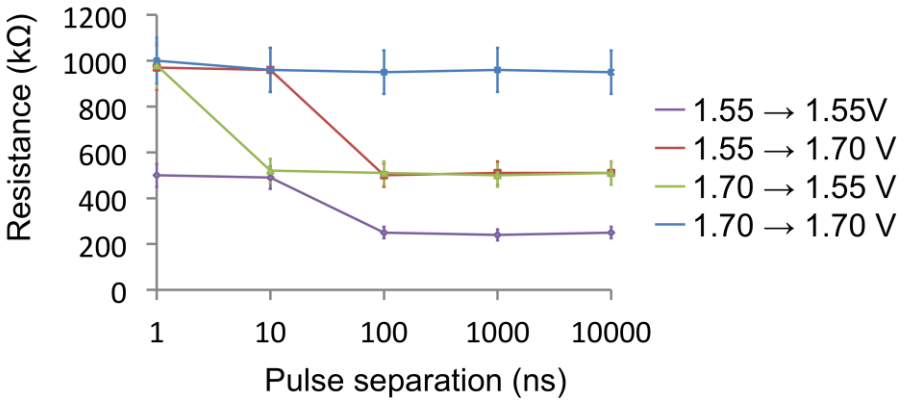

Fig. S16. Dependence of the final electrical-resistance level on the separation between the pairs of pulses employed to switch the PC cells. The error bars show the range of values obtained from the experiments performed on three different cells. The pulse length was kept constant at t = 15 ns. The cells are initially at a low-resistance level of R = 50 kΩ. In the experiments, the cells show an increase in the resistance level (from R = 50 to 200-1000 kΩ) after the application of the voltage pulses. However, the increment in the resistance level becomes smaller as the separation between the pulses is increased. It should be noted that the cells exhibit a lower resistance level after an excitation using the pulse sequence comprising two 1.55 V pulses than other pulse sequences, as the former sequence provides less energy to induce a crystal-to-glass transition compared to the latter sequences.

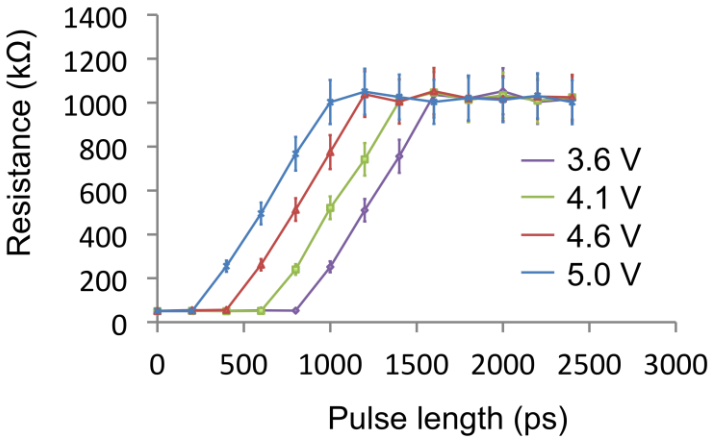

Fig. S17. Correlation between the electrical-resistance level and the length of single voltage pulses applied to switch the PC cells, within picosecond time scales. The error bars show the range of values obtained from the experiments performed on three different cells. The cells are initially at a low-resistance level of R = 50 kΩ. In contrast to Fig. S16, it should be noted that the cells show a general increase in the resistance level as the length of the pulses is increased until it reaches the high-resistance level, due mainly to the higher energy provided by the voltage pulses to induce a crystal-to-glass transition.