Low Thermal Budget Fine-pitch Cu/Dielectric Hybrid Bonding with Cu Microstructure Modifications

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***Abstract*— Advanced packaging featuring vertical integration has emerged as a crucial technology facilitating high performance, low power consumption, and compatibility for heterogeneous integration. Metal/dielectric hybrid bonding stands out as a pivotal technique enabling the vertical stacking of multifunctional components. However, certain applications, such as memory stacking, demand specific low-thermal budget processing. Although new dielectrics like SiCN are promising for reducing the thermal budget of dielectric-to-dielectric bonding interfaces, the formation of metal/Cu-Cu interconnects requires a higher thermal budget. Consequently, the overall thermal budget for Cu/dielectric hybrid bonding exceeds 350 °C. This paper aims to achieve Cu/dielectric bonding at a lower thermal budget of ⩽ 250 °C. This goal is accomplished by modifying the Cu microstructure through grain size variation employing the modifications into the conventional damascene process flow or with a combination of both. Systematic investigations in Cu dishing, by comparing the proposed methods to the conventional damascene flow reveal no variations with the chemical mechanical planarization (CMP) process. Furthermore, grain modifications with high <111> oriented Cu were investigated by altering the plating parameters without special chemistry or by using an alternate deposition method. The scanning electron microscopy-electron backscatter diffraction (SEM-EBSD) is utilized for understanding the Cu microstructure modifications. Interface characterization demonstrates significant enhancement in bonding interface grain growth with our proposed methods, leading to low thermal budget Cu/dielectric hybrid bonding.**

Keywords— Cu Grain modification, hybrid bonding, low thermal budget

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I. Introduction

Emerging technologies such as high-performance computing (HPC), 5G, autonomous vehicles, Internet of Things (IoT) devices, and virtual/augmented reality are increasingly shaping consumer demands. These innovations require high-performance, energy-efficient chips capable of handling vast amounts of data quickly [1]. While Moore's Law [2] has traditionally driven chip performance through device scaling, progress has slowed due to limited technological advancements, hindering the integration of all functionalities into a single chip footprint [3]. To overcome these constraints, there is a push for innovation in backend technology, involving the integration of multiple chips into a single package. Advancements in packaging technology, particularly vertical integration, are crucial for achieving high performance, low power consumption, and compatibility for heterogeneous integration [4]. Wafer bonding plays a pivotal role in vertically stacking multifunctionalities, necessitating higher interconnect density, especially for applications like CMOS image sensors (CIS) [5]. Metal/dielectric hybrid bonding technology is emerging as the solution for achieving higher interconnect densities [6]. Moreover, memory stacking applications require low thermal-budget hybrid bonding to mitigate memory losses and minimize stress in thin films caused by high process temperatures. In addition, lowering the thermal budgets will also help reduce the warpage/bow and thermal stress effects for stacked dies, increase the throughput at a lower cost, and minimize the delamination at the interface layers in the active device region [7]. Industries are exploring alternative dielectrics like SiCN to reduce thermal budgets in dielectric bonding [8]. However, the overall bonding thermal budget remains high (>350°C for a few hours) due to Cu-Cu interconnect formation, with challenges

such as Cu surface oxide formation and Cu to oxide dishing [9]. Various methods such as thermocompression bonding with surface passivation, ultra-high vacuum bonding, and surface activation have been proposed to address Cu thermal budget issues, yet achieving damascene compatibility remains challenging [10-13]. Although the damascene-compatible nano-twinned copper (nt-Cu) process shows promise, industry adoption is hindered by complex plating chemistry and process times [14]. Apart from this, as from Harrison's classification [15], Cu grain boundary diffusion is higher than compared with lattice diffusion coefficient in the face-centered cubic (FCC) structures and will be enhanced with high <111> oriented Cu. The higher diffusion enhances the grain growth at the bonding interface.

In this endeavor, the effect of Cu microstructure modifications in achieving the reliable Cu-Cu interconnect at Cu/dielectric hybrid bonding, at a lower thermal budget of $\leqslant$ 250 °C has been investigated. The detailed surface and interface characterization has been examined in the following sections.

II. Fabrication Protocol

A. *Wafer preparation and modification to the conventional damascene process*

The entire experimental investigation was done with the 300 mm process line. P-type, double-side polished Si wafers have been used for this study. Before processing these wafers a standard cleaning has been implemented. The damascene process has been well adopted for the preparation of the Cu/dielectric hybrid bonding surface. Fig. 1(A), and 1 (B) show the schematic of the conventional and proposed approaches of the damascene process. These various process sequences and their fabrication methods, numerous process and inspection tools have been utilized as follows. The dielectric layer deposition using the PECVD process, PR coating, and development using SUSS track and exposure using ULTRATECH stepper tools. The stepper mask has been designed with a 6 µm pitch with a 3 µm pad size most of the die and small test structures of 10 µm pitch with a 3 µm pad, with a total pattern density of ~ 16%. Following, the capacitive coupled plasma (CCP) etch tool was utilized for dielectric layers etching, and an in-house PR stripper for PR removal on the dielectric. Afterward, the PVD process was utilized for depositing the barrier and Cu seed layer respectively, Following, the trench filling with electrochemical plating/deposition was done using the ECD tool. The resulting Cu overburden followed by barrier layer removal has been removed by polishing with the CMP tool, with endpoint detection method. Towards the assessment of Cu dishing and surface roughness, a fully automated inline atomic force microscopy (AFM) – InSightAFP by Bruker, has been utilized. The bonding process with precise alignment was carried out using the EVG Gemini FB XT tool. The bonded wafer annealing was carried out using the SPTS vertical batch process annealer. The bonded wafer inspection using the confocal surface acoustic microscopic image (C-SAM) has been utilized, following its bond strength measurement carried out with Maszara's blade testing using the EVG 20. Following, for interface inspection the samples are prepared with a Disco dicing tool and its inspection using high-resolution microscopes supplied by ZEISS / JEOL focused ion beam scanning electron microscopy (FIB-SEM). The Cu grain study investigation utilized a FIB followed by electron back-scattered diffraction imaging (EBSD) imaging.

In the conventional and proposed approaches, the schematic (a-c) suggests the dielectric deposition, pattern using stepper and etch the dielectric. The following (d-f) shows the barrier layer, Cu seed layer deposition, and Cu electroplating. In the proposed approach, the Cu deposition has been modified using changes to the ECP parameters or alternate filling method, shown in Fig 1(B) (f). Also, the post-trench fill annealing in the proposed approach is eliminated or optimized. Following the Cu overburden and barrier layer removal using CMP, then wafer bonding as shown in (h-i). The effect of these modifications on the conventional damascene process flow has been discussed in detail in the following sections.

III. Results and Discussion

A void-free bonding interface is necessary for reliable interconnect formation across the hybrid bonding interface. However, attaining a low thermal budget in terms of Cu

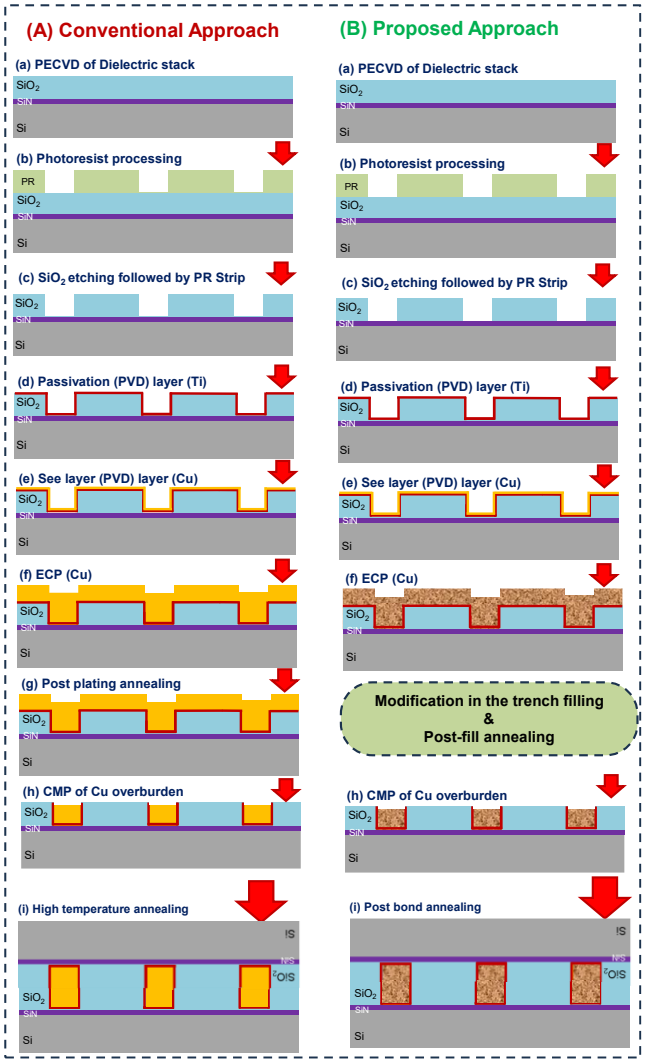

Fig.1. Schematic of damascene process fabrication (A). Conventional approach, (B). Proposed approach.

interconnect is challenging. It is due to its rapid formation of surface oxide and surface dishing resulting after the CMP process [16-18]. Fabricating the Cu structure with more thermal expansion could be one of the solutions for lowering the Cu - Cu interconnect thermal budget, explained in detail as follows.

A. Effect of post trech fill annealing.

As with the conventional damascene process, it was observed practice of annealing after electroplating. Mirkarimi, Laura, et al. [19], proposed to anneal the post plate annealing to 120 ˚C for 60 min, and 200 ˚C for 10 min by C.H. Seah et al. [20]. However, the Cu grain structure and enhancement of the grain growth could happen even at room temperature and is more rapid at high temperatures [21]. After annealing of ECP films followed by CMP resulted in a dishing of Cu, needs to be controlled to a limit of less than a few nm, due to no further expansions of the Cu at low thermal budgets. Fig. 2 shows the effect of the annealing after the ECP process. To understand the grain growth before and after annealing an X-SEM with EBSD analysis was performed. Fig. 2(a) shows the EBSD and band contrast of the Cu pad after the ECP process followed by CMP, and Fig. 2(b), after annealing to 200 ˚C for 1 hr. It suggests a significant grain growth of post-plating annealed Cu as compared with the pre-annealed Cu.

B. Effect on Cu dishing.

The Cu-to-dielectric dishing is a crucial factor in the formation of a void-free bonding interface. The wafers with/ without post-plating annealing are subject to the CMP with the same polishing slurry and polishing recipe. To investigate Cu dishing formation, an AFM inspection was conducted at specific locations on both types of wafers using an automated AFM tool, as shown in Fig. 3. The inspection focused on two specific locations at the wafer center (C1, E1) and two more at

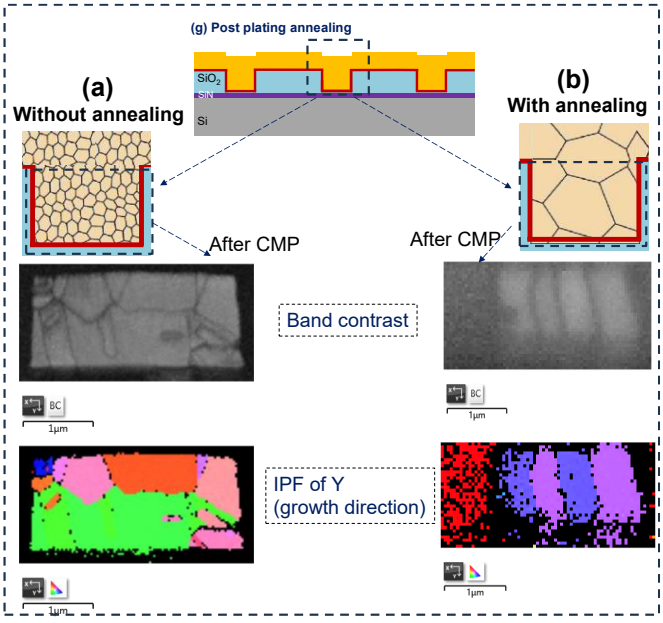

Fig. 2. The effect on electroplated Cu in damascene process with its band contrast and EBD inverse pole figure (IPF) images. (a) without annealing. (b). with annealing.

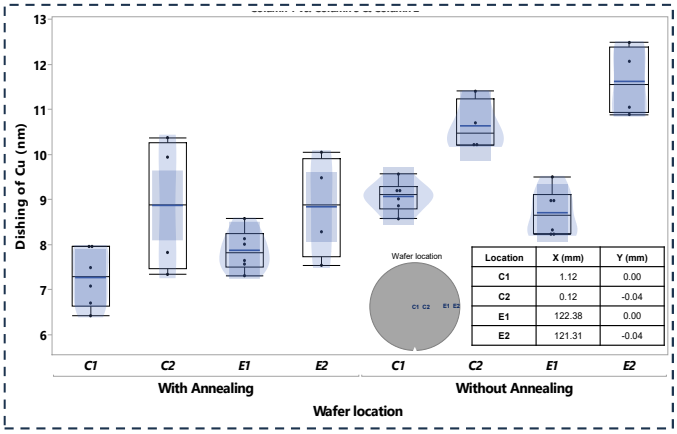

Fig. 3. The AFM surface morphology (Cu dishing) inspection of Cu/dielectric among various substrates of center and edge locations (updated in table) with and without post-ECP plating annealing.

the wafer edge (C2, E2), with pad sizes of 3 µm and pitches of 6 µm (C1, E1) and 10 µm (C2, E2). The resulting Cu dishing on the Cu/dielectric surface measured approximately 8nm ±3 nm on both types of wafers, indicating no significant difference in Cu dishing between annealed and non-annealed wafers. However, variations in dishing were observed between C1 and C2, as well as E1 and E2, attributed to slight changes in pattern pitch from 6 µm to 10 µm, increased dishing with increased pitch even though the pad size is constant. It confirms the pitch dependency of the CMP and necessitates uniformity in pad and pitch designs to avoid non-uniformity in the CMP.

Additionally, surface roughness was observed on both Cu and dielectric surfaces, measuring 2 µm × 2 µm. The average root mean square (RMS) roughness on the dielectric surface was higher on non-annealed wafers compared to annealed wafers, although remaining below 0.3 nm across all wafers. Similarly, the average RMS roughness on Cu pads was lower on non-annealed wafers compared to annealed wafers, potentially due to increased grain sizes in the annealed samples.

C. Bonding interface inspection

The wafer bonding among the wafers with post-plating annealed and without post-plating annealing has been performed separately. Before bonding, these wafers are treated with N_2 plasma, followed by DI water rinse. Post-bonded wafers are annealed at ≤ 250 ˚C, 2hr in N_2 atmosphere. To understand the effect of the proposed approach to the conventional approach on bonding interface formation, an interface characterization has been performed. Fig 4 (a,b) shows the C-SAM interface inspection of the bonded wafers with and without post-ECP annealing respectively. It suggests a more than 90 % bonding yield without any interface voids suggesting no major interface voids due to the degas or particles. However, the white contrast has been observed at the bonding interface in Fig 4 (a) and is subjected to wafer handling, but not due to the particle/polymer defects. Following, the dicing of 10 mm × 10 mm was processed to check the delamination or chip-off of the bonding interface, however, no such scenarios have been observed as shown in

Fig. 4 (c, d), suggesting a very highly reliable bonding interface in both the cases. It can be correlated to the higher dielectric bonding area (~84 %) of the hybrid bonded wafers [22,23].

In addition, the bonding interface using the FIB-SEM inspection reveals that the voids at the bonding interface with the distinguishable bonding interface in the case of annealed samples as shown in Fig. 4(e), on the other hand, a non-distinguishable and higher grain grown Cu across the bonding interface as shown in Fig. 4(f).

The investigations suggest that the effect of grain size is also a critical factor in enhancing the Cu interconnect formation at the lower thermal budgets.

D. Fabrication of smaller grain structures

Efforts were made to produce smaller grain copper with a pronounced <111> orientation by optimizing plating parameters rather than altering the chemistry. These parameter adjustments encompass variations in current density (expressed in amperes per square decimeter, ASD), duty cycle or current pulsing, and wafer rotations per minute (RPM). Figures 5(a) to (c) present electron backscatter diffraction (EBSD) inspections conducted on the cross-section of the copper pad under different plating conditions aimed at modifying grain sizes. Figure 5(a), characterized by higher RPM (accompanied by higher current density, no duty cycle, and ambient temperature), indicates that despite initial growth yielding smaller-grain copper, grain size increased progressively with growth, accompanied by a minor prevalence of <111> oriented planes. Conversely, heightened current density (no duty cycle, lower RPM, and ambient temperature) as depicted in Figure 5(b), resulted in the absence of smaller grains, with minimal <111> oriented planes observed. Upon increasing the duty cycle to a higher range (alongside higher current density, lower RPM, and ambient temperature), a larger copper grain with a predominant orientation lying between <101> and <111> emerged, as illustrated in Figure 5(c). It has been recognized that achieving the desired copper microstructure without altering the plating chemistry may pose challenges. Consequently, Fig. 5(d) shows an ECP-free filling of the trench using the PVD process that has been explored and

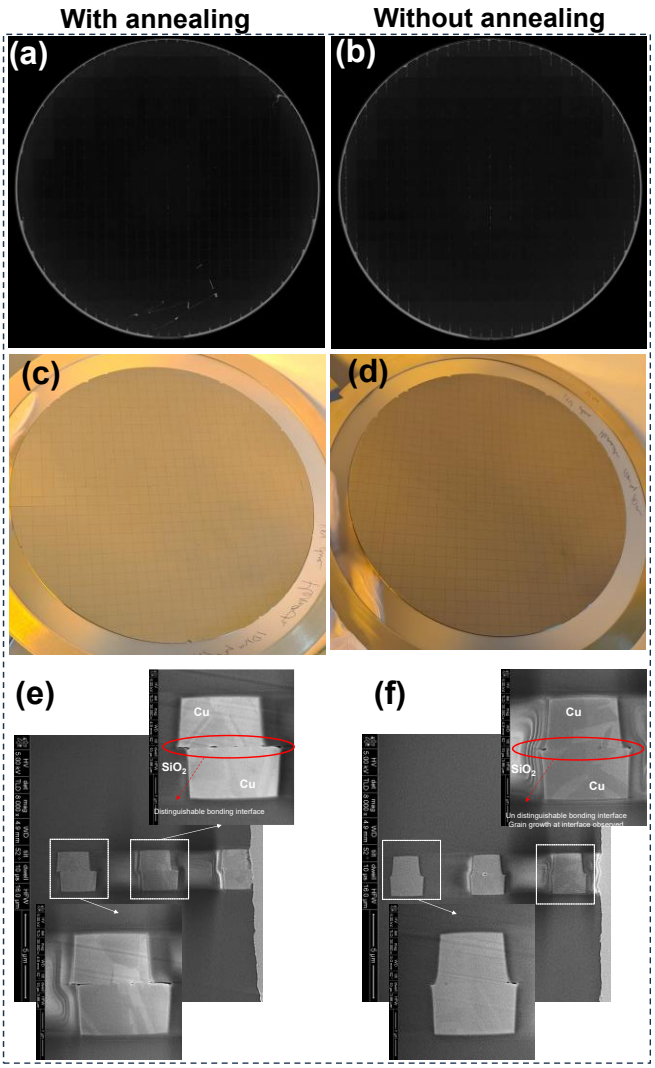

Fig. 4. Interface inspections of the processed damascene process with and without post-ECP anneal. (a,b). C-SAM interface inspection. (c,d). 5mm X 5mm dicing. (e,f). FIB-SEM of at the Cu/dielectric interface.

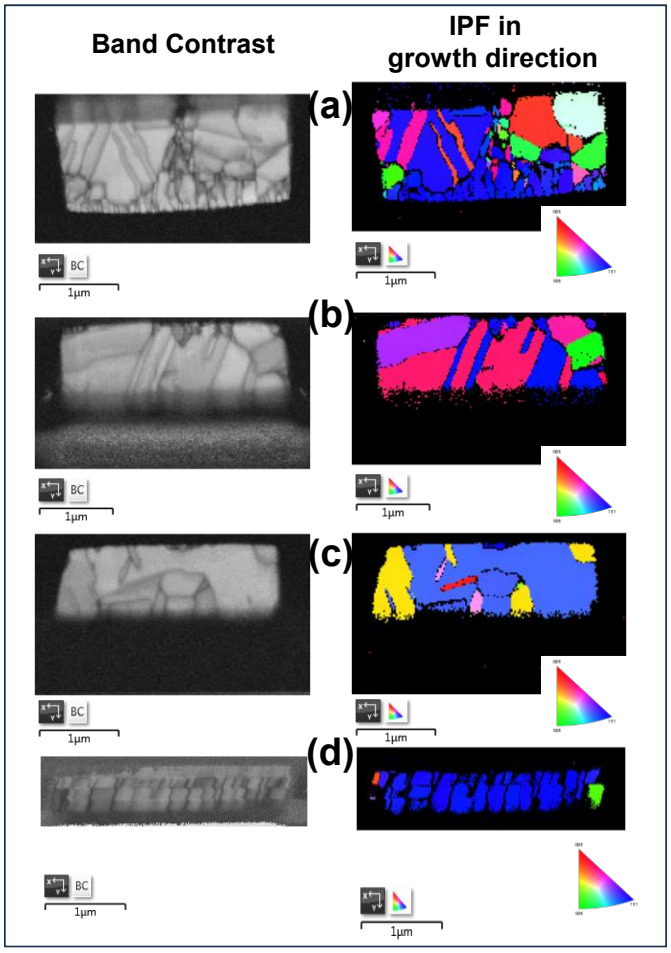

Fig. 5. EBSD on the cross-section of the Cu pad using ECP process at, (a) Change in RPM. (b). Higher current density. (c). Higher pulse/duty cycle. (d) Alternate process method (PVD) for trench fill.

optimized. It resulted in a successful fabrication of smaller grains and increased occurrence of <111> oriented copper planes.

IV. Conclusions

In this endeavor, a successful demonstration of Cu/dielectric hybrid bonding at fine pitch (~6 µm) with lower post-bond annealing temperatures (⩽ 250° C for 2 hours). Our study delved into the impact of post-trench fill annealing on Cu grain growth. Interestingly, it was found no significant difference in CMP polishing rate or Cu dishing between post-plated Cu with or without annealing. However, a slight increase in surface roughness was noted for annealed Cu wafers and dielectric roughness for non-annealed wafers. Investigations into the bonding interface revealed that smaller grain structures contribute to enhanced interface bonding quality by promoting Cu grain growth compared to larger grain Cu pads. Achieving smaller Cu grains with a high <111> orientation using conventional ECP chemistry and plating parameter optimizations may require intricate process development. Consequently, we have successfully developed and demonstrated an alternative trench-filling method using the PVD process, yielding smaller grains with a high <111> orientation. These findings are crucial for advancing hybrid bonding at lower thermal budgets in future applications.

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