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# Variable Range Hopping-Assisted Parasitic Channel Leakage in AlN/GaN/AlGaN HEMTs on Si

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This work investigates the off-state leakage characteristics of AlN/GaN/AlGaN high electron mobility transistors (HEMTs) on Si substrate with varying mesa depths, and uncovers the existence of a parasitic channel associated with the AlGaN back barrier. Significant differences in off-state leakage up to three orders of magnitude were observed between devices fabricated using different mesa depths. The electrical properties of AlN/GaN/AlGaN HEMTs were measured, it was found that there is a N-type parasitic channel in the unintentionally doped AlGaN back-barrier. Analysis of the isolation test structure, which retains this parasitic channel, reveals a buffer leakage of 12.8 mA/mm and a sheet resistance of 7739.1 Ω/sq, as a result of the parasitic channel. The depletion electric field strength of the parasitic channel is $3.2\times10^5$ V/cm. Temperature-dependent *I-V* curves obtained from the isolation area affirm that the primary leakage mechanism is 2-dimensional variable range hopping (2D-VRH) along the sidewall. As the isolation distance extends from 3 μm to 5 μm, the slope of the fitting line decreases from -53.14 to -126.11 due to increased resistance. [doi:xxx]

GaN-based high electron mobility transistors (HEMTs) are particularly notable among its exceptional properties, having secured a significant portion of the semiconductor market.[1,2] Established growth and manufacturing techniques for GaN millimeter-wave devices on SiC substrates underscore their potential, though cost-efficiency remains a challenge.[3] As technology advances, the cutoff frequency, output power, and efficiency of GaN millimeter-wave devices on Si substrate continue to improve.[4] Additionally, emerging technical features such as larger sizes, complementary Metal-Oxide-Semiconductor compatible processes,[5] and three-dimensional heterogeneous integration[6] are driving costs down and expanding their application prospects.

For GaN HEMTs on Si substrate, the barrier layers typically made of AlGaN, InAlN, and AlN.[7–9] However, during the heteroepitaxial growth process of these barrier layer materials and the GaN buffer with the substrate, certain defects are inevitably introduced. These defects can result in various reliability issues in devices.[10] Consequently, the epitaxial structure and doping concentration of GaN on Si substrate have become the focal points of current research.[11–14] The polarization effect is significant in AlN/GaN HEMTs on Si substrate, leading to the degradation of RF device sub-threshold characteristics and a reduction in electron mobility. The addition of AlGaN back barrier material below the channel layer enables the control of charge carrier movement by adjusting the distribution of electron energy, thus preventing electron spillover and reducing leakage currents.[15-18] Additionally, the back barrier can effectively manage the electric field distribution across the device, enhancing the breakdown voltage and improving the overall robustness of the HEMTs.[19,20] However, the introducing of back barrier can lead to the formation of P or N-type parasitic channel, where electrons may inadvertently accumulate and flow along unintended paths, particularly along the sidewalls of the isolation regions. This phenomenon can severely impact the switching performance of the device.

In this study, we demonstrate the existence of a

parasitic channel at the back barrier AlGaN by etching isolation regions to different depths. Through TLM testing, a sheet resistance of 7739.1 Ω/sq and a saturation current of 12.8 mA/mm was obtained for this N-type parasitic channel. Temperature dependent measurements indicate that electrons primarily move and connect to the N-type parasitic channel through the 2-dimension variable range hopping (2D-VRH)[21] mechanism on the sidewall surface of the isolation region. The findings offer a reasonable explanation for the OFF-state leakage issues observed in AlN/GaN/AlGaN HEMTs on Si substrate.

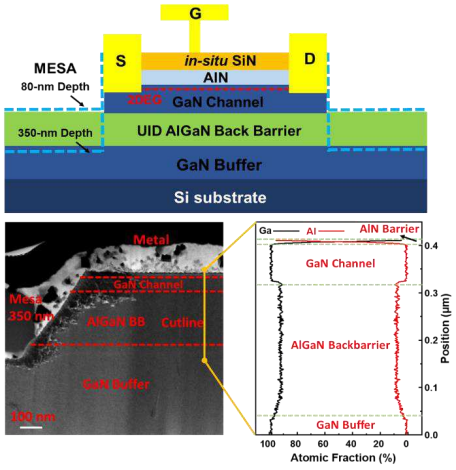


Fig. 1. (a) Schematic cross-section of AlN/GaN/AlGaN HEMTs on Si (without metal pad). (b) Scanning transmission electron microscopy image of epitaxial layers and (c) EDS line scanning of the Al, and Ga elements.

In this work, AlN/GaN/AlGaN epitaxial layers were grown on 6-inch Si substrates using metal-organic chemical vapor deposition (MOCVD). The epitaxial layers consist of a C-doped GaN buffer layer, a 250-nm AlGaN unintentionally doped back barrier layer, an 80-nm GaN channel layer, and a 3-nm SiN cap layer on a 4-nm AlN barrier layer. The Hall measurement at room temperature showed a sheet carrier density of $1.47 \times 10^{13}$ $cm^{-2}$, mobility of 1075 $cm^2/V{\cdot}s$, and sheet resistance of 395 Ω/sq. The source and drain ohmic contacts were fabricated using Ti/Al/Ni/Au via electron beam evaporation, lift-off process, and rapid thermal annealing at 775 ℃ in $N_2$ for 30 s. The transmission line passivation with plasma-enhanced chemical vapor deposition (PECVD) was used to derive the ohmic contact resistance of 0.37 Ω·mm. The mesa region was defined by removing the SiN/AlN/GaN layer with inductively coupled plasma (ICP) etch in $Cl_2/BCl_3$ plasma. Figure 1(a) shows two types of devices were fabricated with mesa depths of 80 nm and 350 nm, respectively. A 360-nm Ni/Au metal was evaporated to form the T-gate. A cross-sectional view of the epitaxial structure and the mesa structure is shown in Figure 1(b).

Using Energy-Dispersive X-Ray Spectroscopy (EDS), the alloy composition of the AlGaN back barrier was determined to be $Al_{0.08}Ga_{0.92}N$, as shown in Figure 1(c). The thickness of the AlGaN back barrier is approximately 270 nm, likely attributed to growth discrepancies. The mesa depth is measured using Atomic Force Microscopy (AFM).

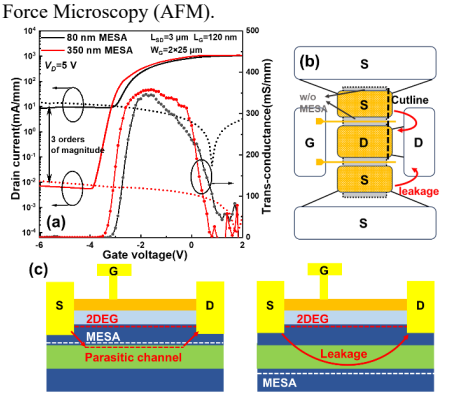


Fig. 2. (a) Transfer sweeps and gate current curves of AlN/GaN/AlGaN HEMTs on Si with different mesa depths. (b) Top view layout of AlN/GaN/AlGaN HEMTs on Si. (c) Illustration of the leakage paths in two devices of different mesa depths (based on the cutline in Fig. 2(b)).

The proposed transistors featuring a gate length ($L_G$) of 120 nm, a source-drain length ($L_{SD}$) of 3 μm were characterized, as shown in Figure 2(a). The layout of the devices is illustrated in Figure 2(b). The device with a mesa depth of 350 nm exhibits favorable transfer characteristics, with a maximum saturation current of 1056 mA/mm, an off-state leakage current of approximately 7.18 μA/mm, and a maximum transconductance of 357.9 mS/mm. The current ON-OFF ratio reaches $10^5$~$10^6$, indicating good subthreshold characteristics and effective gate control over the main 2DEG channel. The result is attributed to the presence of the AlGaN back barrier, which effectively reduces vertical buffer leakage and promotes the confinement of the main 2DEG channel. On the other hand, for the devices with a mesa depth of 80 nm, the saturation current is 1031 mA/mm, maximum transconductance is 345.2 mS/mm, it is comparable to the characteristics of AlN/GaN/AlGaN HEMTs on Si with a 350 nm mesa depth. A lower ON-OFF ratio of $10^2$ was obtained. The off-state leakage current is 8.6 mA/mm, which is 3

orders of magnitude higher than that of the device with 350 nm mesa depth.

As shown in Figure 2(b), in the non-mesa region (indicated in gray in the figure), two source electrodes and one drain electrode are fabricated, forming a gate triode structure with a double-finger gate situated between the three ohmic contacts. Due to the presence of two gate fingers spanning the mesa/non-mesa region in the direction of gate electrode interconnection, any surface leakage in this region and buffer leakage near the sidewall will be mitigated by the gate, theoretically resulting in no leakage condition. In terms of the direction of drain electrode interconnection, the gate finger does not cover the entire region, the leakage channel close to the surface cannot be completely exhausted, thus inadequately addressing sidewall leakage. The leakage channel in this region, as indicated by the red arrow, is between the source and the drain. However, given that the etching process and epitaxial structure used for both devices are identical, the substantial difference in surface leakage cannot be attributed solely to the source-drain leakage path outside the mesa. Therefore, it is hypothesized that the leakage channel predominantly exists on the sidewall or within the mesa structure.

The cross-sectional structures of the devices with varying MESA depths, together with illustrations of the proposed leakage paths, are illustrated in Figure 2(c). For the devices with 80 nm mesa depth, the leakage channel consists of the parasitic channel deep within the epitaxial structure and connected to the ohmic contacts through the mesa sidewalls. This parasitic channel is believed to be associated with surface leakage or body leakage channel, resulting in a significant off-state leakage current. For devices with a mesa depth of 350 nm, the parasitic channel is intercepted at the mesa, and the off-state leakage is primarily influenced by surface and buffer leakage.

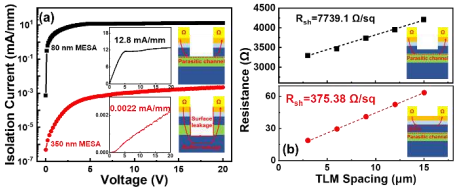


Fig. 3. (a) Isolation leakage with 80 and 350 nm mesa depths with 3 μm Ohmic contact spacing. The insets show the isolation leakage in a linear scale, and the leakage current path. (b) TLM test through the parasitic channel and main 2DEG channel.

To verify the presence of the parasitic channel, as depicted in Figure 3(a), isolation leakage tests were conducted on devices with two different mesa depths. For the sample with a mesa depth of 350 nm, as voltage was increased from 0 V to 20 V, leakage initially surged rapidly from $4.9\times10^{-7}$ mA/mm to $5\times10^{-4}$ mA/mm, followed by a gradual, slower increase. The leakage current of the 350 nm-HEMTs steadily rose to $2.2\times10^{-3}$ mA/mm at 20 V. The leakage is primarily attributed to buffer leakage and partial surface leakage.

Conversely, for the sample with a mesa depth of 80 nm, a leakage current of 1.2 mA/mm was measured at a voltage of 0.4 V, significantly surpassing the standard current of 1 mA/mm that defines device switching. The illustration of the device structure suggests the presence of parasitic channel, leading to isolation leakage. Moreover, as voltage increased, the saturation current rose to 12.8 mA/mm, further affirming the existence of parasitic channel. Interestingly, current saturation was observed in this leakage channel. This behavior did not conform to any known leakage mechanism but resembled the characteristics of conductive channel.

Figure 3(b) illustrates two test structures designed to extract the sheet resistance ($R_{sh}$) of the main 2DEG channel and the parasitic channel. Transmission line model (TLM) indicates that $R_{sh}$ of the parasitic channel was 7739.1 Ω/sq, confirming that this parasitic channel exhibits conductive characteristics similar to those of a 2DEG. This observation confirms the hypothesis regarding the existence of a parasitic channel. The extracted sheet resistance of the main 2DEG channel is 375 Ω/sq, which is close to the result obtained from the Hall measurement (395 Ω/sq).

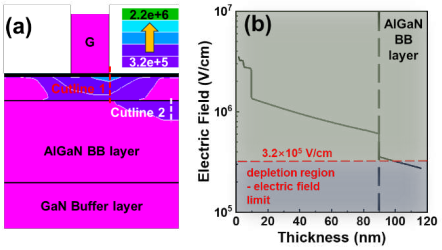


Fig. 4. (a) The electric field distribution (units: V/cm) at bias conditions $V_G$= −6 V, $V_D$=5 V, obtained by simulation. (b) Variation of the maximum electric field with depth of the epitaxial material.

The presence of the parasitic channel induces off-state leakage through the sidewalls of the isolation region, but surface leakage does not propagate through the access region, primarily due to the depletion effect of the gate electrode under negative bias. The simulated electric field profiles at $V_G$=−6 V, $V_D$=5 V are illustrated in Figure 4(a). The electric field intensity at the depletion region of the parasitic channel is $3.2\times10^5$ V/cm, at which

point the top gate could deplete the parasitic channel. For practical device fabrication, a portion of the gate electrodes is placed on the sidewalls, further enhancing the depletion effect of the gate. Therefore, leakage does not propagate through the access region under bias conditions. As shown in Figure 4(b), the electric field intensity gradient at different depths was analyzed. As the thickness gradually increases, the electric field intensity in the depletion region at the parasitic channel gradually decreases until the depth of the AlGaN back barrier reaches 101 nm. In this case, the electric field intensity is not enough to control the parasitic channel.

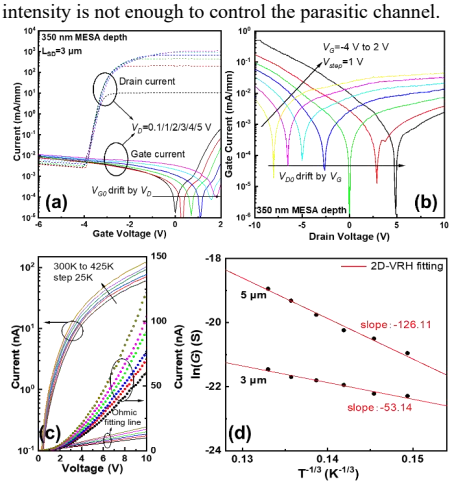


Fig. 5. (a) Transfer sweeps and gate current curves of AlN/GaN/AlGaN HEMTs on Si with different drain bias voltages. (b) Gate current versus drain voltage with different gate bias voltages. (c) Temperature-dependent *I-V* curves of 5 μm isolated Ohmic contacts and Ohmic fitting line at low voltage. (d) 2D-VRH fitting line with different spacings between isolated Ohmic contacts.

Given that the surface leakage mechanisms in AlN/GaN/AlGaN HEMTs on Si with two etching depths are the same, the only distinction lies in whether the parasitic channel is involved in the leakage. Since the devices with a mesa depth of 80 nm have unusual switching characteristics, leakage mechanism analysis was performed on the device with a mesa depth of 350 nm. As shown in Figure 5(a), the transfer characteristics of the device with a source-drain spacing of 3 μm were measured under various drain voltages. With the drain voltage ranging from 0.1 V to 5 V, the off-state leakage exhibited a gradual increase, while the sub-threshold slope remained relatively constant. This phenomenon can be attributed to the role of the back barrier in effectively confining the 2DEG. Concerning the gate current, the gate zero-point voltage $V_{G0}$ continued to drift positively as the drain voltage increased, indicating the influence of drain voltage on gate current. This underscores the dependency of the gate zero-point voltage $V_{G0}$ on drain voltage.

As shown in Figure 5(b), the output characteristics of the device with 80 nm mesa depth were assessed. It was noted that a linear relationship also exists between the drain zero-point voltage $V_{D0}$ and $V_G$. This finding aligns with previous research,[22] confirming that the non-zero switching phenomenon of gate current is unrelated to the access region but is primarily associated with isolation leakage.

In order to investigate the conduction mechanism of sidewall leakage, a variable temperature current test was conducted on two ohmic pads spaced 3 μm apart, covering a temperature range of 300 K to 425 K with increments of 25 K, as shown in Figure 5(c). The leakage current increases with increasing temperature. The low-field leakage current shows ohmic characteristics, as deduced for the *I-V* in linear scale. An ohmic fitting line was applied, and the resulting slope represents the low-field conductance $G$ of the device at each temperature point, consistent with the Variable-Range Hopping (VRH) mechanism.

In the VRH mechanism, electrons jump from one local state (space site) to another local state,[23,24] and the relationship between its conductivity and temperature is as follows[21]:

$$\sigma \propto \exp\left[-T^{-\left(\frac{1}{d+1}\right)}\right] \quad (1)$$

where $d$ represents the dimension, and is 2 in this case.

The hopping probability at a given temperature depends on two parameters: $R$, the spatial separation of the sites, and $W$, their energy separation. In amorphous systems, these parameters are independent and random. Thus, the relationship between jump probability and parameters is described as follows[24]:

$$P \propto \exp\left(-\frac{W}{kT} - 2\alpha R\right) \quad (2)$$

where $\alpha^{-1}$ denotes the attenuation length for a hydrogen-like localized wave-function. Based on this relationship, the variable temperature test results were fitted, as shown in Figure 5(d). Devices with different pitches exhibit temperature-dependent characteristics. Among them, the slopes of the 2D-VRH fitting for the 5 μm and 3 μm ohmic pad spacings are −126.11 and −53.14, respectively. Given that the same mesa etch process was used, the difference in the slope values indicates that the reduction of the spatial component $R$ affects the results. The fitting outcomes indicate that sidewall surface defects are the cause of device reverse leakage. For devices with varying mesa depths, the same

etching process results in the same degree of surface defects. Consequently, for the devices with a mesa depth of 80 nm, electrons establish a connection between the ohmic pad and the parasitic channel on the sidewall surface through 2D-VRH, leading to a poor ON-OFF ratio.

In conclusion, this study confirmed the presence of a parasitic channel in AlN/GaN/AlGaN HEMTs on Si, associated with the AlGaN back barrier, with a measured $R_{sh}$ of 7739.1 Ω/sq. The temperature-dependent *I-V* test demonstrated that sidewall leakage in the isolation region is primarily governed by the 2D-VRH mechanism. The findings of this work offer insights into potential issues in AlN/GaN/AlGaN HEMTs on Si substrate through the analysis of the leakage mechanism and the demonstration of N-type parasitic channel.

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