Development, Testing, and Integration of Silicon and Glass Substrates for Advanced Ion Trap Design

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Surface electrode ion trap is a promising candidate for quantum information processing (QIP), due to its feasibilities towards large-scale fabrication and on-chip electro-optical integration. In this paper, surface electrode ion traps on different substrates (e.g., high-resistivity silicon, silicon with ground plane and glass) are fabricated, assembled and tested. To simultaneously leverage the established fabrication technique of silicon and superior insulation property of glass, we further demonstrate a novel ion trap design with heterogenous integration of silicon and glass, acting respectively as ion trap and interposer substrates. The vertical connection between the silicon ion trap and the glass interposer is achieved by through silicon via (TSV) and micro bump. This silicon-glass integrated system advances the development of ion trap and enriches the toolbox of scalable QIP.

Standard back end of line CMOS process is used for the fabrication of ion traps on both silicon and glass substrates. With 12-inch silicon/glass wafers, ~2,000 traps with different design dimensions can be fabricated simultaneously. For ion trap on high-resistivity silicon substrate (HR trap, Fig. 1(a)), lithography-defined electroplating of 3.7 µm Cu with Au finish is conducted on top of 3 µm patterned SiO_2 layer. For ion trap on silicon with grounding plane (GND trap, Fig. 1(b)), 1 µm Cu damascene process is used to form the meshed grounding plane that shields silicon substrate from RF signal penetration. For ion trap on glass substrate (glass trap, Fig. 1(c)), Cu and Au can be directly electroplated onto glass substrate after adhesion and seed layers deposition. To evaluate the RF performance of various traps, *S* parameter measurement and resonator test are conducted. Fig. 2(a) and (b) show that glass trap features extremely low RF loss as compared to silicon counterparts.

Heterogenous integration of silicon ion trap and glass interposer with TSV interconnections (TSV trap, Fig. 1(d)) is thus proposed, in which the possibility of monolithic integration of photonics (e.g., grating couplers, waveguides) and electronics (DACs) components is preserved on the silicon ion trap chip, whereas the RF performance of the entire device can be guaranteed by the glass interposer. As shown in Fig. 1(e) and (f), grating couplers can be implemented into the silicon trap chip. Additional grounding layer with designed openings on top of grating couplers is introduced to further minimize RF loss. $^{88}Sr^+$ ions are successfully trapped on both glass and TSV traps (Fig. 2(c) and (d)).

In summary, this work discusses the performance of ion traps on various substrates and demonstrates the silicon-glass integrated system to enable the scalability of surface electrode ion trap.

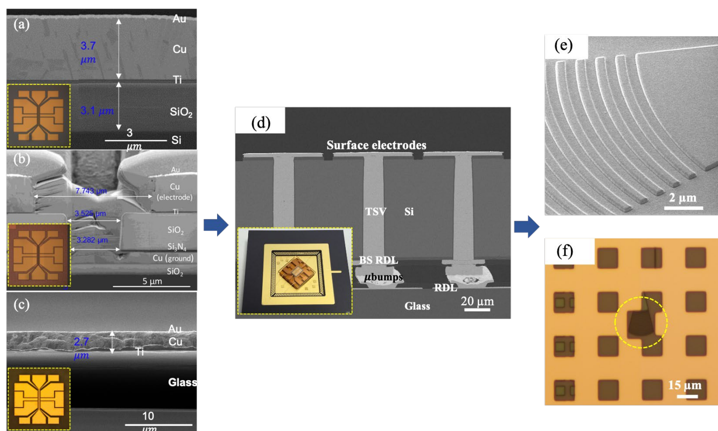

Figure 1. (a-c) Cross-sectional SEM images of HR trap, GND trap and glass trap. The insets are optical images of corresponding traps. (d) Cross-sectional SEM image of heterogenous-integrated TSV trap that has silicon trap and glass interposer. (e) Grating coupler designed for 1092 nm wavelength, which is integrated into the silicon trap for on-chip optical repumping of $^{88}Sr^+$ ion. (f) Grounding plane with openings on top of the output grating coupler.

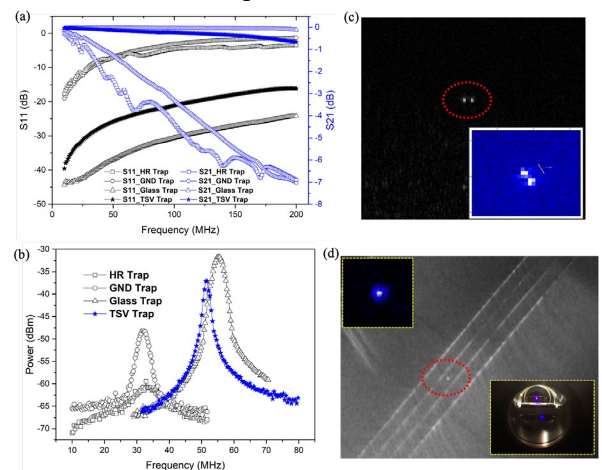

Figure 2. (a,b) S parameter and resonator test results of ion traps with different substrates. The TSV trap features a low insertion loss and a high resonance peak, which are close to those of glass trap. (c) Fluorescence image of two trapped ions on glass trap (the inter-ion distance is ~7 µm). (d) Fluorescence image of single trapped ion on TSV trap. The inset below the trap in the trapping chamber.

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